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Numerical Simulation of Field-effect Transistor GAA SiNWFET Parameters Based on Nanowires

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A perspective way for further increase in MOSFET transistors scaling value is the usage of Si, GaAs, ZnO nanowires and carbon nanotubes as channels between the source and drain. In this work, we present the results of a numerical simulation of 3D transistors with five *n*-type Si (SiNWFETs) channels based on SOI (Silicon-on-Insulator) technology and Gate-all-around (GAA) structure. 5-channel GAA SiNWFET structures are simulated by Silvaco TCAD tools. Their distinct electrical characteristics are demonstrated, in particular, the valid values of threshold voltage V_t, subthreshold scattering SS, drain induced barrier lowering (DIBL), leakage current I_{off} and I_{on}/I_{off} coefficient are obtained. The effect of temperature on static transmission characteristics is studied. A typical view of the MOSFET dependencies is obtained: the intersection of operating characteristics for different temperatures at a constant drain voltage due to a decrease in the switch-on current and threshold voltage V_t, the corresponding decrease in charge carrier mobility and energy redistribution of carriers, the Fermi energy shift to the middle of the band gap and the formation of a depleted region near the semiconductor surface at lower values of the electric field strength. At a fixed drain voltage of 1.2 V a further temperature increase in the range of 280-400 K leads to a decrease in the threshold voltage V_t by 22.5 %, an increase in the subthreshold scattering SS by 43.1 %, a decrease in the switch-on current by 10.7 % and a decrease in DIBL by 12.6 %.

Keywords: SOI GAA SiNWFETs, Nanowire, Short-channel effects, Temperature effects.

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1. INTRODUCTION

The continuously increasing requirements for increasing productivity, decreasing energy consumption and widening the usage areas of nanowire field transistors (NWFETs) compared to MOSFET transistors, which are widely used in sensor electronics and medicine, stipulate the necessity of study their structural features, working characteristics, etc. [1-3]. Recently, the use of Si, GaAs, ZnO nanowires as NWFET channels of Gate-all-around (GAA) type is considered as a way to improve the characteristics described above. The authors of [1, 2] have studied the dual-metal gate (DMG) GAA NWFET structures as a complex simulation – from simulation of the technological fabrication processes to such parameters as the influence of the grown texture orientation and the distribution of components in the gate on the effective work function (W_{eff}) values [4]. The data obtained by these authors indicate the prospects of using these nanoscale structures as candidates for the formation of the next generation of nanowire transistors.

Among them, except the possibility of further nanoscale procedure, GAA NWFETs have excellent gate controlling, short-channel effects (SCEs) stability [5, 6], etc. As an example, in paper [7], structural models of a 5-channel GAA NWFET were designed and their performance characteristics were compared depending on the operating conditions. The authors of [8] showed that NW-channel transistors have better operating characteristics than FinFETs, their concentration and other dependencies were analyzed. It should be noted that a similar methodology is successfully used by the authors [8] in other cases, such as for compact simulation of film photoconverters [9]. The authors of [10] demonstrated unified models of vertical GAA FETs with channels based on NWs and nanosheets (NSs) realized by 3-nm technology. It has been shown that these structures have a bigger speed and lesser power consumption than FinFETs.

The aim of this work is to study the influence of temperature on the operating characteristics of five *n*-channel GAA SiNWFETs using Silvaco TCAD simulation software.

2. NUMERICAL SIMULATION PROCEDURE

Silvaco TCAD is a package of programs which are connected to each other and this connection can be realized as a block-sheme presented in Fig. 1. The basic structural element is DeckBuild [11], because it creates and executes batch files, the order of actions is set, there are other components running which are subsequently coordinated there. A numerical simulation of the operating characteristics and structural elements is executed using Atlas device simulator [12]. Most Atlas models use two types of input data. The first type is program code (ASCII), which consists of the necessary execution commands, the second one is a geometry file which estimates a 2D or 3D device structure, its areas and doping profiles.

Three types of output data are generated in the Atlas simulator. The first type is a program execution report which informs the user about code execution stages and presents information about errors and alerts during the simulation. The second type of output data is the journal's file which consists of all terminal voltage and current values during device simulation. It is generated using "Solve" or "Extract" commands and as usual has ".log" or ".dat" extension. Each of them represents an ASCII code written in a data table. The third type of output data is a solution file or a ".str"

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structured file that stores graphical data connected with the variation data determined earlier by pointers.

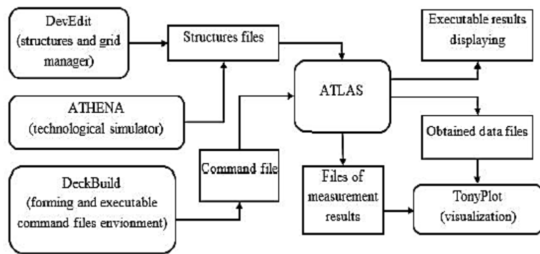

Fig. 1 – Silvaco TCAD structural scheme

Let us consider the alhorithm of designing a GAA NWFET compact model using Silvaco TCAD:

1. In "DeckBuild" working directory, an ".in" command file is created.

2. In Atlas, an initial 3D grid structure and Si substrate area with an oxide-covered surface are specified.

3. Commands for storage and view of a ".str"-structure in TonyPlot3D are added to the command file; on the basis of the grid data and TonyPlot3D visualization it is necessary to simplify the grid in the substrate area using "Eliminate" commands.

4. Creation of the gate of a FET-structure; in case of multilayer solutions, it is necessary to check the order of the area set –first, surface layers are created and second – inner layers, respectively.

5. Creation of the GAA NWFET channel – analogue to the gate multilayer structure. It should be noted that in the Atlas package it is possible to form areas only in the case of rectangular parallelepipeds, so to simulate the areas with a complex shape additional algorithms are used to make it possible to utilize overlapping layers.

6. Setting the areas of source and drain structures. Setting the electrode structures – in this case it needs to use field-effect transistor nomenclature.

7. Setting the channel doping profile corresponding to the type of conductivity. The feature of 3D structure formation in Atlas should be checked – when setting up an irregular distribution, it is necessary to set a doping profile for each 2D structure in the selected direction. Wherein, the plane coordinates can coincide with grid knots; checking of the doping profile can be provided in TonyPlot3D by grabbing all areas except the channel and, subsequently, by setting the appropriate visualization mode.

8. Specifying (as necessary) the additional commands for setting the electrical parameters of materials and contact structures.

9. Setting the models and methods for analyzing FET in the ATLAS program, specifying the commands for the initial measurement procedure.

10. Carrying out the analysis of the created structure: calculation of the *I-V* curves; calculation of the transmission *I-V* dependencies of the drain-source currents on the gate voltage value ($I_{DS}(V_G)$) at constant values of drain-source voltages, in this work V_{DS} had values of 0.1 eV and 1.2 V; calculation of the output *I-V* dependencies of drain-source currents on the drain-source voltage $I_{DS}(V_{DS})$ in case of the channel saturation current during the variation of the gate voltage V_G; it should be noted that in case of *p*-type transistors V_G will be negative.

11. Calculation of the following parameters [12]: V_t, SS, I_{on}, I_{off}, I_{on}/I_{off} and DIBL. The I_{off} value can be determined from the low-voltage *I-V* curve by changing the "MAX" function to "MIN" in the equation to extract the maximum current value. The DIBL value is calculated as the ratio of the initial voltage difference V_t to the difference of V_{DS} values.

It should be noted that the ATHENA process simulator [13] allows to simulate the processes of deposition, diffusion, oxidation, etching and so on in the case of 2D structures.

3. DEVICE STRUCTURE

In this section, we present the results of numerical simulation of SOI GAA SiNWFET 3D structures using Silvaco TCAD tools.

To measure the electrical characteristics of 5-channel GAA SiNWFET, the corresponding structures with a channel length of 30 nm and a round-like cross-section of nanowires were designed. Transistors had a gate length $L_G = 14$ nm and a nanowire diameter $D_{NW} = 8$ nm, their geometry is presented in Fig. 2a.

When designing the structures, the following configuration of channel doping profiles was used: in the channel volume the concentration of acceptor impurity was $5 \cdot 10^{15}$ cm^{-3}; in the near-contact (drain and source) areas, donor impurity with a higher concentration of $5 \cdot 10^{18}$ cm^{-3} was doped. The corresponding concentration distribution of acceptor impurities in channels is presented in Fig. 2b.

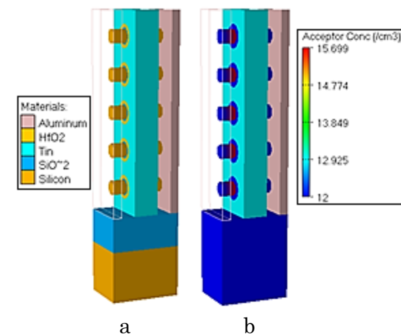

Fig. 2 – Structures of a 5-channel GAA SiNWFET with a presentation of their geometry (a) and concentration distribution of acceptor impurities inside the channels (b)

The efective work function of the gate electrode was 4.4.0 eV in case of *n*-type conductivity [4]. HfO_2 ($k = 22$) with a thickness of 2 nm was used as a high-k dielectric layer, SiO_2 situated under high-k dielectric layer with a thickness of 1 nm (Fig. 2a) was chosen as a barrier layer.

4. SIMULATION AND RESULTS

Typical I_{DS}-V_{GS} dependencies at temperatures of 280, 300, 340, 360, 380 and 400 K for the proposed 5-channel GAA SiNWFET structures with *n*-type conductivity in case of fixed drain-source voltage values $V_{DS} = 1.2$ V and $V_{DS} = 0.1$ V are presented in Fig. 3.

With increasing temperature, a number of typical variations in the static transmission characteristics of a 5-channel *n*-type GAA SiNWFET are detected, which are caused in general by the following physical

processes [5, 6]. 1) with an increase in temperature in the studied range, a decrease in the mobility of charge carriers is observed that leads to a decrease in the I_{on} value. 2) In the case of the proposed structures, the position of this point is situated close to the following values: $I_{DS} = 1.9 \cdot 10^{-5}$ A, $V_{GS} = 0.65$ V (see Fig. 3a) and $I_{DS} = 1.0 \cdot 10^{-5}$ A, $V_{GS} = 0.55$ V (see Fig. 3b).

Calculation of the DIBL values at fixed temperatures of 280 K and 400 K showed its negligible decrease from 36.4 to 31.8 mV/V (Fig. 4). During the temperature variation, the energy redistribution of carriers and a shift of the Fermi level towards the middle of the band gap are observed.

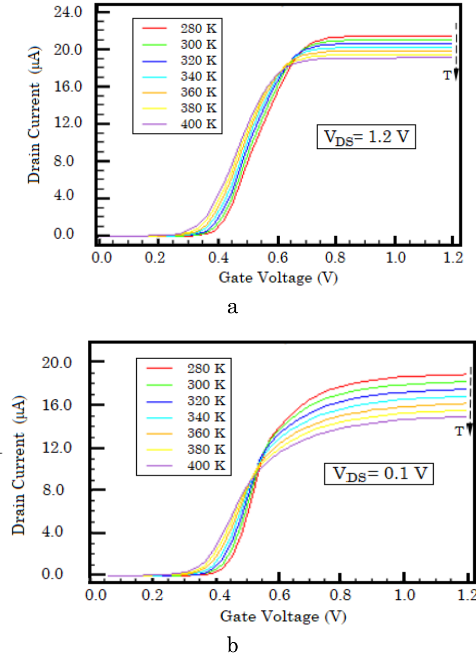

Fig. 3 – I_{DS}-V_{GS} curves of 5-channel GAA SiNWFET n-type transistors as a function of temperature variations and fixed drain-source voltage values of 1.2 V (a) and 0.1 V (b). The arrow direction indicates an increase in temperature

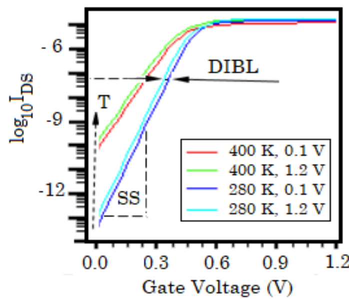

Fig. 4 – $\log_{10}(I_{DS}$-$V_{GS})$ curves of 5-channel GAA SiNWFET n-type transistors as a function of temperature variations and fixed drain-source voltage values of 1.2 V (a) and 0.1 V (b). The arrow direction indicates an increase in temperature

This effect leads to the formation near the semiconductor surface of a depletion level (inversion layer) at lesser electrical field strengths. Therefore, with increasing temperature, the value of the initial voltage V_t decreases. As a result of the above described effect, the static transmission characteristics are presented in case of the constant initial voltage at the source. But these characteristics at different temperatures intersect. This can be caused by the presence of the so-called "thermal stable point", where the opposite effects are compensated and channel current (drain current) is conctant.

5-channel GAA SiNWFET operating characteristics at the drain-source voltage values $V_{DS} = 1.2$ V are presented in Table 1. It should be noted that at room temperature ($T = 300$ K) V_t and SS values are 0.39 V and 62.00 mV/decade, respectively. Currents I_{on}, I_{of} and I_{on}/I_{of} coefficent values are $2.11 \cdot 10^{-5}$ A, $0.53 \cdot 10^{-12}$ A and $40.26 \cdot 10^{6}$ a.u., respectively.

Table 1 – The parameters used for 5-channel GAA SiNWFETs as a function of working temperature

Parameters	Working temperature						
	280 K	**300 K**	**320 K**	**340 K**	**360 K**	**380 K**	**400 K**
V_t, V	0.40	0.39	0.37	0.36	0.34	0.33	0.31
SS, mV/decade	57.79	62.00	66.10	70.20	74.31	78.41	82.52
$I_{off} \times 10^{12}$, A	0.11	0.53	2.10	7.23	21.79	58.86	144.76
$I_{on} \times 10^{5}$, A	2.15	2.11	2.07	2.04	1.99	1.95	1.92
$(I_{on}/I_{off}) \times 10^{-6}$	198.32	40.26	9.85	2.81	0.92	0.33	0.13

In this case, with an increase in the working temperature from 280 to 400 K, the initial voltage V_t decreases by 22.5 %, the SS value increases by 43.1 %, and the switch-on current decreases by 10.7 %. It should be noted that the temperature dependence of dielectric parameters leads to a rapid increase in the drain current. In particular, it is well-fixed at increased temperatures of 380 K and 400 K, and, moreover, negatively influences the curvature of transistor transmission characteristics. Obtained results are well-correlated with the results obtained by us and other authors in case of SiNW FETs [1-3, 7, 14-16] and FinFETs [3, 4, 7]. It should be noted that direct studies of the structure and phase states, electrophysical properties of thermal-stable bimetallic film alloys have been obtained by theauthors in [17-20]. The obtained results have shown that the studied structures can be used as gate contacts for CMOS (see, for example, [4]).

5. CONCLUSIONS

GAA SiNWFET structures with 5 n-type channels doped with acceptor impurity with a concentration of $5 \cdot 10^{15}$ cm^{-3} have been successfully designed and the influence of the working temperature of 280, 300, 340, 360, 380 and 400 K on static transmission and other operating characteristics has been studied. The typical temperature dependencies have been obtained, the view of which may be caused by the well-known theories [5, 6] in the case of MOSFET transistors.

As a conclusion, it is necessary to note that obtained results can be used in further studies of nanoelectronic 3D devices.

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Числове моделювання параметрів польових транзисторів GAA SiNWFET на основі нанодротів

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Перспективним напрямом подальшого зростання рівня масштабування MOSFET транзисторів вважається застосування нанодротів Si, GaAs і ZnO та вуглецевих нанотрубок як каналів між витоком та стоком. У даній роботі представлені результати числового проектування 3D-транзисторів з п'ятьма *n*-каналами Si (SiNWFET), виготовленими за технологією SOI (Silicon-on-Insulator) із затвором Gate-all-around (GAA). Структури 5-канальних GAA SiNWFET транзисторів моделюються за допомогою інструментів Silvaco TCAD. Проведено моделювання електричних характеристик, отримано допустимі значення порогової напруги, допорогового розкиду, зниження бар'еру, спричинене стоком, DIBL, сили струму витоку I_{off} та коефіцієнта I_{on}/I_{off}. Досліджено вплив температури на статичні передавальні характеристики польового транзистора, отримано типовий для MOSFET транзисторів характер залежностей: перетинання робочих характеристик для різних температур при постійній стоковій напрузі, що обумовлено зменшенням величини сили струму "switch-on" та порогової напруги внаслідок відповідного зменшення рухливості носіїв заряду та перерозподілу носіїв по енергіям, зміщенням енергії Фермі до середини забороненої зони та утворенням області збіднення біля поверхні напівпровідника при менших напруженостях електричного поля. При фіксованій напрузі на стоці 1.2 В зростання температури в інтервалі від 280 до 400 К призводить до зменшення порогової напруги V_t на 22,5 %, збільшення допорогового розкиду на 43.1 %, спадання сили струму "switch-on" на 10.7 % та зниження бар'еру, спричинене стоком, DIBL на 12.6 %.

Ключові слова: SOI GAA SiNWFETs, Нанодроти, Короткоканальні ефекти, Температурні ефекти.