TEMPERATURE DEPENDENCE of RESISTIVITY OF POROUS SILICON FORMED ON N+ SUBSTRATES

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ABSTRACT

Results of measurement of resistivity of mesoporous silicon formed on n-type substrates in a wide temperature range are presented. Measurements show that at low temperatures there is a growth of resistance of four orders of magnitude compared to that at room temperature which occurs in a relatively narrow temperature range.

Key words: porous silicon, resistivity, space charge region

INTRODUCTION

Electrical properties of porous silicon (PS) are of great importance for engineering of PS-based electronic devices. It is well known that the conductance mechanisms of PS differ from that of bulk silicon [1]. Especially it concerns temperature dependence of resistivity. But the exact mechanism of the electronic transport in PS layers isn't ultimately understood up till now. Different approaches were developed during last years. They are based on the band gap modulation via quantum confinement effects in silicon crystallites forming porous silicon skeleton, on the hopping at the Fermi level mechanism, on the thermionic emission above energy barriers and on the space charge models [2 – 5]. None of them explains satisfactory the resistivity versus temperature dependencies.

In this work, in order to clarify the conductance mechanisms of PS, we perform the investigation of mesoporous silicon resistivity behavior in a wide temperature range: from 300 K down to 10 K.

SAMPLES CHARACTERIZATION AND MEASURING TECHNIQUE

PS samples used for the measurements were prepared by electrochemical anodization technique. Antimony-doped 0.01 Ohm·cm wafers with (111) orientation and standard thickness of 450 μm were used. PS layers were formed in

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$HF:C_3H_7OH:H_2O = 1:3:1$ solution at current density of 65 mA/cm^2 using polytetrafluorethylene cell. The resulting PS layers had total thickness 10 μm and porosity 55%. Vertical pores had diameter in the range 20 nm – 30 nm. Such material can be classified as mesoporous.

In order to carry out the resistivity measurements samples were cut in pieces 20 mm × 10 mm. The resistivity measurements were performed with four probe method using current-in-plane configuration. Electrical contacts to PS layer were made by indium attached directly to PS. In this case the structure under study can be treated as consisting of two layers: highly doped N+ substrate and PS itself. The transport measurements were performed in a ^{4}He cryostat in a temperature interval 300 K – 10 K.

The same measurements were carried out for silicon sample without porous layers in order to clarify their role in the conductance mechanism.

RESULTS AND DISCUSSION

The typical curves, representing results of measurements of resistance versus temperature for both Si and PS are shown in *Fig. 1*.

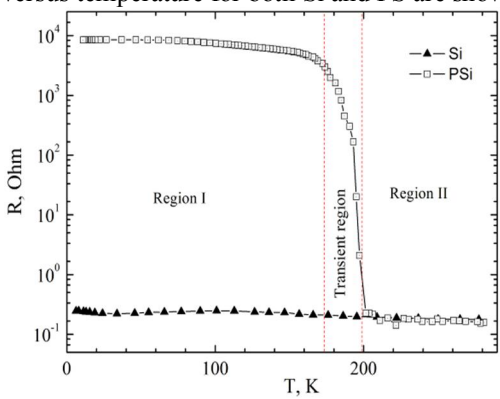

Fig. 1 – The measured resistance versus temperature behavior of Si and PS

Two distinctive regions can be found in Fig. 1 for PS. In the region I ($10\ K < T < 170\ K$) the resistivity value is approximately 4 orders of magnitude higher that in the region II ($200\ K < T < 300\ K$), for which resistivities of Si and PS are equal. Moreover it drops in the rather narrow temperature range, $170\ K < T < 200\ K$.

We believe that such giant increase of resistivity of the investigated structure below 200 K is caused mainly by change of the space charge region width in PS.

Indeed, assuming that the Fermi level at the PS surface is fixed at about the middle point of the band gap we can calculate the free space charge region (SCR) width using the following equation [6]

$$W_d = \sqrt{\frac{2 \cdot \varepsilon_0 \cdot \varepsilon_r \cdot V_{bi}}{q \cdot n}}, \qquad (1)$$

where W_d is the free space charge region width; ε_0 is the dielectric constant; ε_r is the permittivity of Si; V_{bi} is the surface potential value; q is the

charge of electron, n is the charge carrier concentration.

The results of calculations of W_d values for three different temperatures related to two different temperature regions are presented in a *Table 1*. Here we reasonably assume V_{bi} = 0.5 eV.

Table 1 – Key PS parameters at different temperatures

T, K	n, cm^{-3}[6]	W_d, nm
300	$3.3 \cdot 10^{18}$	14
200	$2.82 \cdot 10^{18}$	15
100	$1.95 \cdot 10^{18}$	18

In our estimations the variation of the effective impurity concentration in porous silicon compared to that in substrate is neglected. As we see the SCR width values at room temperature are quite close to the pores skeleton dimensions (20 nm – 30 nm). We have to note, that the electron mean free path change with temperature is less with respect to the change of the SCR width. When temperature lowers, the SCR area in the pores increases, thus leading to reduction of the part of the skeleton where the charge carriers have less scattering, see *Fig. 2*.

The above mentioned fact will have a significant influence on the resistivity of PS and thus the overall structure resistivity, up to the moment of overlapping of space regions of neighboring pores. As we suppose it is exactly the space charge region overlapping that causes such significant increase of the resistivity of the measured structure with lowering the temperature.

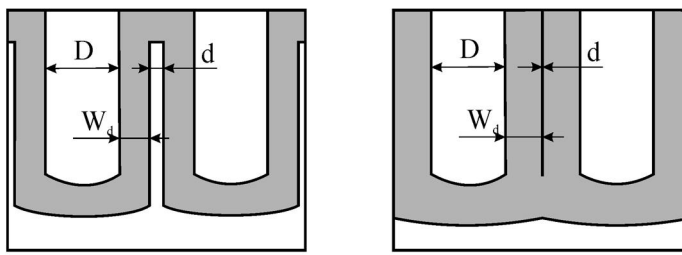

Fig. 2 – Sketch of the PS representing two pores with SCR and undepleted region at two different temperatures. (a) T > 200K, (b) T < 170K. D is the pore inner diameter, d is dimension of the undepleted region

CONCLUSIONS

In the present work the lateral resistivity of mesoporous silicon on the n^+ substrate was investigated in the wide temperature range. It was found that the resistivity value changes by four orders of magnitude while the temperature is lowered from 300 K down to 10 K. The most significant change takes place in the temperature range 200 K – 170 K. We believe that such giant growth of

resistivity is related to the overlapping of the SCR of neighboring pores while lowering the temperature. Estimations of SCR width at different temperatures strongly support this hypothesis.

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