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Pt-Ti/ALD-Al_2O_3/p-Si MOS CAPACITORS FOR FUTURE ULSI TECHNOLOGY

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The high dielectric constant (high-k) thin film of Al_2O_3 was deposited by using Plasma enhanced atomic layer deposition (PE-ALD) technique. The electron beam evaporation system was used to deposit the Pt-Ti metal to fabricate the Pt-Ti/Al_2O_3/Si MOS capacitors. Thickness measurement of Al_2O_3 gate dielectric was carried out with variable angle spectroscopic ellipsometry, which is measured to be 2.83 *nm. The MOS capacitors were characterized to evaluate the electrical properties using capacitance voltage (C-V) analyzer at different measurement frequencies. Capacitance voltage measurement shows that, dielectric constant k ranges from* 7.87 *to* 10.44. *In CV curve a slight negative shift is observed in the flatband voltage because of presence of trap charges in the Al_2O_3 MOS capacitor. A lower equivalent oxide thickness (EOT) of* 1.057 *nm is obtained for the fabricated Pt-Ti/Al_2O_3/Si MOS capacitors.*

Keywords: *Al_2O_3, HIGH-K, GATE DIELECTRIC, MOS CAPACITOR, ELLIPSOMETER, C-V, ALD.*

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1. INTRODUCTION

The scaling down of Complementary Metal Oxide Semiconductor (CMOS) transistors requires replacement of conventional SiO_2 layer with high-k material for gate dielectric applications. The performance of silicon ULSI circuits depends on the capability of the MOSFET, especially the processing speed and electrical power dissipation which are dependent on the geometrical size of MOSFET. In order to reduce the gate leakage current, and also to maximize gate capacitance, recent efforts have been made to replace gate silicon-oxides (SiO_2) and oxynitrides (SiON) with high-k materials such as HfO_2 [1], ZrO_2 [2], $LaAlO_3$ [3], TiO_2 [4], Al_2O_3 [5, 6] and CeO_2 [7]. Thin films of high-k dielectrics possesses properties such as high thermal stability, high dielectric constants (k ~ 10-80) and large band gap (> 5.6 eV) that makes them applicable in the field of advanced CMOS technology. In the advanced CMOS technology, high-k materials are used as an insulator in gate stacks. Interfacial layers consisting of SiO_2 are usually formed between the Si substrate and the high-k layers. As SiO_2 has a lower dielectric constant than the high-k material these SiO_2 interlayers account for a significant increase in the total equivalent oxide thickness (EOT). The direct deposition of high-k on Si without an interface layer would reduce this increase in EOT. The oxide layer on the Si substrate needs to be removed by hydrofluoric acid (HF)

treatment before the deposition of high-k thin film. Because HF-treated Si surfaces become hydrophobic with hydrogen terminated Si bonds, it has been reported that unfavorable growth features such as island growth appear on hydrophobic surfaces [8]. The Al_2O_3 thin film with a dielectric constant of 9 is one of the candidate materials to replace SiO_2 because of its high energy gap 7-8 eV and its thermodynamic stability on Si to reduce the tunneling current for the same gate capacitance [9]. The deposition methods and the deposition conditions tend to determine the crystallinity and purity of a deposited dielectric thin film. High temperature annealing can result in the crystallization and densification of a dielectric material. A variety of techniques are available for the deposition of high-k layer on Si substrate, such as RF Sputtering [10], PLD [11], Thermal Evaporation [12], Electron beam evaporation [13], LPCVD [14], sol gel [15], Atomic layer deposition [16]. A promising new method of depositing very thin films has been developed for a variety of applications, including gate dielectrics, capacitor dielectrics, and diffusion barriers. The new technique, called atomic layer deposition (ALD), solves many of the most significant problems associated with traditional thin-film deposition technologies, including conformal film deposition over high-aspect ratio structures, high-temperature processing, large-area film uniformity, and accurate film thickness control.

In this paper, we report the details of fabrication and characterization of Pt-Ti/ALD-Al_2O_3/p-Si MOS capacitor. The second section of paper describes the experimental details. The results are discussed in third section and the fourth section concludes the paper.

2. EXPERIMENTAL

The *p*-type Si $\langle 100 \rangle$ substrates were cleaned by a RCA process. After the RCA treatment, the substrates were dried and put into the deposition chamber of PE-ALD (Model-Oxford FlexAL) system. Trimetyl Aluminium (TMA) was used as precursor material for 10 cycles at substrate temperature of $300^{\circ}C$ in ALD chamber for the Al_2O_3 deposition. The Pt-Ti metal contacts were formed by electron beam evaporation system (CHA model no. SEC-600) through shadow mask with electrode area of 1.77×10^{-4} cm^2 to fabricate the MOS capacitors, where Ti and Pt have thickness of 2 nm and 20 nm at the deposition rate 0.2 Å/sec and 0.5 Å/sec respectively. Rapid thermal annealing (RTA, AET Model No-RX-6) was performed on the fabricated Pt-Ti/ALD-Al_2O_3/p-Si MOS capacitors at 350 °C in a forming gas environment (N_2:H_2, 90:10) for 30 minutes. Aluminum was deposited as the backside contact using thermal evaporation system.

3. RESULTS AND DISCUSSION

3.1 Ellipsometry

The films of Al_2O_3 were characterized for measurement of thickness using the variable angle spectroscopic ellipsometry (M2000DI JA Woollam Co-Inc) at 632.8 nm, the thickness of the films was found to be 2.83 nm. The minimum equivalent oxide thickness (EOT) of 1.057 nm has been determined by using physical thickness (2.83 nm) of Al_2O_3 layer and dielectric constant obtained from the capacitance voltage (C-V) measurement, which is compatible to the current technology nodes.

3.2 Capacitance-Voltage (C-V) Measurement

The Pt-Ti/Al_2O_3/Si MOS capacitors were characterized using the single sweep capacitance voltage (C-V) analyzer (Agilent 4284A LCR meter) at 100 kHz, 500 kHz and 1 MHz frequencies. The accumulation capacitance is observed to be low due to existence of series resistance from experimental/measurement errors. This series resistance affects the dielectric constant of the high-k thin films. The series resistance is determined to be 374 Ω and its effect has been eliminated from the measured C-V curve. The dielectric constant of the Al_2O_3 thin film determined from the corrected accumulation capacitance, physical thickness of high-k thin film and Pt-Ti gate electrode area was in the range of 7.87 to 10.44. In CV curve a slight negative shift is observed in the flatband voltage because of presence of positive trap charges in the Al_2O_3 MOS capacitor. The frequency dispersion in corrected CV curves is observed in Figure 1 may be due to the presence of trap charges.

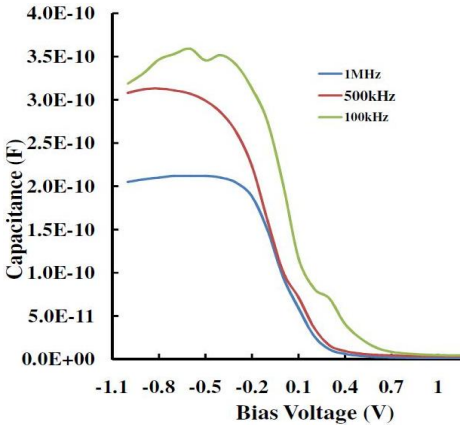

***Fig. 1** – Capacitance-Voltage curve of Pt-Ti/Al_2O_3/Si MOS capacitor*

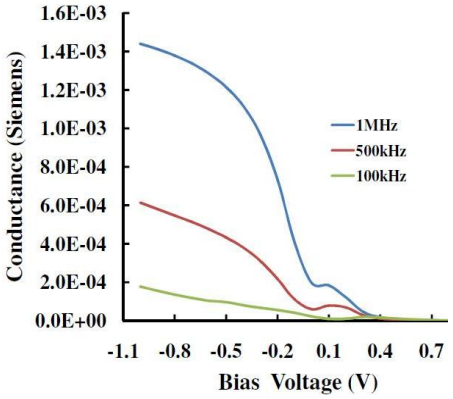

***Fig. 2** – Conductance-Voltage curve of Pt-Ti/Al_2O_3/Si MOS capacitor*

3.3 Conductance Voltage (G-V) Measurement

The conductance voltage measurement of the fabricated Pt-Ti/Al_2O_3/Si MOS capacitor is also noted at different frequencies such as 100 *k*, 500 *k* and 1 MHz. It is observed from the Figure 2 that, the conductance value increases as the measurement frequency increases. The interface trapped density is determined using the G-V curve which is in the range of 1.3832×10^{13}-1.9937×10^{13} $eV^{-1}cm^{-2}$.

4. CONCLUSION

The Pt-Ti/Al_2O_3/Si MOS capacitors were fabricated by the PEALD technique with precise control over the thickness of the Al_2O_3 thin film, resulting in the minimum equivalent oxide thickness of 1.057 nm. The interface traps charges are determined in the range of 1.3832×10^{13}-1.9937×10^{13} $eV^{-1}cm^{-2}$ at the Si/ Al_2O_3 interface for different frequencies. The dielectric constant of Al_2O_3 gate dielectric layer is estimated in the range of 7.87 to 10.44 with varied frequencies, which is well compatible with the current technology nodes.

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