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ACTIVATION ENERGY OF POLYCRYSTALLINE SILICON THIN FILM TRANSISTOR

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The activation energy of a poly-Si thin film transistor is observed to be influenced by the grain size, trap state density and the inversion layer thickness. The present study aims to investigate these parameters theoretically so as to explore optimum conditions for the working of a polycrystalline silicon thin film transistor. Our computations have revealed that the activation energy decreases with the increase of gate bias for all values of grain size, trap states density and the inversion layer thickness. These findings are compared with the experimental results.

Keywords: ACTIVATION ENERGY, POLYSILICON, TFT, GRAIN SIZE, TRAP STATE DENSITY.

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1. INTRODUCTION

Polycrystalline silicon film transistors are receiving significant attention because of recent application of high speed pixel switching devices in active matrix liquid crystal displays (AMLCDs) and have been widely used in switches, drivers and analog circuits. Currently the poly-Si TFTs are used in various fields such as solar cells and 3D integrated circuits because of their high field effect mobility and driving current. These devices are a promising candidate to be used in the fully integrated flat panel display system on panel (SOP) as a controller and memory. The Device simulation of poly-Si TFTs is playing an important role in predicting and analyzing the device characteristics. It is the most promising display because of higher resolution, lower power consumption, smaller module size and higher module durability [1-3].

Polysilicon is composed of silicon crystallites with a grain boundary in between two crystallites. Defects caused by incomplete atomic bonding and disordered material in the boundary result in trapping state that reduce the number of carriers and create space-charge regions in the crystallites. After trapping of charges at the grain boundary a potential barrier is developed. If there is no potential barrier at the grain boundary then the activation energy for the source-drain current depends on the surface potential and is simply the difference in energy between the valance band and Fermi level at the surface and if the barrier forms at the grain boundary then the activation energy is approximately given by the sum of the energy difference and barrier height. Mainly in the case of poly-Si has assumed a grain depletion & grain

boundary trapping model to be responsible for barrier formation. The performance degradation of the device arises from the presence of high density of trapping states at the grain boundaries. Many techniques were applied to improve the poly silicon performance through grain size enlargement, reduction of the grain boundary and the intra grain defect densities [4].

In this paper we are going to discuss the effect of poly-Si inversion layer thickness (t_{Si}), trap state density (N_T) and grain size (L_g) on the activation energy. The theoretical calculated results show a reasonably good agreement with the experimental results.

2. THEORY

It is assumed that polycrystalline material is composed of linear chain of identical crystallites having a grain size (L_g). The electric conduction in polycrystalline silicon films is considered to be by way of trapping the free carriers at the trap states located at the grain boundaries thus forming a potential barrier. As a consequence, depletion regions are formed on both the sides of a grain boundary. To satisfy charge neutrality, this results in the bending of energy bands thus forming the barrier at the grain boundary [5].

Assuming one dimensional flow of charge carriers and thermionic emission to be the dominant current mechanism over a grain boundary, the current density may be expressed as [6],

$$J = q^2 n_0 (V_c / KT) V_d \exp[(E_G + \Psi_B - E_F)/KT], \quad (1)$$

where, n_0 is the concentration of free carriers in the grain, $V_c = (KT/2\pi m^*)^{1/2}$ is the collection velocity, m^* is the effective mass of the carrier, V_d is the voltage drop across the grain boundary, E_G is the band gap energy, E_F is the Fermi energy referred to the intrinsic Fermi level in the neutral region, Ψ_B is the barrier height.

In the case of high gate voltage when the grains are not fully depleted, the over all charge neutrality condition $Q_{sc} + Q_t = 0$ is used to calculate the grain boundary barrier height (Ψ_B). This means that the space charge density (Q_{sc}) in the depletion region of the grain is compensated by the trapped charge density (Q_t) at the grain boundary trap states. One dimensional Poisson's equation is,

$$\frac{d^2\Psi}{dx^2} = -\frac{1}{\epsilon_s} \rho_s \quad (2)$$

Employing the simple criterion that the charges in the inversion layer become significant when the electron concentration at the surface is equal to the substrate impurity concentration, the barrier height is easily obtained as

$$\Psi_B = \frac{KT}{q} \ln \frac{N_A}{n_i} \quad (3)$$

The intrinsic carrier concentration is, $n_i = N_A \exp(-q\Psi_B/KT)$. The applied voltage must be larger enough to create this depletion charge and the surface potential. The threshold voltage required for strong inversion,

$$V_T = \sqrt{2q\epsilon_s N_A (2\Psi_B)} / C_{OX} + 2\Psi_B \quad (4)$$

Assuming the partially depleted grains the potential barrier height is given by [7],

$$\Psi_B = qN_T^2/8N\epsilon_s$$

Where, N_T is the trap state density and N is the gate induced electron concentration given by [8],

$$N = C_{OX}(V_G - V_T)/qt_{Si} \quad (5)$$

The grain boundary potential barrier (Ψ_B) is expressed as,

$$\Psi_B = q^2N_T^2t_{Si}/8\epsilon_sC_{OX}(V_G - V_T) \quad (6)$$

The dependence of barrier height (Ψ_B) on the grain size is predicted through the relationship [9],

$$N_T = [35 + 2.55 L_g^{-0.363}] \times 10^{10} \text{ per cm}^2$$

The potential barriers resulting from the trapping of charge carriers at the grain boundary, act to suppress current flowing through the channel. Because the barrier forms at the grain boundary the activation energy is given by [10],

$$E_a = \Psi_B - 0.5KT$$

Therefore by putting the value of, Ψ_B activation energy can be expressed as,

$$E_a = q^2N_T^2t_{Si}/8\epsilon_sC_{OX}(V_G - V_T) - 0.5 KT \quad (7)$$

For all purposes of numerication the second term appears to be negligible.

3. RESULT & CONCLUSION

The activation energy is calculated for (i) different values of grain size (L_g) from 50 nm to 500nm (ii) different values of trap state density (N_T) from $11.8 \times 10^{16}/\text{m}^2$ to $5.33 \times 10^{16} / \text{m}^2$ (iii) different value of inversion layer thickness (t_{Si}) from 10 nm to 50 nm. The parameters taken for calculation are $C_{OX} = 160 \mu\text{F}/\text{m}^2$, $K = 1.38 \times 10^{-23} \text{ J/K}$, $T = 300 \text{ K}$.

Figure 1 a & b show the variation of activation energy (E_a) with the gate voltage for different values of L_g , N_T and t_{Si} . Comparison between the theoretical predicted results and experimental results shows a reasonably good agreement [7]. The activation energy is seen to decrease with the increase in gate voltage for all values grain size, trap state density, inversion layer thickness. It is clear from the graph that the activation energy decreases as the gate bias increases and it is larger for smaller grain size and vice-versa, and from another graph the activation energy decreases as the gate bias increases and it is larger for larger value of inversion layer thickness.

This may be due to the fact that when t_{Si} is increased the area of poly-Si film will decrease which reduces the area for conduction, so that a higher channel resistance is expected which results in high activation energy. If the grain size is small then there will be more grain boundary present so, the trap state density will be more, results in trapping state that reduce the number of carriers and create space-charge regions in the crystallites [11, 12].

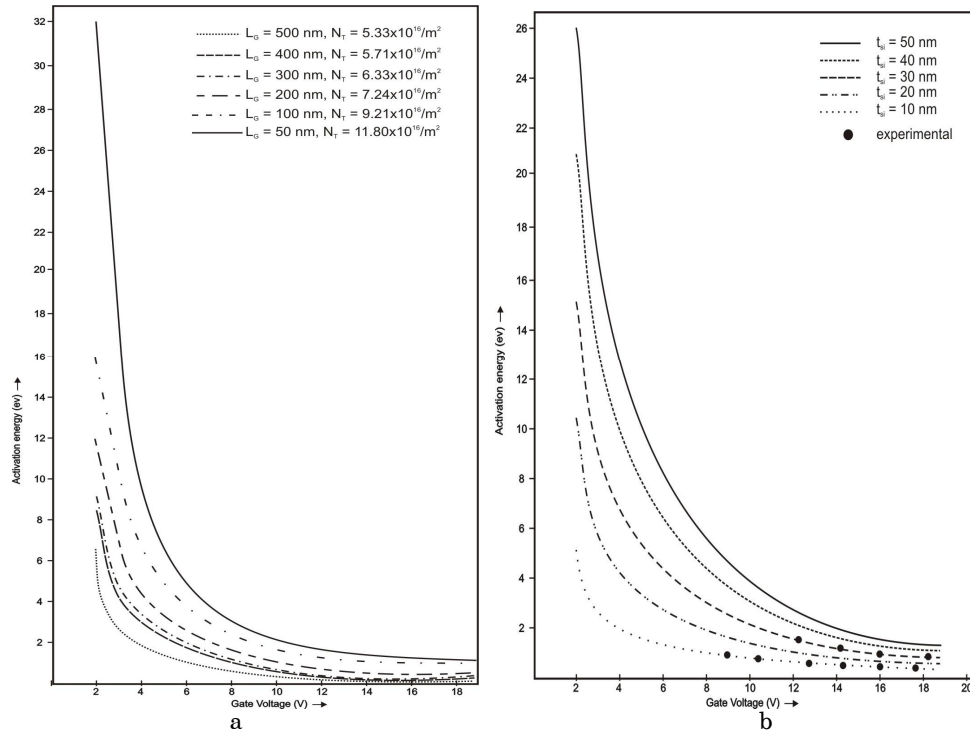


Fig. 1 - Variation of activation energy with gate voltage for different values of trap state density layer thickness (a) and variation of activation with gate voltage for different values of inversion (b)

So, it is difficult for a carrier to move within the channel hence results in high value of activation energy.

REFERENCES

1. P.T. Chow, M. Wong *IEEE T. Electron. Dev.* **56**, 1493 (2009).
2. F.T. Chien, C.N. Liao, C. M.Fang, Y.T. Tsai, *IEEE T. Electron. Dev.* **56**, 441 (2009).
3. M. Wong, T. Chow, C.C. Wong, D. Zhang, *IEEE T. Electron. Dev.* **55**, 2148 (2008).
4. F.V. Farmakis, J. Birni, C.A. Dimitriadis, *IEEE T. Electron. Dev.* **48**, 83 (2001).
5. J. Levinson, F.R. Shepherd, M. Rider, *J. Appl. Phys.* **53**, 1193 (1982).
6. G. Baccarani, B. Ricco, *J. Appl. Phys* **49**, 5565 (1978).
7. N. Gupta, B.P. Tyagi, *Int. J. Mod. Phys. B* **19**, 791 (2005).
8. A.T. Hatzopoulos, C.A. Dimitriadis, *IEEE T. Electron. Dev.* **52**, 1727 (2005).
9. B.P. Tyagi, K. Sen, *Int. J. Electron.* **58**, 83 (1985).
10. N.C.C Lu, L. Gerzberg, J.D. Meindl, *IEEE T. Electron. Dev.* **28**, 818 (1981).
11. B.G. Streetman, S. Banerjee *Solid State Electronic Devices* (Prentice Hall: 2000).
12. S.M. Sze, *Semiconductor Devices Physics and Technology* (New York: Wiley, 1985).