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## SCHOTTKY CONTACT OF GALLIUM ON P-TYPE SILICON

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*The evolution of barrier at Schottky contact and its stabilization to value characterized by the barrier height and unambiguous measurement is still being curiously perused as they hold the key control and manufacture of tailor made Schottky devices for a host of existing and potential for future applications in electronics, optoelectronics and microwave devices. In this context, gallium – silicon Schottky diode has been fabricated and analyzed.*

***Keywords:*** *SCHOTTKY CONTACT, THIN FILM, INTERFACIAL STRAIN, BARRIER HEIGHT, FLAT BAND BARRIER HEIGHT, IDEALITY FACTOR.*

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## 1. INTRODUCTION

The knowledge of physics for barrier formation in a metal-semiconductor Schottky contact is still incomplete. It is well known that the ultimate barrier development across such system is a result of simultaneous process of band line-up and accompanying charge transfer across the interface [1, 2]. In Schottky contact, charge transfer may have contributed from (a) properties of contacting materials metal and semiconductor (b) interface states and metal induced gap states (MIGS) (c) defects, impurities and chemical mismatch at the interface (d) Crystallography, epitaxy and relative orientation and coordinates of atoms at the interface etc.

Physical understanding about the evolution of Schottky barriers at metal-semiconductor (M-S) interfaces centered around describing the source and the mode of charge transport across the interface required for establishing equilibrium across the interfaces by band realignment. The earliest model in this regard, given by Schottky [3] and Mott [4]. This predicted Schottky barriers $\phi_{bp}$ at M-S interfaces with p type semiconductors as,

$$\phi_{bp} = E_g - (\phi_m - \chi_s) \quad (1)$$

where $\chi_s$ is the electron affinity of the semiconductor, $E_g$ is the semiconductor band gap. However, experimental results did not correspond to the predictions of above equations e.g. linear dependence of barrier heights with the choice of the metal work function on a chosen semiconductor. In order to resolve this situation, Bardeen [5] proposed that presence of intrinsic surface states within the band gap and their occupancy should be taken into consideration since situation within the bulk and at the surface of the semiconductor cannot be

assumed to be the same. As a result, the Fermi level of the semiconductor is not free to move for realignment on interface formation as it would be when there were no allowed energy levels in the energy gap as in the bulk. Therefore, the Fermi energy level can be pinned by surface states and may not be free to vary for interface formation by different metals. Although Bardeen's proposition provided a way out of this impasse, it did not indicate how to quantitatively estimate and control the contribution of surface states for barrier height, which will now depend on local electronic structure also. Later on, Cowely and Sze [6] attempted to describe the Schottky barrier variation by synthesizing the linear work function model of Mott and Schottky with Bardeen's interface state model. Such an attempt was based on the proposition that density of states is independent of energy within the band gap and the charge in them depends on the position of the Fermi level with respect to the charge neutrality level. To resolve the above impasses was later criticized by Heine [7] and others, and they propounded the concept of metal induced gap states at the interface. Later on, the role of both extrinsic and intrinsic defects of the interface was highlighted by Spicer [8]. However, many of the observations regarding metallization of semiconductor surfaces could be related to above MIGS and defect models, strong exceptions to these were also experimentally observed [9].

In this context, liquid metal Schottky contacts have not been exploited much, only some reports are found on them in literature Hg-Si [2, 10-18] and Ga-Si [18-25] systems. However, if liquid metals are used to fabricate Schottky interfaces, structural and morphological changes of the above kind and the possibility of chemical reaction within the interface zone can be easily avoided. Moreover, the exposure time of the semiconductor, substrate to the ambient can be minimized to avoid its possible contamination and the liquid metal over layer will always be metallic in character and will spread almost uniformly over the selected area. At the same time, the metallic over layer will be only weakly bonded to the semiconductor substrate. Thus, liquid metal semiconductor Schottky interfaces provide an interesting alternative route to examine more closely the physical aspect about the evolution of Schottky barriers e.g. factors contributing and dominating the exchange of changes at the interface for band line up. With this view point, the present paper describes chemical stability of gallium with p-type silicon to give rectifying Schottky barriers.

## 2. EXPERIMENTAL

In this investigation p-type Si ⟨100⟩ crystals having acceptor density of around $10^{16}$ / $cm^3$ were used. The ohmic back contact on the rough surface of the silicon crystal was made of aluminium by depositing 0.15 μm thick film of pure aluminum by thermal evaporation in a vacuum of around $10^{-6}$ torr. The other polished surface of the crystal was etched in 1:3:5 $HNO_3$ : HF : $CH_3COOH$ around 30 seconds when brown vapors appeared and then it was dipped for a minute in dilute solution of 1:9 HF:$H_2O$. The crystal was then mounted in the sample holder below the capillary arrangement and pure gallium (99.99 %) was put into the capillary using a disposable syringe. The I-V data on the so formed Schottky diodes were obtained at 100 Hz and C-V data were obtained at 100 kHz using HP-LCR meter (Model – 4274 A).

## 3. RESULTS AND DISCUSSIONS

The representative nature of I-V characteristics of Ga-Si (p) diode after formation is shown in Fig. 1. From this figure, it can be observed that an I-V characteristic of the Schottky contact possesses good rectifying behavior. A representative $V_d$ - $I_d$ characterstics after correcting the measured I-V data for series and shunt resistance has been shown in Fig. 2.

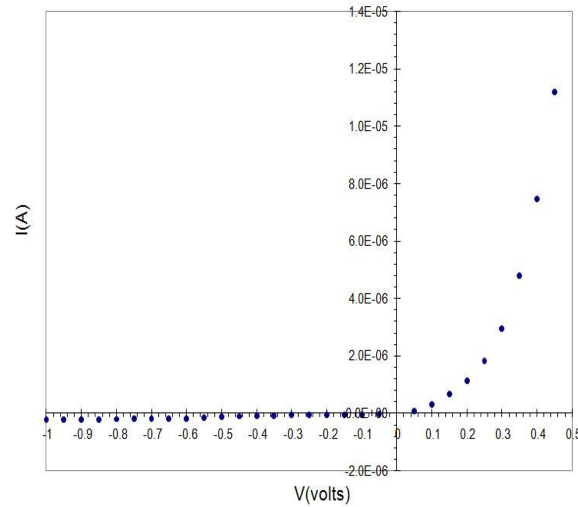


***Fig. 1*** *– A representative I-V characteristics of Ga-Si (p) Schottky diode*

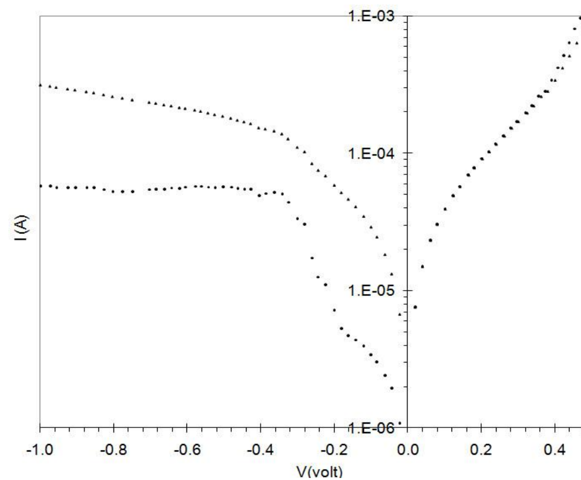


***Fig. 2*** *– A representative corrected ( • ) and uncorrected ( ▲ ) I-V characteristics of Ga-Si (p) Schottky diode*

In order to evaluate the characterizing parameters Ln $\{I/[1 - \exp(-qV/kT)]\}$ against $V$ plots, shown in Fig. 3, were used [26]. The flat band barrier height [26], known to be more fundamental in nature, and given as,

$$\phi_{bF} = n\phi_{b0} - (n - 1)(kT/q)\ \ln[N_V\ N_A] \quad (2)$$

Here, $N_V$ is the density of state in the valance band.

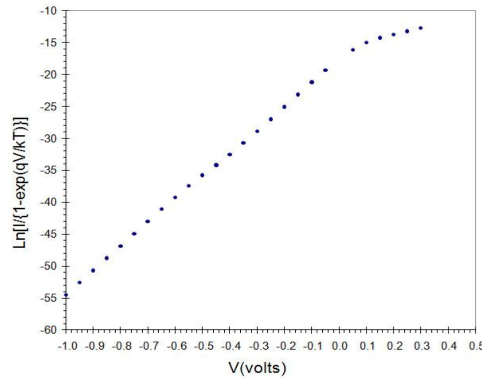


***Fig. 3*** *– A representative* Ln $\{I/[1-\exp(-qV/kT)]\}$*-V characteristics of Ga-Si(p) Schottky diode*

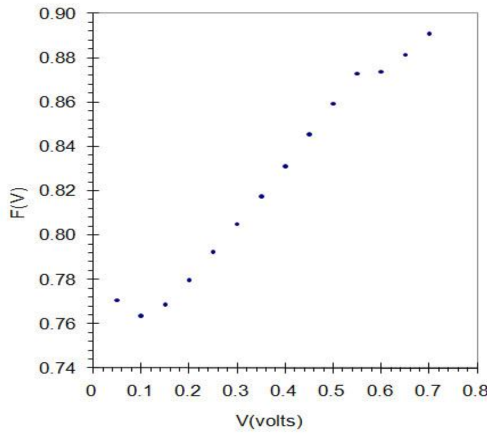


***Fig. 4*** *– A representative Norde plot of Ga-Si (p) Schottky diode*

The forward bias data were also analyzed by a Norde plot shown in Fig. 4 and barrier heights was also obtained after analysing C - V data at 100 kHz using $C^{-2}$ versus V plot given in Fig. 5 [26]. The values of ideality factors, zero bias barrier heights $\phi_{bo}$, flat band barrier heights $\phi_{bf,}$ barrier heights $\phi_b$ (Norde), barrier height as obtained by C-V measurements $\phi_b^{C\text{-}V}$ have been plotted as function of time in Fig. 6. It is obvious from Fig. 5 that apparent conclusions made about the stability of the behaviour of Ga-Si (p) Schottky diode looking on the nature of characteristics are confirmed.

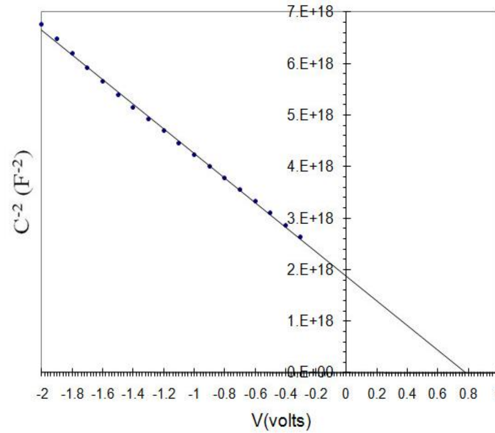


*Fig. 5* – *A representative $C^{-2}$ - Vcharacteristics of Ga-Si (p) Schottky diode*

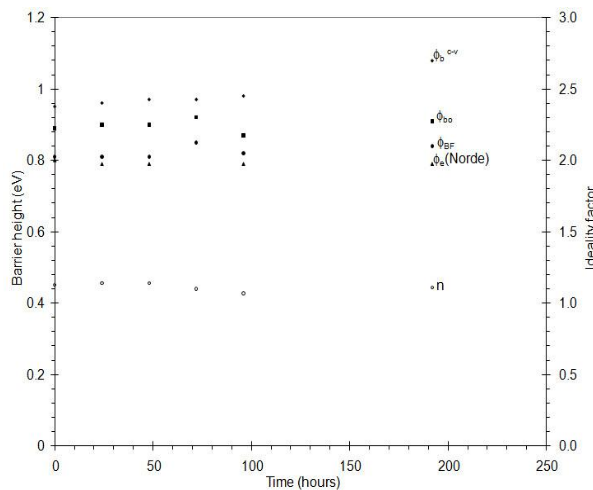


*Fig. 6* – *Variation of Barrier Height and Ideality factor with time of Ga-Si (p) Schottky diode*

The value of barrier heights as obtained on the analysis are given the values expected on Schottky, Bardeen, MIGS and unified defect model [9] in Table. 1. The obtained values of barrier heights of Ga-Si (p) Schottky diode is nearer to the theoretical value calculated by Schottky model than other models. Here, it may be relevant to recall that all models invoke exchange of charges across the interface for band alignment. However excepts Schottky model, such an exchange is proposed to be originating largely from within the interfacial zone, though the initial origin of such charges may be different in different models. Further, these models have been proposed to explain observed barrier heights in Schottky diodes formed by evaporation of solid metals and it has been found that barriers on chemically prepared surfaces are larger than Bardeen model. It is usually attributed to decoupling of metal and semiconductor due to presence of oxide layer. Thus, larger barrier heights, in case of liquid metal Schottky diodes may be arising

on account of the absence of strong bonding forces between liquid metal and the silicon. It has been observed by Monch [27] and Spicer et al. [8] that MIGS do not dominate until metallic of over layer develops.

***Table 1*** *– The theoretical and experimental values of barrier height* (*eV*) *for Ga-*(*p*) *Si* (100) *Schottky diode i.e. ideality factor, n* = 1.10

| Theoretical Values of Barrier Height (eV) | | | | Experimental Values of Barrier Height (eV) | | | |
|---|---|---|---|---|---|---|---|
| Schottky Model | Bardeen Model | Heine Model | Unified Defect Model | Zero bias barrier height $\phi_{bo}$(I-V) | $\phi_b$ (Norde) | Flat band barrier height $\phi_{bf}$ | From C-V measurement $\phi_b$(C-V) |
| 1.12 | 0.36 | 0.47 | 0.59 | 0.82 | 0.82 | 1.02 | 1.02 |

Further Nelson's [28] calculation shows that the step prior to development of delocalized state in the band gap is covalent bonding across the interface due to chemisorptions of adatoms formed by evaporation. Thus deviation and the movement of the observed barrier heights may be attributed to the absence of strong bonding between neighboring atoms. These will tend to make device regime liquid metal overlayer Schottky interface behavior more similar to the thin overlayer of evaporated solid metal Schottky interfaces. In solid phase of metal these interfacial bondings have been found to give rise to interface states which can affect Fermi level pinning at the interface and consequently the barrier heights to different values depending on number and kinds of such states. However, all these different values of barrier heights at low thickness of metallic over layers tend to merge into one value (pinned value) for higher thickness over layers, probably due to larger concentration of defects etc. When these bondings break on melting, the Fermi level pinning gets largely removed and consequently a higher value of barrier height can be expected after melting. i.e. values, which are nearer to Schottky limits. The flatband barrier height $\phi_{bf}$ a fundamental measure of Schottky barrier which eliminates the effects of image force lowering is calculated from I-V measurements. Here, we find the agreement between the flat band barrier $\phi_{bf}$ and the values of barrier height from capacitance measurement, which are more nearer to Schottky limits.

## 4. CONCLUSION

It can be concluded that the Ga-Si (p) Schottly diode show reproducible, repeatable and stability properties. Although gallium is to be non reactive with silicon [29]. Interfacial changes near the melting temperature is likely to give rise to building up or relaxation of bonds between gallium and silicon while silicon has cubic structure, gallium in the solid state has orthorhombic structure. Thus, interfacial strain can be expected to give rise to interface states and their additional creation may modify Fermi levels at the interface, interfacial band alignment and the barrier height. Therefore it can be concluded that the evolutionary aspects of Schottky diodes e.g. contribution of interfacial strain which are seen only at smaller thicknesses of metallic over layers in case of solid-solid contacts may be seen more clearly in case of solid-liquid contacts.

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