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STRATEGIC REVIEW OF ARSENIDE, PHOSPHIDE AND NITRIDE MOSFETS

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Metal oxide semiconductor field effect transistor used as an amplifier and switch uses Si primarily as a channel material for its very stable oxide SiO_2. *In-spite of many advantages there are some restrictions for* Si *MOS, so the world is approaching towards compound semiconductor for higher frequency and current. The development of compound semiconductor metal oxide semiconductor is also facing critical problems due to the lack of availability of proper gate oxide material. Research is being conducted on arsenide and phosphide metal oxide semiconductor field effect transistor. Nitride channel MOS are in focus due to their high band gap, high current and high temperature uses.*

Keywords: *REVIEW, ARSENIDE, PHOSPHIDE, NITRIDE, MOSFET, COMPARISON.*

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1. INTRODUCTION

In present days MOSFETs find their applications in digital circuits as well as in switching. Generally Si-MOS is used due to super quality of SiO_2 as a gate oxide material on silicon. But it has certain limitations like low mobility of electron in Si compared to GaAs due to which Si-MOS has a frequency limitation as well as drain current in case of Si MOS is also low. Thus, in order to remove these limitations we have to go for III-V compound semiconductor MOSFET. Basic research works on compound semiconductor had started as early as in 1960's but even after such a long time compound semiconductor MOSFETs are under-performing as compared to their price and performance. Main constrains for the compound semiconductor MOSFETs are leaky gate oxide with interface, trap charges and low breakdown. The intended properties of a MOS gate oxide are high resistivity, high breakdown field, low trap charge density, chemical stability, good interface property and little or no drift of charge through oxide layer. Different types of oxide like Al_2O_3, (Ga_2O_3, Gd_2O_3) GGO are used in different types of MOS. Work is in progress on three types of MOSFETs like Arsenide, Phosphide and Nitride channel MOSFET. This paper reviews the remarkable progress being made in the development of compound semiconductor MOSFET in the context of material device properties, device structures and DC performances.

2. III-V MOSFET

2.1 Arsenide MOSFET

First anodic-oxide arsenide MOS was reported in 1976 by B. Bayraktararoglu et al. [1]. It was GaAs MOS where Al_2O_3 was used as a gate oxide layer.

Metal layer of In-Sn-Al was exposed to electrolyte causing the growth of native oxide. Oxide layer thickness was found to be 1000 Å. Breakdown field for this MOS was reported as 10^7 V/cm and threshold voltage as 0.2 V [1]. But Al_2O_3 creates some trap at interface due to which Ga_2O_3 and Gd_2O_3 (GGO) [2,3,11] which is native oxide and having dielectric coefficient (k) 14.2, much higher than that of SiO_2 (3.9) [2] could also be considered as an option. Hafnium oxide which is another rare earth oxide proves itself as a good gate oxide material for compound semiconductor MOS [15, 16]. Due to high dielectric constant the breakdown voltage for this MOS will be higher and also leads to increase its current conducting capability. Trap charge density in GGO is also very low in the order of 2×10^{10} cm^{-2} eV^{-1} [3]. Passlack et al. reports this distribution of surface charge as U-shaped [25]. To deposit GGO on GaAs in MBE at first oxide on GaAs is deposited by heating followed by depositing the oxide using electron beam evaporation at a temperature of 350-550 °C. P-channel MOS with an oxide thickness of 400 Å, extrinsic transconductance was found as 0.3 mS/mm and breakdown field as 3.6×10^6 V/cm [2, 3]. In GGO (band gap 4.4 eV) the ratio of Ga_2O_3 and Gd_2O_3 is nearly constant (55:45) [3]. For GaAs depletion MOSFET transconductance was found as 210 ms/mm [3] and maximum frequency of oscillation as 36 GHz [3]. Introduction of Indium in GaAs results increase in mobility and higher saturation voltage. For $In_{0.53}Ga_{0.47}As$ MOS with GGO as gate oxide showed maximum oscillating frequency as 10 GHz. Reduction in the frequency might have been due to higher interface charge density (D_{it}). If GGO was grown on ultrahigh vacuum (< 10^{-9} Torr) then leakage current would have been as low as 10^{-9} A/cm^2 and breakdown voltage 10^7 V/cm [5]. If novel oxide GGO was grown on As free environment then interfacial state density would have been comparable with that of SiO_2 (10^{10} cm^{-2} eV^{-1}) [6]. To increase the high current density P.Parikh et al [4] reported Al_2O_3 as an oxide layer on GaAs. 200 Å epitaxial layer of $Al_{0.98}Ga_{0.02}As$ is oxidized with steam at 85 °C forming Al_2O_3 layer. Current level for this MOS was reported 330 mA/mm and breakdown voltage as 30V [4]. Transconductance (g_m)

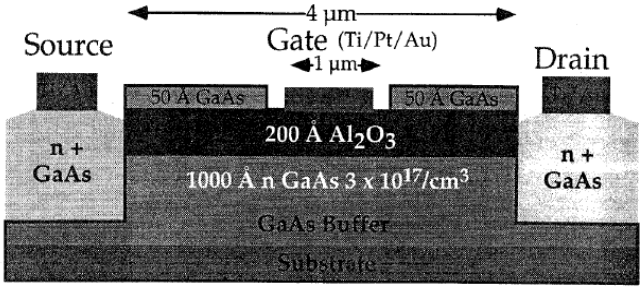


Fig. 1 *— Cross-section schematic of D-mode MOSFET (From Ref. 4)*

was 110 mS/mm where RF parameter i.e. maximum oscillating frequency was reported as 21 GHz [4]. J.Y.Wu et al introduce the concept of 'selective liquid phase oxide gate' [7] where GaAs is immersed into Ga-ion containing nitric acid solution to make a stable oxide which is composed by Ga_2O_3, As and As_2O_3. This liquid phase oxide gate MOS has breakdown voltage of 4.5×10^6 V/cm, leakage current as 10^{-8} A/cm^2. Reported value of the dielectric constant is low (3.1) [7]. The only advantage of this oxide layer is

that it is formed in room temperature. SiO_2 as a gate oxide layer on GaAs for a MOS reported higher density of interface state (10^{14} cm^{-2} eV^{-1}) [8]. Though low temperature LPD grown SiO_2 on GaAs, shows much lower interface state [9]. For InAlAs MOSFET where the oxide layer was formed by thermal oxidation of InAlAs (Al = 48 %) showed transconductance of 6 ms/mm for gate length of 8 μm [10]. Breakdown field for this type of oxide layer was found lower than that of MOS using Al_2O_3 as oxide layer [10]. $In_{0.2}Ga_{0.8}As$ channel p-type enhancement mode MOSFET [11] where AlGaAs layer acts as spacer layer and Ga_2O_3 as a gate oxide showed interface charge density of 3×10^{11} cm^{-2} eV^{-1}. With Si-delta doped region below the channel this MOS (Fig. 2) shows a good transconductance value of 51 mS/mm [11]. Be-doped n-type InGaAs n-channel MOS where GGO was used as a gate oxide material shows excellent c-v characteristics and surface

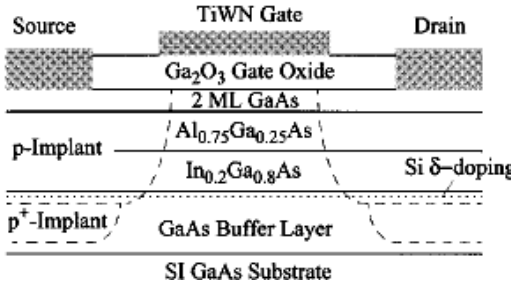
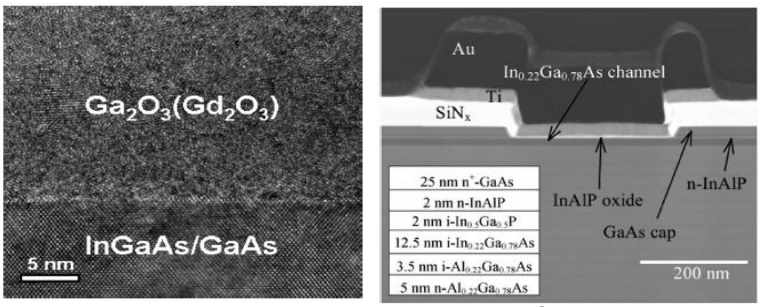


Fig. 2 *– Cross section view of self-alligned enhancement mode* InGaAs *MOSFET [11]*

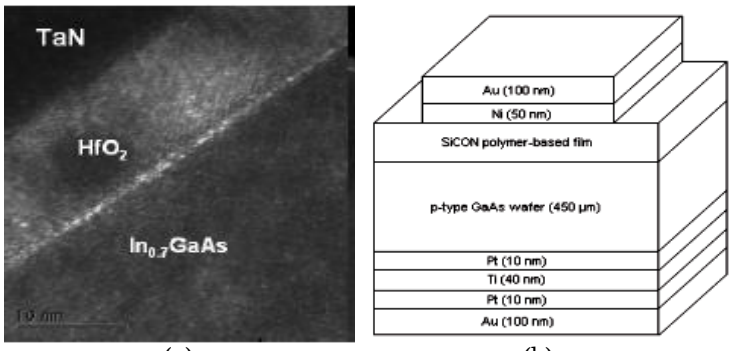
trap density was in the order of 10^{11} cm^{-2} eV^{-1} [12]. With gate length of 4 μm this device shows maximum drain current of 30 mA/mm and transconductance of 1.7 mS/mm [12]. Threshold voltage was found moderate (1.8 V) [12]. Very good surface state between InGaAs and GGO makes the surface charge density comparable with Si. TEM of the interface between InGaAs/GaAs and GGO is shown in Fig. 3(a). Drain current and transconductance of $In_{0.2}Ga_{0.8}As$ channel can be increased by growing a layer of Al_2O_3 on GGO gate oxide layer [13]. This device gave a transconductance value of 48 mS/mm and maximum drain current value of 135 mA/mm [13]. Metal gate last shows large traps at oxide-semiconductor interface compared to metal gate first process due to higher chance of contamination in first case [13]. To achieve higher current and low threshold voltage form $In_{0.22}Ga_{0.78}As$-channel MOS native oxide of InAlP is currently taken as a gate oxide material [14]. The cross section of the MOS is shown in Fig. 3(b). Top most InAlP layer is oxidized with steam at a temperature of 440 °C for 9.5 minute to grow a oxide of thickness 3.5 nm. Low threshold voltage (0.25V) was found for this MOS [14]. For gate length of 0.25 μm transconductance was found as 245 ms/mm and saturation drain current as 165 mA/mm. RF characteristics of this type of MOS are also found very promising. The reported value of maximum oscillation frequency for this MOSFET was 80 GHz [14]. TEM image of the interface of $HfO_2/P_xN_y/In0.{}_{70}Ga_{0.47}As$ is shown in Fig. 4a. Recently In rich $In_{0.57}Ga0_{.47}As$ receives considerable attention as increasing In amount increases mobility of electron in the channel. For n-channel $In_{0.57}Ga_{0.47}As$ MOS with Al_2O_3 as gate oxide repots maximum drain current of 200 mA/mm [17].



(a) (b)

Fig. 3 *– HR-TEM of GGO and* InGaAs/GaAs *interface (a) [12] and cross section of InGaAs channel enhancement MOS with native oxide of* InAlP *(b) [14]*

Here gate is fabricated at first which increases contamination at the oxide semiconductor interface [17]. InGaAs (In = 57 %) channel E-mode MOSFET where Al_2O_3 was grown by ALD as a gate oxide reports much higher drain current (360 mA/mm) [18]. Possible reason for this high current might be the formation of gate at last; as a result it suffers less from contamination at the oxide semiconductor interface. Threshold voltage for these MOS was found as 0.25 V and surface charge density as 1.4×10^{12} cm^{-2}eV^{-1} by HF-LF method [18]. At the same time ZrO_2 grown on InGaAs had surface charge density of 10^{13} cm^{-2}eV^{-1} [20]. Plasma based PH_3 passivation technique is one of the best way to passivate the open surface. H.J. Ho et al. reported a technique to passivate InGaAs of a n-MOSFET [19]. After plasma-PH_3 treatment using MOCVD, HfO_2 and HfAlO were deposited. Plasma-PH3 passivation improves the thermal stability between oxide-semiconductor interface upto 750 °C [19]. Metal contact was given by TiN. Interface between plasma-PH3 treated InGaAs-HfO_2-TiN is shown in the Fig. 4b. Transconductance



(a) (b)

Fig. 4 *– TEM of interface of-* $HfO_2/P_xN_y/In_{0.70}Ga_{0.47}As$ S/D *formed at* 700 °C *[14] (a) and GaAs MOS capacitor with* SiCON *polymer layer as gate dielectric [22] (b)*

for this MOS was reported high (378 mS/mm at V_d = 1 V) and the effective mobility of electron was found as 2557 cm^2/V s [19], which was higher than that of enhancement mode MOSFET [18]. ZrO_2 as gate oxide material on InGaAs grown on p-type InAlAs shows interface charge density in the range of 10^{13} cm^{-2} eV^{-1} [20]. CVD grown polymer based thin film 'SiCON', grown on GaAs showed very good result [22]. Process of growing this polymer layer

is described in detail in Ref. 23, 24. This MOS (shown in Fig. 4b) reported density of interface charge as 9.7×10^9 cm^{-2}eV^{-1}[22]. Dielectric leakage current reported in the range of nA/cm^2 and breakdown field 2.05 MV/cm [22].

2.2 Phosphide MOSFET

InP due to its high electron mobility, has been used as a MOSFET channel material. Compared to GaAs, InP has higher saturation velocity which goes in favor of InP MOSFET. Thermal oxidization of InP produces oxide on it but it shows a departure from stoichiometry [26, 27] which causes degradation of properties at the interface of InP-oxide. Oxide grown on InP using plasma oxidation system is stable both thermally and chemically and does not react with organic solvents [26]. Though P_2O_5 has strong affinity to water but due to different chemical composition does not react even with boiling water [26]. No accumulation of phosphorous at the interface was reported [26]. This InP channel MOSFET showed channel conductance of

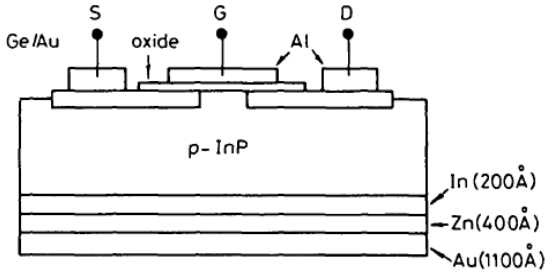
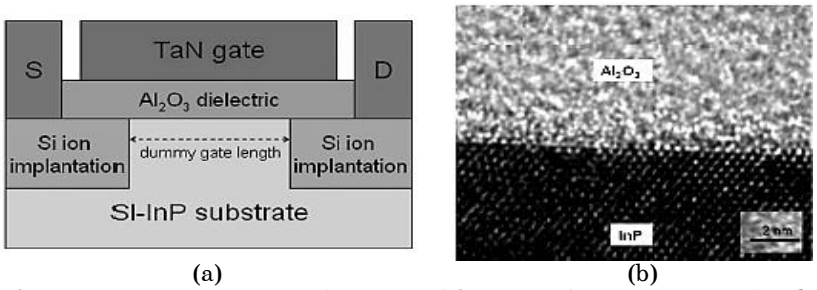


Fig. 5 *– Cross section view of self-alligned enhancement mode* InP *MOSFET [26]*

1.2 mA/V at $V_g = 13$ V [26]. Electron surface mobility at the interface was reported much lower (400 cm^2 V^{-1} S^{-1}) than the bulk mobility [26]. SiO_2 was also tried as a gate oxide for InP MOS [28,32]. Using plasma enhanced decomposition of tetraethoxysilane in oxygen plasma, a layer of SiO_2 was deposited at 300 °C [28]. Oxide layer quality was found to be dependent on deposition condition. Fe-doped InP MOS with SiO_2 as oxide showed electron surface mobility in between 250-750 cm^2 V^{-1} S^{-1} but X-ray study shows dislocation densities in the order of 10^4-10^5 cm^{-2} [28]. Kawakami et al. reported interface between InP and Al_2O_3 [29] and unpinned Fermi level [33]. Using anodic oxide as gate insulator promising surface charge density was observed. D_{it} of the order of 8×10^{10} cm^{-2}eV^{-1} was achieved in mid-band if the oxide was annealed at 200 °C [30]. Enhancement mode n-channel InP metal oxide semiconductor field effect transistor with ALD grown Al_2O_3 as gate oxide (30 nm) showed maximum drain current of 70 mA/mm for a gate length of 0.75 μm [33]. Gate oxide was grown at substrate temperature of 300 °C using $Al(CH_3)_3$ and water vapor at nitrogen environment [33]. Source and drain was done using ion-implantation of Si and then RTA at 720 °C for a period of 10 second. Leakage current for this MOS was reported as 10 μA/mm at maximum gate voltage of 8V [33]. Interface charge density was comparatively high and in the order of 10^{12} cm^{-2}eV^{-1}. Electron mobility at the interface was reported as 650 cm^2 V^{-1} S^{-1} and transconductance as 10mS/mm [33]. Inversion type InP MOS (Fig. 6a) with ALD grown

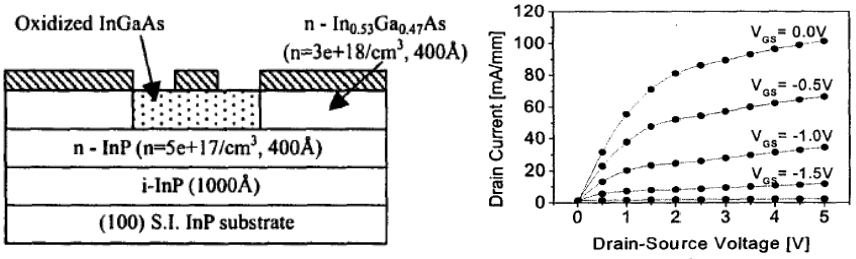
Al_2O_3 as oxide layer having effective oxide thickness of 21 Å shows improvement in transconductance [34]. Fig. 6b shows sharp interface between Al_2O_3 and InP without any sign of interfacial reaction. For this MOS possessing gate length of 50 μm, drain current was reported as 50mA/mm [34]. High electron mobility of 745 cm^2/V s was also reported at the interface [34]. Another way



(a) (b)

Fig. 6 *– Schematic cross-section of* InP *MOSFET (a) and TEM of* Al_2O_3-InP *interface (b) [34]*

to passivate InP-MOS is by using liquid phase oxidized InGaAs [35]. This oxide layer was formed by using a solution of Ga-ion contained nitric acid with oxygen plasma treatment. Peak transconductance of the depletion mode MOS (Fig. 7a) was found as 60 mS/mm [35]. In this case, normalized drain saturation current was reported as 78 mA/mm and maximum operation frequency (f_{Max}) as 70 GHz [35]. Drain current vs drain-source voltage curve for the device was shown in Fig. 7b. Maximum drain current drift from its saturation level was reported as 7.1% due to the interface trap charge [35].



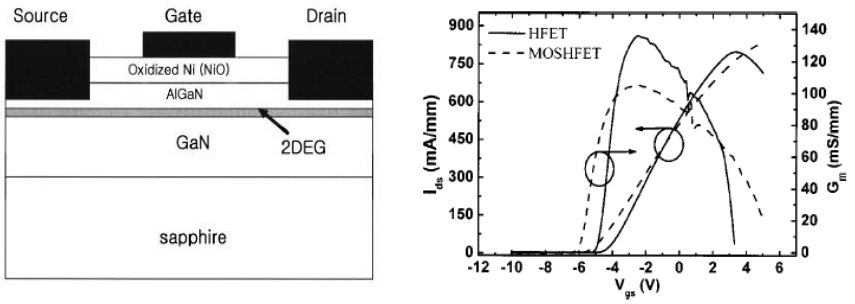
(a) (b)

Fig. 7 *– Schematic cross-section of InP MOSFET with InGaAs liquid oxide (a) and drain current-voltage characteristics InP channel MOSFET (b) [35]*

2.3 Nitrite MOSFET

Gallium Nitride is also being an important material choice for MOSFET researches. Although it has a lower mobility than GaAs and InP based III-V compound semiconductors, but it has other advantages like very high saturation current, high temperature stability, higher breakdown voltage due to its high bandgap. The inherent piezoelectric charge property makes the material a very good choice for high current, high voltage and high power devices. Gallium nitride is also experimented in different magnetic field conditions and found to be very reliable. So, GaN MOSFET can extensively be used for the space application purpose. In search of proper oxide for gate oxide, at first gallium oxide was tried. But both dry [39, 40]

and wet [41] oxidation shows improper interface of Ga_2O_3/GaN [38]. SiO_2 was also tested as a gate dielectric [46, 47, 49]. Then AlN was also tried but it was suffered from defects and grain boundaries [38]. Rear earth oxide HfO_2 has also been tried as gate dielectric [57,58,59,60]. Using SiO_2 as gate dielectric GaN MOSFET was formed in LP-MOCVD on sapphire substrate [49]. PECVD was used to grow an oxide layer of 10-15 nm. Reported values of maximum current and transcondutance were 300 mA/mm and 60 ms/mm respectively for a gate length of 2 μm [49]. Cut-off frequency and gate length product of this GaN MOS was reported as 11.6 GHz-micron which is comparable to the same value of AlGaN/GaN MOSFET grown on same substrate [49]. Crystalline gadolinium oxides (Gd_2O_3) have been investigated as a gate oxide material for GaN MOS. Deposition of Gd_2O_3 on GaN was done in MBE using Gd and oxygen plasma at a temperature of 650 °C [38]. Though crystalline structure of the oxide but it shows low breakdown field (0.5 MV/cm), which proves the presence of large no. of defects at the interface [38]. Thermal stability experiment at a temperature of 1000 °C showed less than 10% increase in RMS roughness of Gd_2O_3 interface [38]. If a layer of SiO_2 (300 Å) was deposited then it shows very low leakage current in the order of pA [38]. Leakage current in the order of 10-11 A was reported for wet oxidized nitride MOS [55]. Among all these tests for the search of gate oxide, amorphous GGO proves itself better in almost all the way [42, 43, 44, 45]. GGO layer was deposited by electron beam evaporation from a single crystal GGO in MBE [38]. GGO/GaN MOS showed leakage current in the order of mA to nA [38]. Dielectric constant of GGO is found very high (14). GGO/GaN allows modulation at forward voltage of 3 V, where as SiO_2 layer added Gd_2O_3/GaN MOS shows the value as 7V [38]. High temperature silicon-di-oxide (HTO, 900°C) deposited GaN MOS showed interface trap density as 3×10^{11} $cm^{-2}eV^{-1}$ near the conduction band edge [46]. Gate leakage current for this RESURF (Reduced SURface Field) GaN MOS was reported very low and in order of pA, where as field electron mobility reported as 110 cm^2/Vs [46]. High doping in GaN may cause degradation of mobility in the channel as a result AlGaN/GaN heterostructure is being used to generate 2DEG. AlGaN/GaN heretostructure MOS with SiO_2 as oxide layer repots mobility of 1180 cm^2/ Vs [37]. Sheet carrier concentration at the interface was found as 1.15×10^{13} cm^{-3} and maximum drain current as 600 mA/mm [37]. Gate oxide for this MOS was fabricated by PECVD. Gate leakage current found four times lower than that of AlGaN/GaN HEMT [37]. Maximum transconductance for this MOS was reported as 75 mS/mm [37]. AlGaN/GaN heterostructure MOSFET with nickel oxide as dielectric is reported by C.S. Oh et al. [48]. NiO as dielectric has band-gap energy of 4 eV and dielectric constant of 11.9. Ni oxidation was performed in air ambient at 300°C to 600°C for 5 minutes [48]. Ohmic contact was done by thermal deposition of Ti/Al/Ni/Au. Maximum drain current of the AlGaN/GaN MOS (Fig. 8a) was reported as 800 mA [48]. At high gate voltage the device showed negative resistance (Fig. 8b) due to self-heating but pinch-off was observed for gate voltage about − 5.9 V [48]. Maximum value of g_m value of AlGaN/GaN MOS was reported as 105 ms/mm [48]. In 2006, D. Alexandrov et al. reported a strange type of GaN/InN MOSFET which can behave both n and p-channel MOS. While making the MOS, GaN layer is grown on InN layer where at the interface a layer of $In_xGa_{1-x}N$ is formed which can act as an exciton layer [50]. This layer can behave as a source of both electron and



(a) (b)

Fig. 8 *– Schematic cross-section of* AlGaN/GaN *MOSFET (a) and* I_d *vs* V_{gs} *curve for AlGaN/GaN HFET and MOSFET (b) [48]*

hole depending upon the applied voltage to the heterojunction. If positive voltage with respect is applied to the gate then exciton layer act as a source of electron and generated electrons moves to the higher band gap material i.e. GaN in this case. So GaN/InN MOSFET will become n-channel for positive gate voltage. For negative gate voltage $In_xGa_{1-x}N$ layer breaks and acts a source of holes, making the MOS as p-channel [50]. SiO_2 was used as gate oxide material for the MOS [50]. GaN MOS with SiO_2-Ga_2O_3 as oxide dielectric reports low leakage current in the order of pA [51]. To grow the oxide layer of Ga_2O_3 on GaN, oxidization was done with the help of nitric acid (pH 3.5) with He-Cd laser [51]. Then a layer of SiO_2 was grown. Forward and reverse breakdown fields were found as 2.92 and 11.5 MV/cm respectively, where as leakage currents were 91 and 10 pA [51]. Interface state density was stated as 2×10^{11} cm^{-2}eV^{-1} [51]. Use of GaN as a channel material increases the breakdown voltage which is dependent on the doping of GaN layer. K.Tang et al. [52] shows this phenomenon in their E-mode MOS which has also the advantage of 2DEG at AlGaN/GaN interface. This hybrid MOS-HEMT was built on p-GaN by growing unintentionally doped GaN/AlGaN layer (Fig. 9) [52]. Gate oxide thickness was 100 nm. A reported value of 2DEG at AlGaN/GaN interface was 8×10^{12} cm^{-3} [52]. Maximum breakdown voltage for this hybrid MOS was 1300V, which depends on the doping concentration in the p-GaN layer [52]. With increasing doping in lower GaN region the breakdown voltage for this MOSFET was found reducing [52].

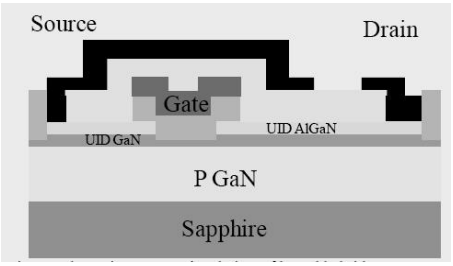
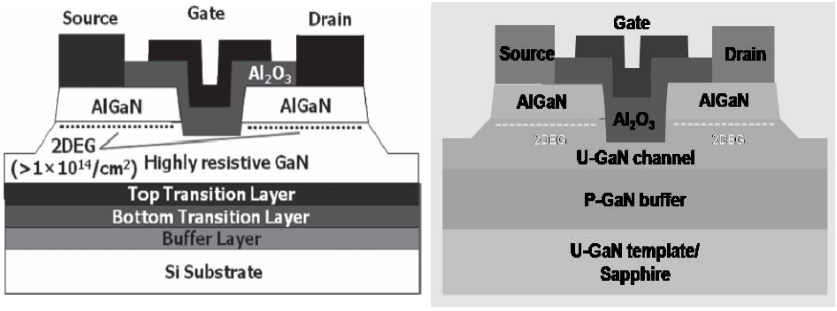


Fig. 9 *– Schematic cross-section of hybrid MOS-HEMT [52]*

By using special technique GaN can be grown on silicon. AlGaN/GaN MOSFET grown on Si was described by K-S. Im et al. [54]. The device was grown on silicon by growing multiple transition layers on them. Bottom

transition layer was made by five stacks of low temperature grown AlN (20 nm) and high temperature grown GaN (150 nm). Upper transition layer was made up of multiple stacks of AlN/GaN superlattice [54]. Upon this a high resistive GaN layer of thickness 0.7 μm and $Al_{0.3}Ga_{0.7}N$ layer (25 nm) was grown. After etching $Al_{0.3}Ga_{0.7}N$ in the gate region 30 nm thick high qualities Al_2O_3 layer was grown using ALD. Source and drains are made up of Ta/Ti/Al/Ni/Au using electron beam evaporator [54]. Reported value of 2DEG at the AlGaN/GaN interface is very high and in the order of $10^{14}cm^{-2}$. This high value is due to the strong tensile stress in the growth of AlGaN/GaN which increases both types of polarizations. This density of 2DEG is greater than that for normal AlGaN/GaN heterostructure. Mobility of 2DEG was found as 120 cm^2/ v s from Hall measurement. Due to higher value of 2DEG drain current was also high (353mA/mm) [54]. Maximum transconductance for this MOS was reported as 98 mS/mm whereas gate leackage current was in the order of 10^{-7} A/mm at gate voltage of 6 V [54]. Field effect mobility for this case was reported as 225 cm^2/V s (highest reported mobility in GaN MOSFET) [54]. For this normally off GaN MOS off-state breakdown voltage was reported as 40 V with a gate length of 0.25 μm [54]. AlGaN/GaN MOSFET grown on sapphire [53] with p-GaN buffer layer showed less promise compared to the previous case [54].



(a) *(b)*

Fig. 10 *– Schematic cross-section of GaN MOSFET grown on Si-substrate [54] (a) and schematic cross section of MOSFET grown on sapphire [53] (b)*

For this normally-off MOSFET (fig. 10b) maximum drain current was reported as 109 mA/mm at $V_g = 7$ V and extribsic transconductance in the order of 30 ms/mm [53]. Sheet carrier (2DEG) density for this was reported in the order of 10^{12} cm^{-2} [53], two order lower than that reported for AlGaN/GaN MOS grown on Si [54]. With increasing channel thickness, density of 2DEG increases due to lower effect of p-GaN buffer on the 2DEG at interface of AlGaN/GaN [53]. H. Kambayashi et al. recently reports AlGaN/GaN hybrid MOS-HFET with maximum drain current of 100 A for a channel length of 2 μm [56].

3. COMPARISON

Arsenide MOSFET is the one subject of maximum interest among researcher in the domain of field effect technology. From Table 1 it is clear that GaAs MOS with GGO as gate oxide material has performed well. From GaAs, MOS technology is shifting towards InGaAs to achieve higher breakdown and

transconductance but at the same time lower threshold voltage and leakage current. Table 2 shows the development of arsenide MOS and their performances improving year after year. For phosphide MOS cost is higher and performance is inferior as compared to Arsenide MOS. So less number of research has been done on phosphide MOS. One of the main disadvantage of this type of device is higher leakage current instead of higher electron mobility in phosphide metal oxide semiconductor field effect transistor. Among all types of MOS technology nitride channel is the new one and most discussed. For nitride MOS breakdown voltage is higher compared with other MOS, so this MOS can be used as to make low frequency high power devices. Nitride MOS with Al_2O_3 as oxide layer shows higher leakage current due to the presence of leaky oxide at the interface. Instead of using only gallium nitride if we use AlGaN/GaN heterostructure then 2DEG formed at the interface that can supply lots of carrier without decreasing the electron mobility caused by high doping. Further Drain current increases This type of device is called as hybrid MOS-HEMT structure as both the advantage of HEMT and MOSFET are available there. GGO as gate oxide reports lowest interface charge density for nitride technology. Nitride MOS with NiO as gate dielectric reports highest drain current.

Table 1 *– Comparison of Arsenide MOSFET*

Year [Ref]	MOSFET	Oxide material	D_{it} $cm^{-2}eV^{-1}$	Breakdown field (V/cm)	Saturated drain current mA/mm	g_m mS/mm	Reverse-Leakage current	V_{Th} V
1996 [2]	E-mode P-channel GaAs	GGO	-	3.6×10^6	-	0.3	-	-
1997 [3]	D-Mode n-channel GaAs	GGO	-	3.6×10^6	-	-	-	-
1998 [4]	D-Mode n-channel GaAs	Al_2O_3	-	-	330	30	50 μA	-
2001 [7]	D-mode n-channel GaAS	Ga_2O_3, As, As_2O_3	5×10^{11}	4.5×10^6	380	80	10 nA	-
2002 [11]	E-mode p-channel GaAs	Ga_2O_3	3×10^{11}	-	0.55	51	-	-0.93
2007 [18]	E-mode n-channel InGaAs	Al_2O_3	1.4×10^{12}	-	360	-	-	0.25
2008 [12]	Inversion-mode n-channel GaAs	GGO	$2\text{-}6\times10^{11}$	-	30	1.7	1-10 nA/cm^2	1.8
2009 [13]	D-mode n-channel InGaAs/GaAs	Al_2O_3/ GGO	10^{11}	-	135	48	-	-
2010 [14]	E-mode InGaAs	Native oxide of InAlP	5×10^{12}	14.7×10^6	165	168	5.5 nA	0.25

Table 2 – *Comparison of Nitride MOSFET*

Year	MOSFET	Gate-Oxide material	Transconductance (mS/mm)	Reverse Leackage Current	Surface Mobility (Cm^2/ V s)	Ref. No.
1998	D-mode GaN	GGO	5	-	-	35
2000	GaN	Gd_2O_3, SiO_2	15	10 μA^{-1} nA	-	38
2002	GaN	SiO_2	60	-	-	49
2003	GaN MOS on AlGaN	SiO_2	-	50 pA	110	46
2003	GaN	SiO_2-Ga_2O_3	-	10 pA	350	51
2010	AlGaN/GaN MOS on Si	Al_2O_3	98	0.1 μA	225	54
2010	AlGaN/GaN MOS on p-GaN	Al_2O_3	30	4 μA	850	53

4. CONCLUSION

In this paper we have studied the properties of different types of MOS in terms of their structure, characteristics and performance. Further arsenide, phosphide and nitride MOS were compared for electrical performances on the basis of some common parameters like threshold voltage, D_{it}, transconductance, gate oxide materials etc. Nitride Hybrid MOS was found to be the most useful transistor for making high power devices. The year wise studies of different III-V MOSFETs demonstrate that various electrical parameters are rapidly transforming into better situations.

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