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Fabrication of Low-Roughness Au/Ti/ SiO_2/Si Substrates for Nanopatterning of 16-Mercapto Hexadecanoic Acid (MHA) by Dip-Pen-Nanolithography

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Silicon based low-roughness Au/Ti/SiO_2/Si substrates were fabricated using standard IC fabrication processes. Evolution of surface roughness during substrate fabrication process was studied. Fabrication process steps, namely, thermal oxidation and e-beam evaporation for ultra-thin Ti(~ 5 nm)/Au(22 nm) films, were optimized to result in surface r.m.s roughness ~ 0.2 m and ~ 1.0 nm, after thermal oxidation and Ti/Au deposition steps respectively. Surface roughness was estimated by atomic force microscope (AFM) imaging and image analysis. Nano-patterning experiments using thiol based 16-MHA molecular-ink on fabricated substrates were carried out, under controlled environment conditions, by dip-pen-nanolithography (DPN) technique. Minimum line-width ~ 60 nm and circular dots radius ~ 175 nm were patterned.

Keywords: Atomic force microscopy, Dip-pen-nanolithography, Nanopatterning, Self-assembled-monolayers.

PACS numbers: 81.16.Nd, 68.35.Ct

1. INTRODUCTION

There has been a continuous quest for fabricating smaller devices & circuits during last four decades following famous Moore's law. Journey from few microns to sub-100 nm gate-length has been possible due to innovations in manufacturing equipments, materials, processes, device-structures and circuit architectures. Lithography, along with other process parameters, determines feature size and hence the components density on the chip. There are various techniques for patterning nanoscale feature sizes for ever shrinking CMOS devices and circuits [1]-[6]. AFM based Dip-Pen-Nanolithography (DPN) is relatively new technique developed by Mirkin's group [7], and is fast becoming a powerful tool to generate nano-scale features of variety of materials on compatible substrates. The generated patterns are basically self-assembled-monolayers (SAM) of desired molecules on substrate surface. In brief, DPN is a direct writing technique utilizing ultra sharp AFM cantilevered tip. Molecules, of the material to be patterned, are coated on the AFM tip. The molecules coated AFM tip scannes the substrate surface in close proximity. Due to ambient humidity a water meniscus is formed between tip and the substrate surface. As tip scannes the substrate surface, ink molecules diffuse through the meniscus to the substrate. The basic system consists of an atomic force microscope (AFM) stage, controlled environment chamber, controller and software for controlling AFM operation, writing process, imaging, data acquisition etc. Direct writing of viruses, protein nano-arrays is also possible with DPN technique. The transported ink-molecules are adsorbed on avaiable sites forming a nano-patterned SAM. The patterning process is very sensitive to environmental conditions (i.e. humidity and temperature), surface conditions, and tip coating procedures [8]. Substrate surface is crucially important for self-assembly process. Surface roughness influences both, the ink-molecules transport as well as AFM imaging contrast [9]. Various ink-substrate combinations have been explored for writing nano-pattern using dip-pen-nanolithography (DPN) [7]. Thiol based 16-Mercapto Hexadecanoic Acid (16-MHA) is a much researched molecular-ink compatible to gold surface. Recently, we reported nano-scale patterning of silicon nanoparticles on SiO_2/Silicon substrate by DPN technique [10].

There are various techniques for depositing ultra-thin films of Ti and Au, such as sputtering, thermal evaporation, e-beam and more recent pulsed laser deposition (PLD) [11]. For nano-patterning, it is very important to have flat substrate surface with low-roughness and without any contamination. For developing silicon based nano-electronic devices, substrate should be compatible with IC fabrication processes. During device fabrication, substrate (normally, silicon wafer) goes through many cycles of thermal, deposition, patterning, chemical etching processes. So, it is compelling to study the evolution of surface roughness as wafer goes through the process steps and also to develop processes which result in low surface roughness. In the present study, Ti/Au thin film was taken up as compatible gold surface to 16-MHA ink. Surface roughness has contributions from chemical cleaning, oxidation and metal deposition processes. Silicon dioxide was grown on silicon substrates by high temperature thermal oxidation, and Ti and Au were deposited by e-beam evaporation to result low surface roughness at final stage. Experimental environment conditions were maintained in an enclosed chamber. On the fabricated substrates, experiments of AFM tip-inking, ink-calibration, and then nano-writing of lines and circular dots were carried out. Written patterns were imaged and analyzed.

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2. EXPERIMENTAL

One-side polished 2" silicon wafers, n-type, ⟨100⟩, 0.01-0.02 Ohm cm, were diced into quarter pieces. These silicon quarter pieces were used in the experiments. After thorough chemical cleaning, surface of starting silicon substrate were imaged by AFM (Nanoscope II, Digital Instruments) in contact mode. The obtained AFM images were analyzed in the system software to estimate r.m.s. roughness of the substrate surface. To study the effect of oxidation process on surface roughness, these wafers were oxidized at two temperature 900 °C and 1000 °C in dry/wet/dry oxygen ambient to result in ~90 nm thick oxide layer. Again, AFM imaging was carried out and roughness was estimated of the oxide surface. For preparing substrate compatible to thiol based 16-MHA ink, titanium and gold deposition runs were carried to get desired deposition rates and thickness. Ti (5 nm)/Au (22 nm) were deposited by optimized electron beam evaporation process parameters; Ti – pressure $\sim 2 \times 10^{-7}$ Torr, beam current ~ 20 mA, and Au – pressure 2-8×10^{-7} Torr, beam current ~ 30 mA. After gold deposition, again, surface roughness was measured through AFM imaging. These substrates were kept under vacuum to avoid surface contamination.

Nano-patterning experiments were carried out using DPN NSCRIPTOR system from M/s Nanoink, USA. Suitable environmental conditions i.e. temperature and relative humidity were controlled and maintained in the controlled environment chamber. DPN AFM stage is enclosed in this chamber. This chamber is placed on vibration isolation table. Commercial ink, 16-MHA in acetonitrile solvent was used for writing. Nano-patterning was performed in controlled humidity, 30-55 % and temperature, 25-35 °C. Triangular shape AFM tip was coated with 16-MHA ink using dipping method and dried. System operation was controlled through InkCAD software. Inking and ink-calibration were performed prior to each writing experiment. After ink calibration, lines and circular dots were designed in the design template using InkCAD. The designed patterns were then written using coated tips mounted in the AFM scanner. The written patterns were imaged with the same system in lateral-force-microscopy (LFM) Mode. The obtained results are presented in next section.

3. RESULTS AND DISCUSSIONS

The AFM image of surface of starting silicon sample is shown in Fig. 1a, the front surface of sample was polished and smooth, and the estimated r.m.s. roughness was 0.23 nm. As shown in Figure 1b, after thermal oxidation at 900 °C, the surface became slightly rougher with r.m.s. roughness ~ 0.31 nm. Roughness were estimated over the window size of 500 × 500 nm. Fig. 2a shows AFM image of silicon sample after oxidation at 1000 °C, and the roughness of the surface was estimated to be 0.21 nm. During oxidation process, initially, silicon surface goes through roughening phase due to uneven oxidation rates at localized non-uniformities at the SiO_2/Si interface. As oxidation proceeds, surface starts getting smoother. This may happen due to viscous flow of oxide at higher temperature followed by stress relaxation, and due to increased oxidation rates at the protrusions during the diffusion-limited oxidation phase. It was observed that the interface became rougher after initial phase of smoothening. The reasons for such observations are not clear [12]. Oxidation at 1000 °C was expected to result in smoother surface compared to the oxidation at 900 °C, because of improved viscous flow of oxide.

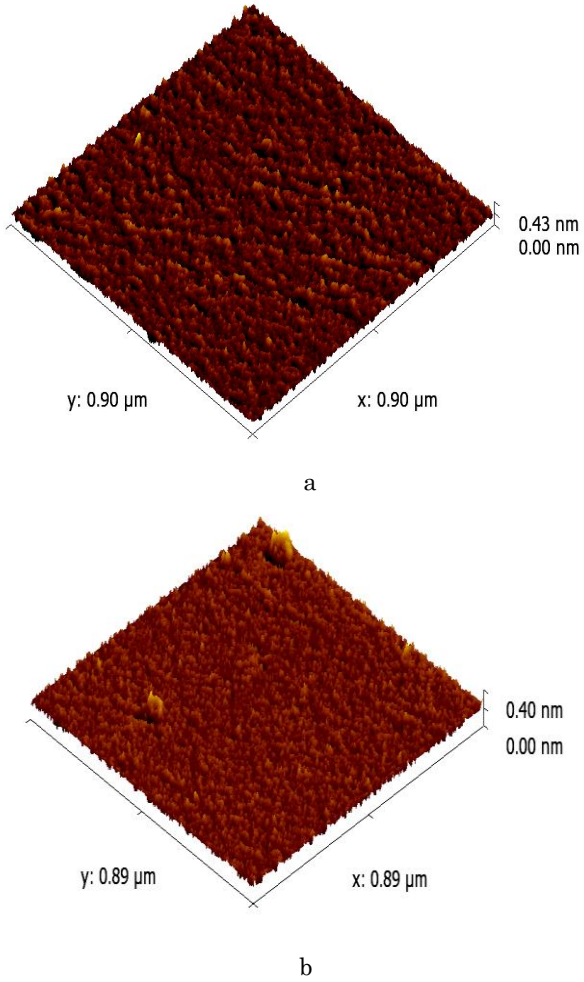

Fig. 1 – AFM images of surface of starting cleaned silicon wafer (a), and after 90nm thermal oxide grown at 900 °C (b). The estimated surface r.m.s. roughness are 0.23 and 0.31 nm respectively, window size was 500 × 500 nm

In our experiments, roughness decreased slightly from 0.31 nm to 0.21 nm with increasing the oxidation temperature from 900 °C to 1000 °C for same oxide thickness of 90 nm. Higher peak-to-peak surface roughness has been observed for wet oxidation at a temperature of 850 °C [13].

Fig. 2b shows AFM image of substrate after Ti (5 nm) and Au (22 nm) deposition by e-beam evaporation. Titanium was deposited to improve adhesion of gold film to the silicon dioxide layer. The estimated roughness at this stage was 0.99 nm. Very flat gold surfaces were obtained by evaporation of gold on mica and silicon wafer followed by glue bonding and transfer on glass substrate [14]. For semiconductor device fabrication, good adhering gold films on silicon substrate are required.

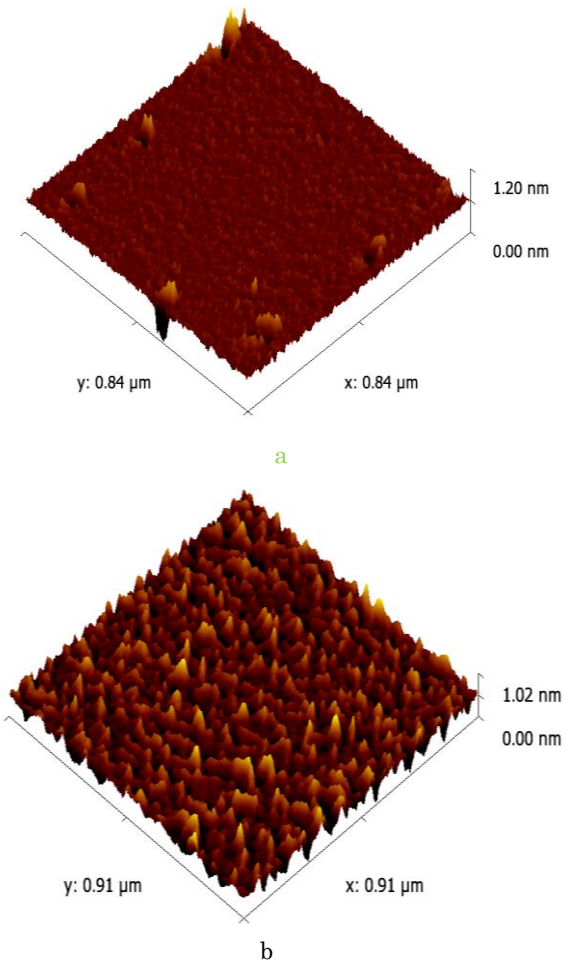

Fig. 2 – AFM images of surfaces of silicon wafer after 90nm thermal oxide grown at 900 °C (a), and after Ti (5 nm)/Au (22 nm) deposition by optimized e-beam evaporation process (b). The estimated surface r.m.s. roughness are 0.21 and 0.99 nm respectively, window size was 500 × 500 nm

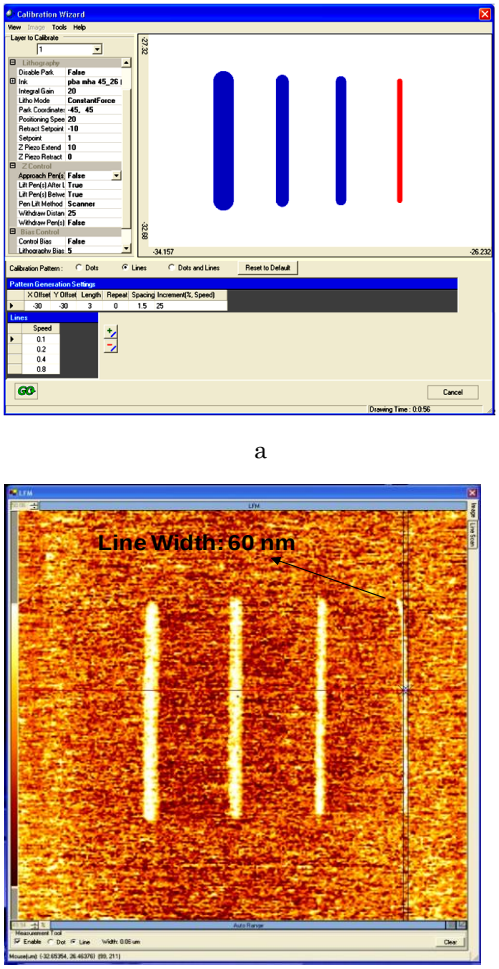

Fig. 3 – Snapshot of design template for nanowriting process for lines with different writing speeds **(0.1-0.8 μm/sec) (a), AFM images of 16 MHA lines written on gold surface using desgined process parameters (b)**

Thermal annealing of gold films further improves the surface flatness. High temperature annealing step can not be carried out at this stage because gold/titanium films are to chemically etched after nano-writing. So, efforts are needed to develop compatible processes to give even flatter gold surfaces on silicon substrates.

Now we present results on nano-patterning. Figure 3a shows window of design template in InkCAD software. Experiments were designed to write lines with varying speeds (0.1 – 0.8 μm/sec). Fig. 3b shows LFM image of lines written with above speeds at R.H. = 40 % and temperature = 25 °C. Minimum width of 60 nm was been achieved at the highest speed of 0.8 μm/sec. It is evidenced that line-width decreased with increasing writing speed. It is due to the fact that at higher tip movement speed, ink-molecules diffusing per unit time through water meniscus are less compared with lower writing speed. These fewer ink-molecules self-assemble on the gold surface resulting in smaller width. It is important to note that even the finest line was continuous. To further reduce the line-width, speed should be increased. But very high writing speeds, may result in broken lines, as molecules may not diffuse and arrive as fast as the tip moves. So, there has to be a trade off between writing speed and width of continuous line, keeping other process parameters same.

Fig. 4 shows LFM images of dots written on fabricated substrate at temperature = 32 °C and relative humidity = 54 %. The dwell time of tip, i.e. time during which tip was stationary at certain location, was varied from 1, 2, 4, 8, 12, 20 seconds. The dots appeared to be circular with little waviness at the periphery. As shown in figure, the dots were marked and encircled, and the area of the circle enclosing the dot was estimated by the system software. Dot radius was calculated from area of circles. The marked dot, written with dwell time of 1 second, has minimum radius of 175 nm. As can be seen, dot size increased with increasing dwell time of the tip. This may be explained as follows, longer dwell times allow more numbers of ink-molecules to diffuse and self-assemble on the surface. Dot size may further be reduced by controlling the number of ink-molecules flowing through water meniscus. This may be achieved by reducing the meniscus width through control of relative humidity. Another way may be by further reducing the dwell time.

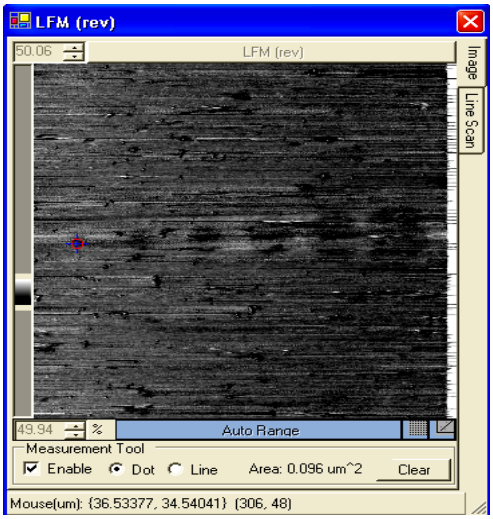

Fig. 4 – LFM images of 16-MHA "Dots" generated with different dwell time of tip (L-R); 1, 2, 4, 8, 12, and 20 seconds at R.H. = 54 %, temp. = 32 C, minimum radius is 175 nm

Smoother boundaries of lines and dots are expected on surfaces with further lower-roughness and with less number of grain boundaries, as grain boundaries facilitate uncontrolled diffusion of ink-molecules. Ideally speaking, large grains (preferably single grains), achievable in peeled gold films from mica-sheet/silicon wafer are best suitable for nano-scale SAM patterning [14]. But, for actual device applications, silicon/GaAs/Alumina based substrates are required. So, much R & D efforts are needed to develop large area substrates for DPN nanolithography and its integration with IC fabrication process.

4. CONCLUSIONS

Surface roughness evolution during substrate fabrication for DPN nano-writing was studied. Surface roughness at starting silicon wafer stage, after thermal oxidation, and after Ti/Au ultra-thin films deposition by e-beam evaporation process, were studied through AFM imaging and analysis. Based on roughness analysis, Au/Ti/SiO_2/Si substrates with roughness r.m.s. value~1.0 nm were fabricated suitable for nano-patterning. Nano-writing was carried out using 16-MHA by DPN technique. Under optimized process conditions, minimum line-width = 60 nm and "dot" radius = 175 nm were patterned. The achieved results are useful for nano-scale device fabrication, as substrate fabrication is critical for nanolithography. Moreover, the developed process is compatible with IC manufacturing technology. However, much is to be done on integration of DPN process with other device fabrication processes before real nanotechnology-enabled nano-electronic/ molecular devices are developed for ever demanding IT sector and pressing health-care needs.

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