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Analytical Modeling of SON MOSFET and Realization Inverter Circuit for High Speed and Ultra Dense Low Power Circuits

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In the recent years, there has been considerable interest in the realization of high speed, small-size and low-power consuming devices and systems. As a consequence, the search for new principle of operation of the small-size, high speed and low-power device is becoming more and more important. In our earlier paper, it has been established that SON technology, not only improve the dc performance with reduce a short-channel effect and threshold voltage, it also improves the frequency response due to improvement in conductance and reduced parasitic effect. Further, it is already in our knowledge that SCEs are suppressed in dual material gate MOSFETs because of the perceivable step in the surface-potential profile, which screens the drain potential. The concept of dual material gate has been applied to SON MOSFETs structure and the features exhibited by resulting new SON structure has been examined for the first time by developing an analytical model and the result agree well with the MEDICI simulation values. In order to substantiate the merits of the proposed SON MOSFETs, a MOS Inverter is realized using the SON MOSFETs and its performance is investigated as an aid to the high-speed, ultra-dense and low-power circuit related work.

Keywords: SON, SOI, Dual Material Gate, MEDICI, Inverter, Short Channel Effects.

PACS numbers: 84.30. – r, 85.30.De, 85.40.Bh, 85.40.Qx,

1. INTRODUCTION

Continuous progress in semiconductor technology has enabled the relentless evolution of electronics, information technology and communication [1-3]. It is evident that power consumption, leakage issues, scalability and noise immunity will be the bench mark for future devices in VLSI circuit design. Since the speed of MOSFET is intrinsically limited by the carrier transit time, the most obvious approach to improve the device speed is to reduce the gate length [4-6]. When the gate length is aggressively scaled, the gate begins to lose control over the channel and the parasitic condition results in saturation, possibly in a reduction of transconductance and in an increase of drain conductance [7-10]. It has already been established that under sub 100 nm regime, conventional MOSFET scaling concepts will be confronted with physical limitations-the lattice constant of Si. The major problems of scaling down the conventional MOSFETs include: (a) quantum mechanical tunnelling through the thin gate oxide, from source to drain and from drain to body; (b) threshold voltage control induced by random doping effects; (c) short channel effects (SCE) and mobility degradation; and (d) process control of thin layer uniformity and accurate lithography and implantation. In order to extend the lifetime of the Si-based CMOS technology, devices with new structures and/or new materials need to be considered [11-15]. Several performance boosters have been proposed in the literature and the International Technology Roadmap for Semiconductor (ITRS) suggest that one or more technology boosters may be required for devices beyond the 45 nm technology node in order to sustain the increase of intrinsic device speed [16]. Continuous down scaling of bulk MOSFET produces strong short channel effects and consequently a high leakage current which limits farther miniaturization of MOSFET [17-20]. Major issue with future MOSFET is how to handle different short-channel effects [21-25]. New device structures like thin-body fully depleted Silicon-On-Insulator (SOI) and recently developed Silicon-On-Nothing (SON) MOSFET, offer advantages over the conventional transistors. In a SOI or SON MOSFET, SCEs are influenced by thin-film thickness, thin-film doping density, substrate biasing, buried oxide thickness, processing technology and material used as gate oxide layer or as BOX layer. SON is found to be more resistive against different short channel effects, more specially Drain Induced Barrier Lowering (DIBL) and two dimensional charge sharing effect modifies threshold voltage of device with small channel length. In long channel devices, gate can be considered to be completely responsible for depleting the channel, whereas in every short channel devices, a significant portion of the depletion region charge under the gate is actually due to drain and source junction depletion rather than the bulk depletion induced by the gate and this effect is known as two-dimensional charge sharing effect. Use of different dielectric materials as GOX or BOX layer, modifies the coupling effect of the lateral field and vertical field at different regions of the device and modifies its performance and which initiates the advantages of SON over SOI structure. In this paper, we have assumed our previously developed analytical models [RF] together with the dual material gate concept to realize a typical CMOS inverter circuits with SON MOSFETs and its performance is studied analytically and compared with result associated with CMOS and SOI based inverters. Power dissipation, propagation delay, dc characteristics, frequency response, are investigated. This type of combined analytical and simulation approach allows us to predicts the technology road map for future ultra-dense, low-power nano-electronics devices and their efficiency in RF frequency range.

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2. MODEL

Currently there is no well-established analytical model for SON MOSFET. Hence, an analytical model is developed [5, 7] by us to estimate the essential parameters (like surface potential, electrical field, threshold voltage, DIBL etc) for SON MOSFETs they are then used to realize a inverter circuit as an aid to digital circuit related work. We tried to evaluated power dissipation, propagation delay, frequency response of SON based inverter to establish SON's superiority over SOI MOSFET's. A more realistic generalized three-interface compact capacitance threshold voltage model of SON MOSFET is developed and relevant analytical expressions are derived [4, 5, 7]. The current voltage model is developed using the derived expression and the basic charge control analysis incorporating necessary short-channel phenomena. Analytical model is developed for SON MOSFET with an intention for using it in digital circuits to get low power VLSI chips. Analysis is limited here on SON based NOT gate (inverter) [Fig. 1] only to have a feeling of the effects of the changes of the device dimension on the power consumption, circuit speed and different threshold voltage modifying short channel phenomena like junction-induced 2D-effects.We have investigated the effect of device parameters on surface potential, threshold voltage, on and off current, sub-threshold slope and DIBL expression.The SON-MOSFET technology is found to offer devices with further scalability and enhanced performance in terms of threshold voltage roll-off, sub-threshold slope and greater current derivability thereby providing scope for further miniaturization of devices [4, 5, 7] and much better performance improvement [26]. SOI/SON-MOSFET layered structure and its equivalent capacitive model are depicted in Fig. 2 and Fig. 3, respectively [5]. In the present work, we have adopted the SON's analytical model of our previous work [7] and extended SON's merits in a digital circuit realization. The various expressions for SON-MOSFET adopted in our present analysis are presented here for individual SON and in performance analysis we have incorporated combination of both the SONs.

2.1 Equivalent Capacitive Model

A layered structure of a SON MOSFET is shown in Fig. 2. The structure considered here has poly silicon (n+) gate. Let t_{GOX}, t_{Si}, $t_{BOX/air}$ and t_{sub} be the thickness of gate oxide, silicon channel layer, BOX layer and substrate layer respectively. L is the effective channel length of the device.

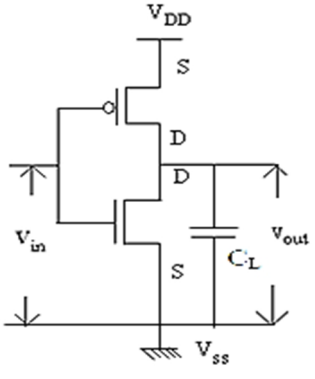

Fig. 1 – Circuit of SON based inverter

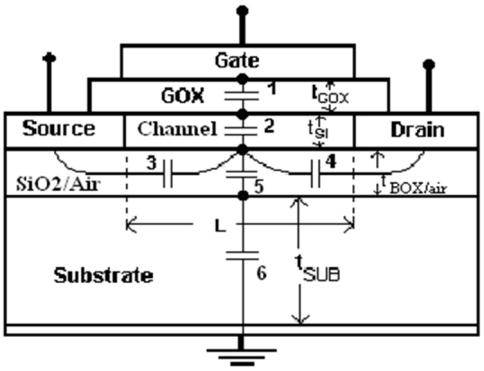

Fig. 2 – SOI/SON-MOSFET layered structure

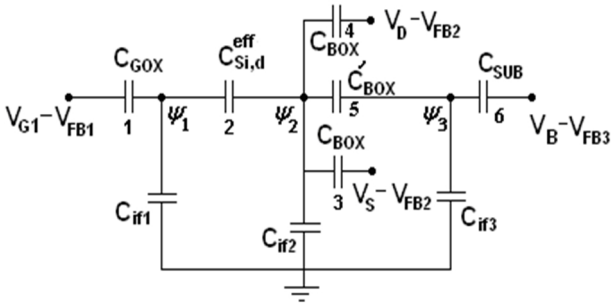

Fig. 3 – Equivalent capacitance model

In Fig. 3 C_{GOX} is the gate oxide capacitance, C'_{BOX} is the capacitance due to substrate bias and C_{BOX} is the capacitance due to fringing field, $C_{if(1,2,3)}$ are the interface state capacitances for three interfaces, $C^{eff}_{Si,d}$ is the silicon channel depletion capacitance. V_{FB1} is the flat band voltage at the front interface of the channel due to gate; V_{FB2} is the flat band voltage at the channel back interface due to source/drain and V_{FB3} is the flat band voltage at the back interface of the channel due to substrate.

2.2 Fringing Field Effect

Till now, two dimensional potential profile in BL region is quite complex to determine but capacitive model could be a possible solution to that problem [4]. Lateral field penetration from source and drain in the BOX in a fully depleted SOI/SON MOSFET is responsible for a dramatic increase of short-channel effects [30]. The coupling between channel back interface potential and the source or drain potential through burred layer can be represented by two capacitor (C_{BOX}) [7]. Both the capacitor have identical values for low V_{DS} with horizontally symmetrical potential distribution in BL around the channel center and they can be expressed as [28].

$$C_{BOX(Drain-Channel)}(z) = \frac{K_{BOX/air}}{t_{BOX/air}\left[\exp\left(\frac{\pi}{t_{BOX/air}}\left(z+\frac{L_{eff}}{2}\right)\right)-1\right]}$$

and

$$C_{BOX(Drain-Channel)}(z) = \frac{K_{air}}{t_{BOX/air}\left[\exp\left(\frac{\pi}{t_{BOX/air}}\left(z-\frac{L_{eff}}{2}\right)\right)-1\right]}$$

2.3 Channel Lateral Field Effect

Channel effect lateral field effect due to high drain biased induced field in a short channel device can be incorporated in the threshold voltage model through a well known technique "voltage dropping transformation(VDT)" [29]. According to VDT, the effects of lateral field in the channel initiated by source and drain junctions are equivalent to a reduction in the effective channel doping [30]. Using VDT for modeling short channel effects (DIBL), the effective channel doping is given by [31]

$$N_A^* = N_A - \frac{2\varepsilon_{Si} V_{DS}^*}{qL_{eff}^2},$$

where V_{DS}^* is an effective voltage given by

$$V_{DS}^* = V_{DS} + 2\left(V_{bi} + \Psi_2 - \Psi_1\right) + \\ +2\sqrt{\left(V_{bi} + \Psi_2 - \Psi_1\right)\left(V_{DS} + V_{bi} + \Psi_2 - \Psi_1\right)}$$

Here V_{DS} is the drain-source voltage, $V_{bi} = \left(k_B T/q\right)\ln\left(N_A N_D/n_i^2\right)$ is the built in potential, k_B is Boltzman constant, Ψ_2 is the bottom potential of the channel area and N_A is the silicon impurity doping concentration. Appling voltage doping transformation, the effective channel depletion layer capacitance is given as [4]

$$C_{Si,d}^{eff} = \frac{dQ_d}{d\Psi} = \frac{qN_A^* t_{Si} L_{eff}}{\Psi_{S1} - \Psi_{S2}}$$

Here Q_d is the total charge per unit area of silicon channel.

In a short channel device, threshold voltage is a function of drain bias or channel potential. $V(x)$ threshold voltage expression can be written as

$$V_{th} = V_{FB1} + H\left[1 + \frac{2C_{BOX}\left\{\frac{C - FV(x)}{G}\right\}}{C_{GOX}\left\{\frac{C - FV(x)}{G} + 2C_{BOX}\right\}}\right] - \\ \left(V(x) - 2V_{FB2}\right)\frac{\left\{\frac{C - FV(x)}{G}\right\}C_{BOX}}{C_{GOX}\left\{\frac{FV(x)}{G} + 2C_{BOX}\right\}}$$

$$I_{on} = WC_{G(eff)}(V_{DD} - V_t)\upsilon_s,$$

$$I_{off} = I_0\, 10 - (V_{n(low)} - \Delta V_{n(DIBL)}).$$

where I_{on} = "on state current". I_{off} = "off state current". $V_{t(low)}$ is average current velocity at low V_{DS} and $\Delta V_{n(DIBL)}$ is V_t reduction.

Subs threshold slope:

$$S \cong (600mV)1 + \frac{\varepsilon_{si}(1-x)G_{ex}}{\varepsilon_{ox}} \cdot \frac{t_{ox}}{td},$$

where

$$t_d = Depletion\ width = \sqrt{\left(2\varepsilon_{si}\frac{\psi_s}{eN_{si}}\right)}$$

$$DIBL \cong \frac{3t_d t_{ox} V_{ds}}{Leff\, 2\left(1 + \frac{\varepsilon_{si}}{\varepsilon_{ox}}\frac{t_{ox}}{t_d}\right)},$$

V_s = average current velocity near the source, "W" is the width, ε_{ox} and t_{ox} are gate oxide permittivity and thickness, respectively. All the symbols have the usual significance as [5].

2.4 Propagation delay

In our analysis, we will calculate the propagation delay of an Inverter. Looking at the high-to-low transition for V_{out} for the inverter, we follow the trajectory of the nMOS current-voltage transistor characteristic.

The load capacitance C_L consists of two major components.

1. The *total gate capacitance* C_G that is the gate capacitance of the transistors being driven by the inverter.

2. A *parasitic capacitance* C_P that results from the drain diffusions of the driving inverter and the wiring to the gates being driven.

We add the values of C_G and C_P to obtain the total load capacitance C_L. Substituting $C_G + C_P$ for C_L, we find the value of t_{PHL} to be and t_{PLH} also [32]

$$t_{PHL} = \frac{(C_G + C_P)V_{OH}/2}{k_n/2(V_{DD} - V_{Tn})^2}, \quad t_{PLH} = \frac{(C_G + C_P)V_{OH}/2}{k_p/2(V_{DD} - V_{Tp})^2}$$

The average propagation delay t_P can be estimated by averaging the transition times as shown in

$$t_p = (t_{PHL} + t_{PLH})/2.$$

2.5 Power dissipation

In an Inverter, power dissipation has three component: like Dynamic power dissipation, short circuit power dissipation and static power dissipation (leakage and sub-threshold leakage). When the inverter is in either of its stable state (ON or OFF) there is only static power dissipation which is contributes less than 20 % of the total power dissipation of the inverter [33]. The dynamic power dissipation (which is the most significant contributor of power dissipation) occur during change of state (OFF to ON or ON to OFF). The short circuit power dissipation is not directly related to Inverter, rather it occurs due to non ideal input or output signal with finite noise and fall times [32]. Hence we have incorporated in our calculation dynamic and static dissipation only and ignored the short circuit power dissipation [34-36].

Where Dynamic power dissipation:

$$P_{dn} = \frac{1}{T}\left[\int_0^{T/2} V_{out}\left(-C_{LOAD}\frac{dV_{out}}{dt}\right)dt + \right. \\ \left. + \int_{T/2}^{T}\left(V_{dd} - V_{out}\right)\left(C_{LOAD}\frac{dV_{out}}{dt}\right)dt\right].$$

Static power or leakage power:

$$p_{lkg} = V_{dd}k_B \exp\left[\frac{(V_{gs} - V_t)q}{nk_B T}\right]\left[1 - \exp\left(\frac{V_{ds}q}{k_B T}\right)\right].$$

3. RESULT AND DISCUSSION

To study the advantages of SON device in a SOI and CMOS logic circuit, SON based inverter circuit is studied by developing the analytical model of SON device. In the present work , the effectiveness of dual material gate has been applied to the SON MOSFET structure and the features shown by the proposed structure have been examined by the first time developing a 2D analytical model and it is exhibited that the result obtained form the proposed model agree well with the MEDICI simulation results. It also emphasized that the proposed structure leads to reduced SCEs, as the surface potential profile shows a step at the interface of the two metal which reduced drain conductance are DIBL. The power consumption of SON based inverter is found to be 5.26 % lower than SOI based inverter and 34.08 % lower than COMS inverter. the signal transmission time is 5.27 % lesser than SOI based inverter and 34.20 % less than CMOS. Load capacitance is the least for SON based inverter among the three similar inverter circuits.

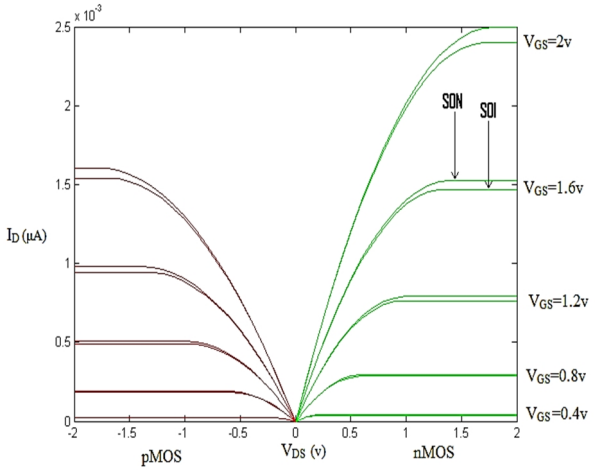

Fig. 4 – I_D-V_{DS} Curve for the inverter

Fig. 4 represents the I_D-V_{DS} characteristics of SON MOSFETs based on ours calculations and SOI MOSFETs at room temperature for a gate voltage range 0 to 2 volt. A significant drain current enhancement in SON MOSFETs is observed compared to bulk MOSFETs is observed which affects the circuit efficiency in CMOS logic techniques.

The switching Characteristics for a SON bassed inverter (Fig. 1) are depicted in Fig. 5. It appears that SON based inverter is faster than CMOS inverter and SOI inverter.

Fig. 6 shows the variation of power dissipation with frequency of the input signal. It appears that the power dissipation is lower for SON based inverter compared to CMOS inverter and SOI inverter. In order to establish the performance supremacy of the present SON based inverter a Table 1 is provided depicting various parameters. Typical parameters used for such performance comparison are: $W = 1$ micro meter, $L_z = 120$ nano meter, $C_{gox} = 44.45$ aF.

Similarly a Bar chart is also given in Fig. 7 to visualize the performance variation of difficult devices and inverter based on those devices.

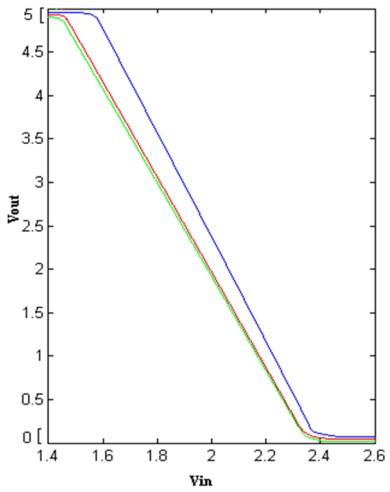

Fig. 5 – Simulates the switching characteristics for the SON-based inverter

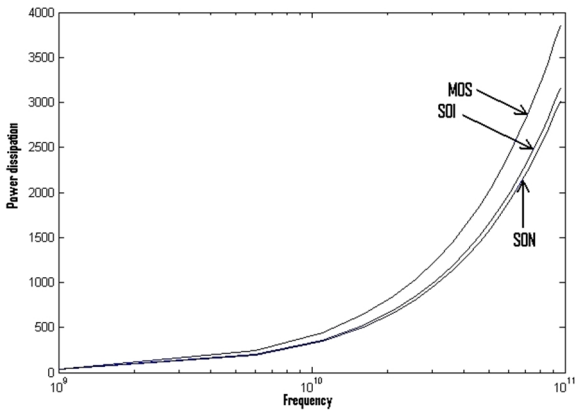

Fig. 6 – Frequency response of inverters

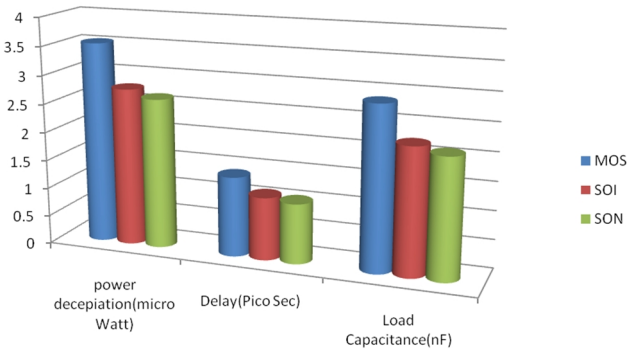

Fig. 7 – Bar chart showing power dissipation and Propagation Delay for Various types of inverter

Table 1 – Calculated /simulated parameters for inverter with different device structure scheme

Device	Threshold Voltage (v)	Power decapita-tion 10 Ghz frequency (micro watt)	Propagation delay (pico sec)	Load capacitance (ff)
MOS	0.2503	140.91	3.535	2.865×10^{-9}
SOI	0.1926	110.62	2.773	2.219×10^{-9}
SON	0.1848	105.09	2.634	2.104×10^{-9}

Table 2 – Power dissipation and propagation delay of inverter for various device parameter

Device		*Na* = 1 – 10 × 10^{21}	*Lz* = 50 – 330 × 10^{-9}	*Tgox* = 5 – 8.5 × 10^{-9}	*Tsi* = 30 – 90 × 10^{-9}
MOS	Power (mW)	596.61 – 600.19	758.81 – 728.12	264.14 – 266.33	610.24 – 614.13
	Delay (pS)	2.213 – 2.200	2.665 – 2777	0.984 – 0.976	2.303 – 2.288
SOI	Power (mW)	492.13 – 494.63	592.01 – 570.64	267.83 – 269.53	480.60 – 482.93
	Delay (pS)	1.761 – 1.752	1.990 – 2.065	0.955 – 0.949	1.731 – 1.722
SON	Power (mW)	469.78 – 471.92	592.45 – 574.15	265.11 – 268.04	478.09 – 480.81
	Delay (pS)	1.670 – 1.662	2.019 – 2.084	0.938 – 0.928	1.714 – 1.704

Table 3 – Comparative study of dissipation, delay, capacitance respected to SON based inverter

Device	Power Dissipation (Micro Watt)	Propagation Delay (pico sec)	Load Capacitance (nF)
SON	105.09	2.634	2.104 × 10^{-9}
SOI	5.26 % More than SON	5.27 % More than SON	5.46 % More than SON
MOS	34.08 % More than SON	34.20 % More than SON	36.16 % More than SON

4. CONCLUSION

In the present work we have used our analytical model for SON MOSFET and shown its supremacy over other device like SOI and CMOS devices. We have employed over SON model to realize an inverter and studied its performance with SOI/CMOS inverter. The impact of reduced SCEs on the performance of 120 nm SON MOSFETs circuits is investigated here using the developed analytical model of SON MOSFETs devices. Significant enhancement in the circuit performance is predicted for SON based circuit thereby offering more advantages for low power VLSI circuit.

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