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CURRENT TRANSPORT BEHAVIOUR OF Au/n-GaAs SCHOTTKY DIODES GROWN ON Ge SUBSTRATE WITH DIFFERENT EPITAXIAL LAYER THICKNESS OVER A WIDE TEMPERATURE RANGE

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*The work presents temperature dependent forward and reverse current-voltage (I-V) analyses of n-*GaAs/Au *Schottky Diodes grown on* n^+ Ge *substrate with different epitaxial layer thicknesses. While some of the Schottky diodes follow TED mechanism, others exceed significantly from this theory due to existence of patches of reduced barrier height embedded in the Schottky interface. The zero bias barrier heights (*ϕ_{bo}*) increase (*0.649 *to* 0.809 *eV) while the ideality factors (*η*) decrease (*1.514 *to* 1.052*) with increase in epitaxial layer thickness (*1-4 μm*), thus, indicating similar behaviour to that observed for the I-V characteristics of the undertaken Schottky diodes with decreasing temperature. It all indicated the existence of barrier inhomogenities over the M-S interface. The breakdown behaviour analysis of these diodes showed some interesting results; the breakdown voltage (*V_{BR}*) decreases with temperature and shows 'Defect Assisted Tunneling' phenomenon through surface or defect states in the* 1 μm *thick epitaxial layer Schottky diode while* V_{BR} *increases with temperature in* 3 μm *and* 4 μm *thick epitaxial layer Schottky diodes which demonstrate 'Avalanche Multiplication' mechanism responsible for junction breakdown. The reverse breakdown voltage is also seen to increase (*2.7-5.9 *Volts) with the increase in epitaxial layer thickness of the diodes. The undertaken diodes have been observed to follow TFE mechanism at low temperatures (below* 200 *K) in which the tunneling current component increases with epitaxial layer thickness which has been ascribed as an impact of* GaAs/Ge *hetero-interface over the* Au/*n-*GaAs *Schottky barrier.*

Keywords: *IDEALITY FACTOR, BARRIER HEIGHT, THERMIONIC FIELD EMISSION, TUNNELING, INHOMOGENITIES, JUNCTION BREAKDOWN, RICHARDSON CONSTANT.*

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1. INTRODUCTION

Gallium Arsenide Schottky Barrier Diodes have been a subject of an extensive investigation on account of their widespread applications in optoelectronics and microwave devices. In the large scale integration of GaAs devices, there is an urgent need to improve the metal-semiconductor contacts for high speed optoelectronic applications.

It has now been well established that metal-semiconductor structures especially Schottky contacts play a key role in making new semiconductor devices [1-4]. Due to its technological importance, full understanding of the nature of their electrical characteristics has been explored. It has also been explored that the interface properties of MS contacts show a dominant impact on the device performance, reliability and stability [5]. The interfaces are very complex regions and their behaviour depend on the preparation conditions [6]. It has been reported in some works in the recent past that the barrier height inhomogenity is caused by grain boundaries, defects, existence of multiple phases in the metal-semiconductor interface [7-9]. The presence of small regions of low barrier heights was experimentally evidenced by using Ballistic Electron Emission Spectroscopy (BEES) [10, 11]. Efforts have also been made to describe the anomalies of the conduction mechanism over Schottky barriers by using TFE theory [12].

Work has also been reported regarding the use of GaAs/Ge epitaxial heterostructure interface for the fabrication of space quality Solar Cells [13] wherein Ge behave as an optimized substrate material for high efficiency GaAs/Ge photovoltaic devices. The GaAs/Ge heterostructures are, however, found extremely sensitive to defects. In the present work, an attempt has been made to establish the current transport phenomenon of the Au/n-GaAs Schottky Diodes at different n^- GaAs thicknesses grown on n^+ Ge substrates as studied over a wide temperature range.

2. EXPERIMENTAL

Schottky Diodes of the type n^-GaAs/Au, with different n-GaAs epitaxial layer thicknesses were grown on n^+ Ge substrate, mounted on the To-39, package and undertaken for the forward and reverse biased current-voltage (I-V) analyses over a wide temperature range. The room temperature I-V characteristics were measured using an automated arrangement consisting of a Keithley's Source Meter (Model 2400), an IBM PC (Pentium-IV) and a Probe Station. The To-39 headers were mounted on a Closed-Cycled Liquid He refrigerator (CTI-Cryotronics Model 22CP) equipped with temperature controller (Lake Shore Model 321) for measuring the temperature dependent I-V characteristics. The temperature dependent I-V characteristics of the Schottky Diodes were carried out from room temperature to low temperatures. The temperature was maintained within a step ± 1K during the data acquisition. The carrier concentrations of the grown epitaxial layers were measured using capacitance-voltage (C-V) measurement at 1MHz frequency using HP 4194A LCR Bridge. The carrier concentration was subsequently confirmed by an electrochemical C-V (ECV) profiler measurement setup.

3. RESULTS AND DISCUSSION

3.1 Current-Voltage (I-V) characteristics:

The room temperature forward and reverse biased current-voltage (I–V) characteristics of the Au/n^-GaAs/n^+Ge Schottky Diodes at different epitaxial layer thicknesses have been plotted in Fig. 1.

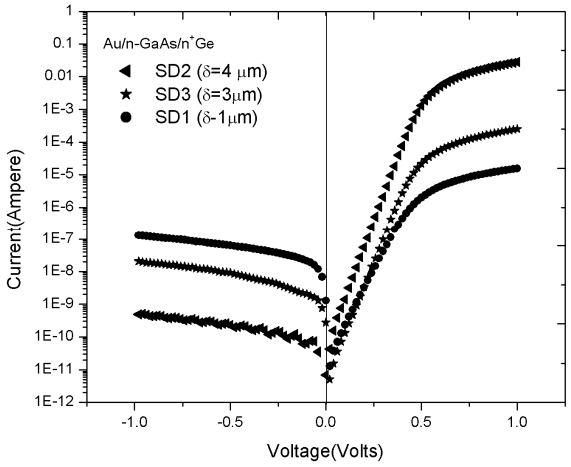

Fig. 1 *– Room temperature forward and reverse biased current-voltage (I-V) characteristics of the* Au/*n*-GaAs/n^+ Ge *Schottky Diodes with epitaxial layer thicknesses of* 1 *μm (SD1),* 4 *μm (SD2) and* 3 *μm (SD3) respectively*

The current through a uniform Metal-semiconductor interface is normally considered on the basis of thermionic emission theory expressed as under:

$$I = I_S\left[\exp\left(\frac{q(V - IR_S)}{\eta KT}\right) - 1\right] \tag{1}$$

where I_S, the saturation current and J_S, the saturation current density defined as :

$$J_S = I_S/S = A^{**}T^2 \exp\left(-\frac{q\phi_{b0}}{KT}\right) \tag{2}$$

The quantities S, A^{**}, T, k, q, ϕ_{bo} and R_S are the diode area, the effective Richardson constant, the temperature in Kelvin, Boltzman's constant, the electronic charge, the zero bias barrier height and the diode series resistance, respectively. ϕ_{bo} is the effective barrier height determined from I_S found from the experimental data of Schottky Diodes. The effective Richardson constant value of 3 A $cm^{-2}K^{-2}$ was used for n^- GaAs [14]. The ideality factor, ɥ is introduced to describe the deviation of the experimental I-V data from the ideal TED model ($\eta = 1$ for ideal case). The effective values of ideality factor using equation (1) is given by

$$\eta = \frac{q}{KT}\frac{dV}{d\ln\left(I/I_S\right)} \tag{3}$$

At room temperature, the undertaken Schottky Diodes, exhibit linearity over five to six orders on the current axis, the linearity, however, decreases with decrease in temperature. Room temperature characteristics of SD1-SD3 Schottky Diodes shift towards higher bias side while the current density decreases (9.23×10^{-13} to 1.65×10^{-15} A/m^2) with reduction in epitaxial layer

thickness. The forward I-V characteristics of the undertaken Schottky Diodes (SD1-SD3) have been measured from room temperature to low temperatures as shown in Fig. 3(a-b). A computer program is utilized to fit the experimental I-V data taking ϕ_{bo}, η and R_S as adjustable parameters [15]. The parameters J_S, ϕ_{bo}, η and R_S measured from the I-V characteristics have been illustrated in Table 1. The values of R_S (18-23 Ω) given in Table 1 determined from the fittings are justified since heavily doped substrates been used.

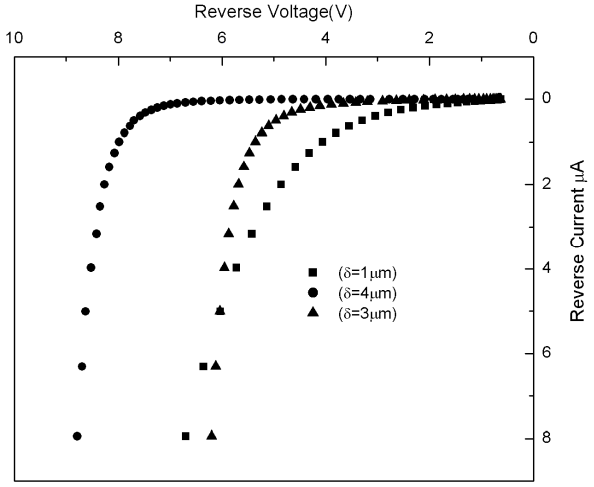

Fig. 2 *– Reverse biased I–V Characteristics of three different epitaxial thicknesses in the* Au/n^-GaAs/n^+Ge *Schottky diodes measured at room temperature*

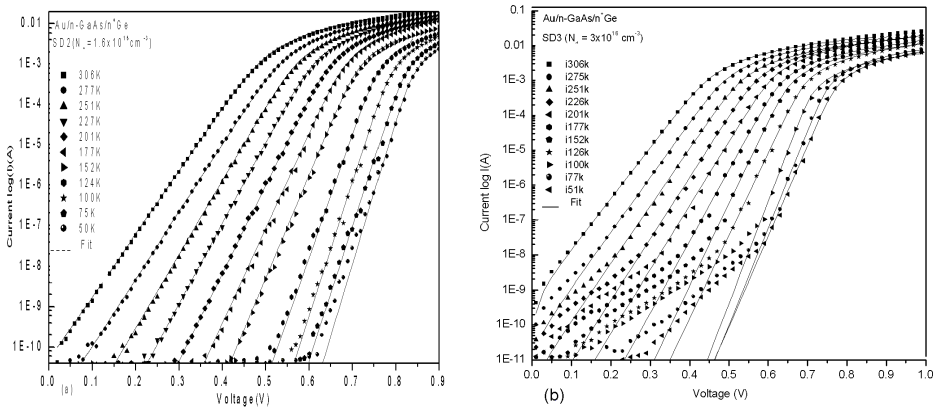

Fig. 3 *– Forward I-V characteristics of n-*GaAs/Au *Schottky Diodes of and a) 4 μm (SD2) b) 3 μm (SD3) at different temperatures (Diode area* = $1.25 \times 10^{-7} m^2$*)*

The fitting curves according to equations (1) and (2) have also been shown as solid lines. The theoretically generated curves match the experimental data quite well at higher temperatures and at large bias at low temperatures. In Fig. 3 (a), the experimental I-V data in SD2 is seen fitted over the entire bias

range at all temperatures. However, in SD3, shown in Figure 3 (b), I-V characteristics show deviations at the current values below 10^{-8} A. Similar, deviations have also been observed below the current values of 10^{-6}A in SD1 (not shown in the Fig. 3). Referring Fig 3 (b), it is observed that the currents in the small bias region in SD3, exceeds significantly to the predicted TE values, a typical plateau like section has been observed in this case which may be due to the 'patches' of reduced barrier heights embedded in the Schottky interface explained on the basis of Tung's pinch-off model [16].

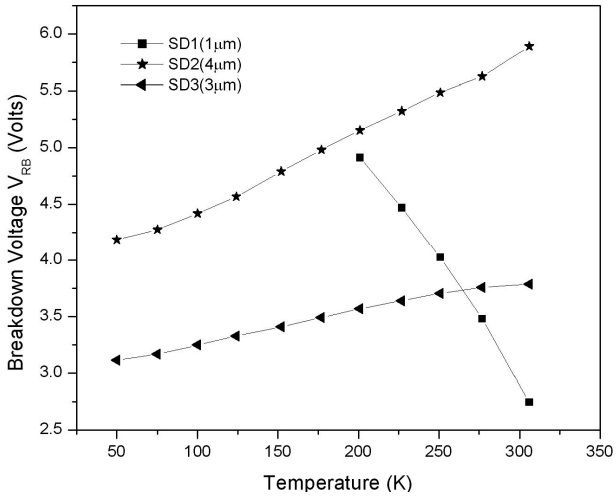

Fig. 4 *– Breakdown Voltage V_{BR} vs. Temperature for n⁻GaAs/Au Schottky diodes grown on* Ge *substrate with different epitaxial layer thicknesses*

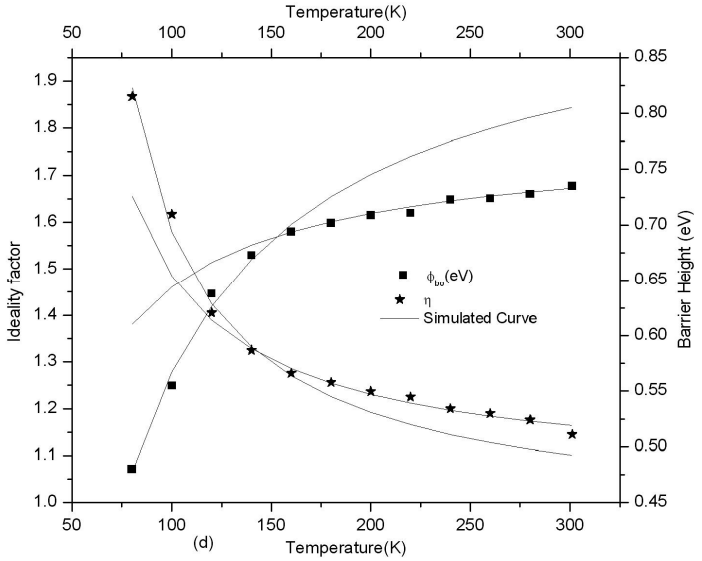

Fig. 5 *– Typical zero bias barrier heights and ideality factors for n⁻GaAs/Au Schottky diodes grown on Ge substrate*

The reverse characteristics of the undertaken Schottky diodes have been plotted in Fig. 2. It is observed that at room temperature, the breakdown voltage (V_{BR}) increases with epitaxial layer thickness as shown in Table. 1. Further, referring Fig 2, it is observed that the knee point is not well defined and causes 'soft' breakdown phenomenon in SD1. However, in case of SD2 and SD3, well-defined knee voltage is observed and thus causes 'sharp' breakdown voltages. The reverse breakdown voltage (V_{BR}) verses temperature plots of all Au/n^-GaAs/n^+Ge Schottky diodes have been plotted in Fig. 4. The breakdown voltage, V_{BR} has been defined as the reverse voltage at which the current becomes equal to few micro amperes [17].

Table 1 *– Au/n-GaAs/n^+-Ge Schottky diode parameters at different n-GaAs epitaxial thicknesses measured at room temperature*

Diode Parameters Symbol	J_S (A/m^2)	Epitaxial Layer Thickness (μm)	V_{BR} (V)	η	ϕ_{bo}	R_S (Ω)
SD1	9.23×10^{-13}	1	2.7	1.514	0.649	23
SD2	1.65×10^{-15}	4	5.9	1.052	0.809	18
SD3	1.94×10^{-14}	3	3.8	1.129	0.744	22

Table 2 *– Schottky interface parameters of SD1-SD3 Schottky Diodes determined over a wide temperature range*

T (K)	SD1(*1μm thickness*)			SD2(*4μm thickness*)			SD3(*3μm thickness*)		
	η	ϕ_{bo}	R_S(Ω)	η	ϕ_{bo}	R_S(Ω)	η	ϕ_{bo}	R_S (Ω)
300	1.513	0.649	22	1.052	0.809	18	1.129	0.745	22
275	1.561	0.628	23	1.057	0.811	19	1.167	0.728	22
250	1.59	0.617	26	1.075	0.808	20	1.223	0.714	25
225	1.601	0.608	26	1.115	0.794	18	1.270	0.696	22
200	1.643	0.59	20	1.160	0.775	18	1.370	0.658	18
175				1.213	0.753	16	1.391	0.642	25
150				1.260	0.723	22	1.410	0.623	28
125				1.300	0.705	25	1.690	0.537	25
100				1.533	0.614	24	1.720	0.517	43
75				2.145	0.457	21	2.350	0.393	29
50				3.300	0.301	22	3.810	0.247	30

It is observed that the breakdown voltage of SD2 (4 μm*)* and SD3 (3 μm*)* are found to increase linearly with temperature and so the breakdown voltage has positive temperature coefficient which is indicative of 'Avalanche Multiplication' mechanism responsible for junction breakdown [18]. However, in case of SD1 (1 μm*)*, the breakdown voltage decreases with temperature and gives negative temperature coefficient which indicates the possible breakdown mechanism as 'Defect Assisted Tunneling' through surface or defect states.

3.2 Zero-bias barrier height, ideality factor and series resistance

A typical plot of the zero bias barrier heights (ϕ_{bo}) and ideality factors (η) derived from the fittings of the I-V data of SD1-SD3 Schottky Diodes at various temperatures using equations (1) and (2) has been plotted in Fig. 5. In all the diodes, the zero-bias barrier heights (ϕ_{bo}) decrease and ideality factors (η) increase with decrease in temperature has been given in Table 2.

Referring to Table 1 and 2, it is observed that the zero-bias barrier heights increase and ideality factors decrease with the increase in epitaxial layer thickness, these changes are indicative of deviations of the current transport phenomenon from the pure thermionic emission diffusion (TED) mechanism and there is a current flow, in excess, to that due to the standard thermionic emission diffusion (TED) theory. Similar trend is also observed with increase in temperature of the I-V characteristics measurements. The reason for considerable deviations may be due to the impact of Ge substrate on the n^-GaAs semiconductor surface which may cause increased density of states at the semiconductor surface due to surface roughness, imperfections etc.

The barrier height can also be determined from $\ln(J_S/T^2)$ versus $(1000/T)$ plot obtained by re-arranging equation (2) in the manner given below :

$$\ln\left(J_S/T^2\right) = A^{**} - \frac{q\phi_{b0}}{KT} \tag{4}$$

Therefore, the $\ln(J_S/T^2)$ versus $(1/T)$ plot should be a straight line with the slope yielding the zero bias barrier height (ϕ_{bo}) and the intercept at the ordinate, the effective Richardson constant (A^{**}). An example of the type of usual and the modified Richardson plots are shown in Fig. 6.

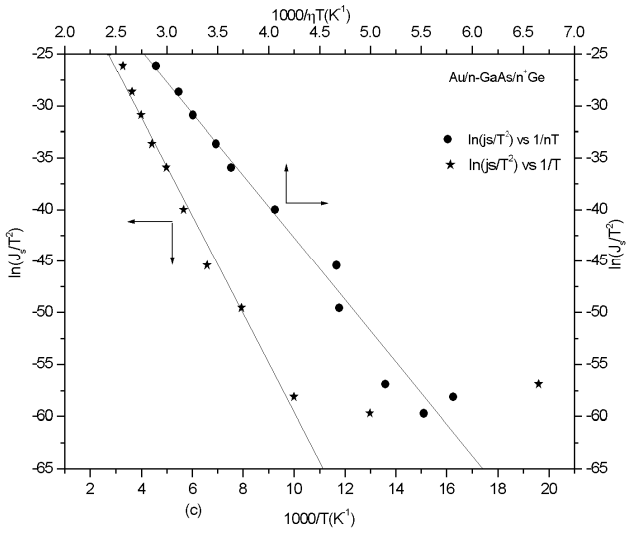

Fig. 6 *– The Usual and modified Richardson plots* $\ln(J_S/T^2)$ *versus* $1000/T$

These plots show non-linear behavior at low temperatures, which demonstrate deviations from TED phenomenon. The asymptotical fit of the linear data yields effective Richardson constant (A^{**}) and an activation

energy values (ϕ_{bo}). The non-linearity in $\ln(J_S/T^2)$ versus $1000/T$ plot at lower temperatures is due to rapid decrease in ϕ_{bo} with fall in temperature. The values of A^{**} and ϕ_{bo} obtained from the Richardson plots of the undertaken Schottky diodes (SD1-SD3) don't come to any concrete interpretations of the current transport mechanism.

3.3 Effect of barrier inhomogeneity's

The temperature dependence of Schottky barrier parameters have been reported to be explained on the basis of the barrier height inhomogeneity's existing in the M-S interface which has been attributed to the variation in thickness, composition of interfaced layer and non-uniformity of interfacial charges. Werner and Guttler [20] explained this abnormal behavior on the basis of Gaussian distribution function with a mean barrier height ϕ_{bm} and standard deviation σ_S emanating from the center to the sides and is represented [19-21],

$$\phi_{b0} = \phi_{bm} - \left(\sigma_S^2 q \Big/ 2KT \right) \tag{5}$$

where σ_S gives the measure of the barrier inhomogeneity.

The plot of ϕ_{bo} versus $1/T$ using equation (5) is straight line with intercept at the ordinate determining the mean barrier height (ϕ_{bm}) and slope the standard deviation (σ_S). The values of ϕ_{bm} and σ_S obtained for the undertaken Schottky diodes have been presented in Table 4. The back substitution of ϕ_{bm} and σ_S values in equation (5) provides continuous curves in Fig. 5 for the ϕ_{bo} and η values.

Further, the abnormal behaviour of ideality factors with temperature has been explained by considering the potential fluctuation model [20]. According to this model, the variations in the ideality factors with temperature are given as:

$$\frac{1}{\eta} = 1 - \gamma + \frac{q\xi\sigma_S}{KT} \tag{6}$$

where γ and ζ are the voltage coefficients of barrier heights and standard deviations, respectively.

The plot of $1/\eta$ versus $1/T$, according to equation (6) should exhibit a straight line with the slope and intercept yielding voltage coefficients of barrier heights, γ and standard deviations, ζ. The values of γ and ζ thus obtained for the undertaken Schottky Diodes are also presented in Table 4. The back substitution of γ and ζ values in equation 6 provided continuous curves for ideality factors in Fig. 5. The existence of 'Double Gaussian Distribution function' observed in SD2 and SD3 can also be attributed to some phase transformation occurring at the Schottky Diode interface. The factors responsible for this type of change may be the composition, electrical charges, non-stoichiometry etc. likely to exists at the MS Schottky interface below certain temperature values [22]. Table 4 demonstrates that the mean barrier heights (ϕ_{bm}) increase with epitaxial layer thickness, thus, confirms the existence of barrier inhomogeneity's over the Schottky interface due to increased epitaxial layer thickness.

3.4 Thermionic Field Emission

The forward current-voltage characteristics on the basis of thermionic field emission (TFE) can be expressed as [1]:

$$I = I_S \exp(V/E_0) \tag{7}$$

where

$$E_0 = E_{00} \coth\left(qE_{00}/KT\right) = \eta KT/q \tag{8}$$

where E_{00} is the characteristic energy related to the 'carrier transmission probability' through the barrier that determines the relative importance of tunneling [23] represented as:

$$E_\infty = \frac{h}{4\pi}\left(\frac{N_D}{m_e^* \varepsilon_S}\right)^{1/2} = 18.5 \times 10^{-15}\left(\frac{N_D}{m_r e_r}\right)^{1/2} \text{eV} \tag{9}$$

Here, $m_e^* = (m_r, m_o)$, the effective mass of electrons $\varepsilon_s = (\varepsilon_r\, \varepsilon_o)$, the permittivity of the semiconductor and N_D, the donor concentration.

According to Padovani and Sumner [23], the characteristic energy, E_{00} indicates that the current transport mechanism is field emission (FE), if $E_{00} >> KT$; the thermionic-field emission (TFE) if $E_{00} \sim KT$; and thermionic emission (TE) if $E_{00} << KT$.

Further, the ideality factor in case of TFE can be expressed as [23]:

$$\eta = \eta_E = qE_{00}/\left(1 - \beta\right) KT \tag{10}$$

A typical $1/\eta$ versus $1000/T$ plot of the experimental data fitted with theoretically generated curves on the basis of Thermionic Field Emission (TFE) according to equation (10) have been illustrated in Fig. 7. The experimentally observed as well as theoretically generated E_{00} values for SD1-SD3 are given in Table 5.

Table 4 *– Barrier height inhomogeneity parameters of the undertaken Schottky diodes (SD1-SD3)*

Diode Symbol	Thickness	ϕ_{bm} (eV)	σ_s	γ	ζ
SD1	1	0.74	0.07	0.26	0.03
SD2	4	0.93	0.08	0.07	0.05
SD3	3	0.86 (Slope I) 0.79 (Slope II)	0.08 0.07	0.18 0.09	0.09 0.04

It has been observed that in SD1, E_{00} is 11.71 in the existing temperature range (300-200 K) is anomalously higher than the theoretical E_{00} value while two set of values been observed for E_{00} and β in Schottky Diodes are 13.27 and 0.03 in the temperature range 306-152 K and 15.15 and 0.16 in the temperature range 152-50 K for SD2 and 18.86 and 0.02 in the temperature range 306-152 K and 12.41 and 0.10 in the temperature range 126-51 K for SD3. This display anomalously high experimental E_{00}

values than theoretical ones as illustrated in Table 5. Further, the condition $KT = E_{00}$ is met at low temperatures (below 200 K) in SD1 and SD2. Further, two set of E_{00} and β values observed at the different temperature regions of Schottky diodes SD2 and SD3 outlines the existence of two distinct phases occurring over the MS interface with a phase transition occurring at 150 K.

Table 5 – *The theoretical E_{00}, I-V fitted E_{00}, β and their ratio R_E of the undertaken Schottky diodes (SD1-SD3)*

Diode Symbol	Thickness (μm)	Theoretical E_{00} (meV)	I-V fitted E_{00} (meV)	β	R_E = experimentalE_{00}/Theoretical E_{00}	KT/qE_{00} (eV)
SD1	1	1.41	11.71	0.30	8.3	26.7 (309 K) 17.3 (201 K)
SD2	4	2.53	13.27 (306-152 K) 15.15 (124-50 K)	0.034 (306-152 K) 0.16 (306-152 K)	5.25 5.99	26.4 (306 K) 13.1 (152 K) 10.7(124 K) 43.1(50 K)
SD3	3	3.46	18.86 (306-152 K) 12.41 (126-51)	0.02 (306-152 K) 0.106 (126-51)	5.45 3.59	26.4 (306 K) 13.1 (152 K) 10.9 (126 K) 44.0 (51 K)

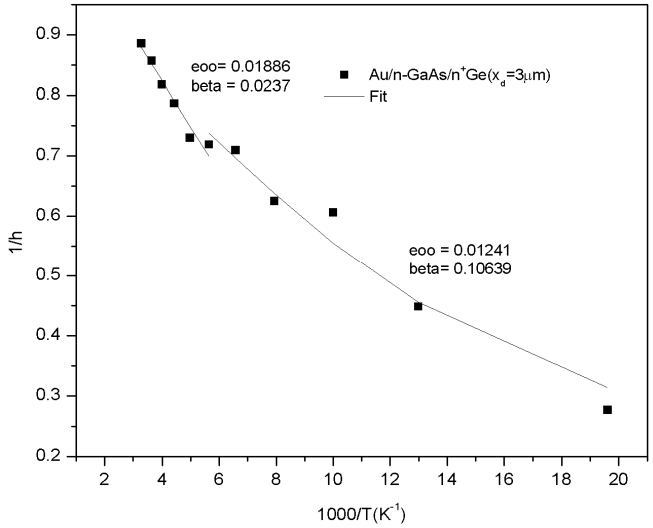

Fig. 7 – *Plot showing $1/\eta$ versus $1000/T$ along with generated curves using Eq. (10) giving E_{00} and β values. The experimental points are also superimposed on the theoretically generated plot shown by solid lines*

Therefore, TFE phenomenon is found to exist at low temperatures in the undertaken Schottky diodes and tunneling current component increases with epitaxial layer thickness. Further, it is anomalously high in diodes containing 'patches' of reduced barrier heights embedded in the Schottky interface area which demonstrate TFE mechanism even at room temperature.

This may be ascribed to a mechanism that controls change in electric field or density of states, interface quality, non-stoichiometry etc. at the semiconductor interface [22, 24].

The changes in the form of increased tunneling current component with change in epitaxial layer thickness observed in the current transport mechanism of the undertaken diodes may be due to the impact of GaAs/Ge hetero-interface over the Au/n-GaAs Schottky barrier.

It is also found that the breakdown voltage decreases with temperature and shows 'Defect Assisted Tunneling' phenomenon through surface or defect states in thin epitaxial layer Schottky diodes (~1 μm) while it increases with temperature in thick epitaxial layer Schottky diodes (~3 μm or above) which demonstrate 'Avalanche Multiplication' mechanism responsible for junction breakdown. Further, the reverse breakdown voltage is also seen to increase with the epitaxial layer thickness of the diodes.

This finding of tunneling breakdown mechanism is quite different than the conventional breakdown mechanism of Avalanche Multiplication normally observed in Schottky diodes.

Further, the existence of patches significantly change the reverse characteristics and the breakdown voltage of the Schottky diodes.

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