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NEW EVOLVING DIRECTIONS FOR DEVICE PERFORMANCE OPTIMIZATION BASED INTEGRATION OF COMPOUND SEMICONDUCTOR DEVICES ON SILICON

***Partha Mukhopadhyay*[1], *Palash Das*[1], *Edward Y. Chang*[2], *Dhrubes Biswas*[1]**

[1] Indian Institute of Technology,
721302, Kharagpur, India
E-mail: partha@ece.iitkgp.ernet.in

[2] National Chiao Tung University,
Hsinchu, Taiwan

Rapid advances in Compound Semiconductor (CS) technologies over last several decades have lead to high performances in peak power, power added efficiency (PAE) and linearity, but these devices are not amenable for integration on mainstream silicon technologies. A strategic direction has been presented for the growth of CS devices on silicon with challenges abounding in scalability, compatibility and cost effectiveness while extracting optimized device performances. The approach at IIT Kharagpur has been simulation and experimental development of customized metamorphic buffers that are scalable and compatible to silicon without sacrificing any CS performances, primarily for electronic applications. This has evolved into a new strategic paradigm for performance optimization of seemingly competing and disparate properties which otherwise will not be supported by conventional process technologies. Simulation of these next generation structures reveals assimilation of superior device properties, with a novel five Indium content composite channel MHEMT indicating improvements over existing composite channel MHEMT in terms of linearity and higher current performances.

Keywords: *METAMORPHIC BUFFER, COMPOUND SEMICONDUCTOR, INTEGRATION, III-V/Si, STRAIN, DISLOCATION DENSITY, LATTICE MISMATCH, COMPOSITE CHANNEL.*

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1. INTRODUCTION

The demand on high-speed transistors and circuits with low-noise figure and low-power consumption increased dramatically over the past few years due to the exponential growth of wireless and fiber communication market. Additional requirement is high power in high frequency which helps to implement the long rang space communication. Quantum well based heterostructure devices (HEMT/HBT) mainly using III-V material shows capability to achieve the above requirements. It is well known that lattice matched InP HEMT [1] /HBT [2, 3] i.e. InGaAs/InP has enormous potential to realize high speed as well as high linearity devices due to the superior carrier transport and other favourable electronic properties. On the other hand, nitrides, especially Gallium Nitride and its alloy based semiconductors are nowadays used in high power applications due to their wide bandgap properties. However, in both cases, the lack of improvement in buffer

technologies creates an adverse environment to grow these devices on electronically good as well as low cost substrate. Available size of InP/SiC wafer is 2-4 inches which leads to huge cost per unit area and implies the use of older fabrication technologies. A potential solution for performance/cost dilemma is to the growth of high quality GaAs/InP/GaN on well matured low cost substrate (GaAs/Si) by metamorphic techniques.

As a result silicon has been attempted as the substrate of III-V growth even though there is a huge lattice and thermal expansion co-efficient mismatch between them. Main advantage is the integration of III-V high performance devices with Si logic circuits on a single silicon wafer. This has inspired new era of research in integration of CS devices on silicon for keeping on track with Moore's law, more so from major silicon foundries. Expensive III-V compound semiconductor substrates are known for their fragility compared to Si, and InP substrates in particular are even more brittle than GaAs. It is well-known that due to the large lattice mismatch (8 %) InP heteroepitaxial growth on silicon is very difficult than GaAs or GaP growth on silicon [4]. Residual strain is very high; hence surface morphology of InP layers grown directly on Si is very poor, with a matte appearance [4]. A novel approach is using GaAs buffer layer for effectively reducing residual stress and dislocation density in InP/Si. Among III-V compounds, InP has been widely used in HEMT for its high peak velocity for electron transport and relatively low surface recombination velocity [5] make it a promising material for microwave applications. The growth of InP on lattice-mismatched substrate, particularly on silicon and gallium arsenide, has considerable technological challenges [6-9]. GaAs on Silicon (GOS) is advantageous when GaAs buffer is used between InP and Si [4]. Better crystalline quality can be achieved in this case than InP grown directly on Si. Substantial quality improvements experienced with increasing layer thickness [4]. On the other hand, sufficiently high bandgap of GaN based devices results in high power up to moderately high frequency applications. Novel nucleation layers as well as composite buffer layers of AlN, SiC, SiN_x, HfN, BP etc may be used to release residual stress between GaN & Si.

2. STRATEGIC INTEGRATION CHALLENGES

2.1 Metamorphic buffer in InP growth

Over the last few years, metamorphic techniques have resulted in growth of high quality InP on semi-insulating GaAs. This combination has the outstanding gain of InP as active layer with the advantages of economies of scale and robustness offered by conventional GaAs substrate processing [10-13]. In metamorphic scheme the active layers of the HEMT/HBT device are grown on top of a compositionally graded buffer layer (metamorphic buffer) which expands the lattice constant from that of the GaAs substrate to InP. The buffer has two primary purposes: (a) to maintain a small constant stress to prevent uncontrolled dislocation nucleation and (b) to trap existing dislocations thereby relaxing lattice mismatch and prevent them from propagating into the device channel. Novel approach of extending the metamorphic technique can be used for the growth of InP on Si through GaAs.

The efficacy of metamorphic technique is to relax the film from strain without nucleating more dislocation at the substrate / film interface. Long misfit dislocations in graded buffer can reduce threading dislocation ρ_t. An

ideal graded buffer should have ρ_t lower than 10^6 cm^{-2} for better device performance [14]. Smooth morphology contains higher dislocation between metamorphic buffer and active layer and it depends on plastic relaxation [15].

Generally higher bandgap material is used as metamorphic buffer than that of the substrate material, which reduces the residual carrier concentration in active layer where high resistivity buffer helps in device isolation, and reduced junction leakage [16]. Typically III-III-V (InAlAs, InGaP), III-V-V (InAsP), III-III-III-V (InGaAlAs) and III-III-V-V (InAlAsP) based metamorphic approach of developing heterostructure devices on GaAs are being extended on silicon by invoking newer alloy systems that are compatible to silicon and CS. The contributing material aspects are well studied with Bandgap vs. Lattice constant plot as shown in Fig. 1.

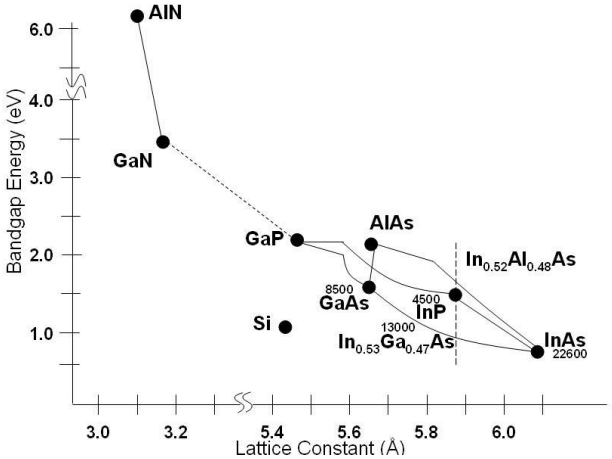

Fig. 1 *– Energy bandgaps vs lattice constants of III-V compound semiconductor materials. The numbers are μ (cm^2/V-s) in respective bulk materials at* 300 *K*

2.2 Nucleation growth for GaN epitaxy

The result of parametric mismatch between GaN & Si leads to a high degree of cracks on the device layer due to the stress generated at the interface of GaN and Si due to lattice mismatch (~16%) and thermal expansion co-efficient mismatch (~ 54 %) [17]. It impedes GaN thick layer growth on Si. Additionally, Si substrate resistivity can be extended upto 10^4 ohm·cm which is less than that of prevailing sapphire substrate and it leads to unnecessary parasitic capacitance effects. Gallium leads to poor wetting on Si, that converts exposed regions to amorphous SiN_x creating epitaxial discontinuities [18]. During the growth of GaN on Si in hydrogen environment at ~1200 K temperature, the substrate outgases Si [19,20] resulting an unintentional n type doping in the device layer. However, pre-treatment of substrate with ammonia leads to the formation of Si_xN_y layer, protecting the substrate from out-gassing, thus preventing unintentional doping.

3. GROWTH ISSUES

3.1 GaAs/Si

Considering the Matthews & Blakeslee model, 4 % lattice mismatch [21] leads to misfit dislocations which relax the strain. This misfit dislocation is generated by two possible mechanisms: nucleation of dislocations at the high shear stress edges of the initial three-dimensional (3D) GaAs islands [22] and nucleation of half dislocation loops on the GaAs surface and their expansion towards the interface [23]. Substantial reduction in the density of threading dislocation, as low as 10^3-10^4 cm^{-2} in 2 μm thick GaAs on Si epitaxial layers, is possible by using proper orientation of substrates, such as the wafer is oriented 2°-4° off (100) towards the [011] orientation to reduce anti-phase domain formation in the overgrown layers [24]. Strained GaAs pseudomorphic superlattice layers [25] reduce dislocation densities by reflection or termination of many of the threading dislocations by about one order of magnitude. Reconstruction of the miscut Si surface takes place during annealing procedure prior to the GaAs deposition; hence anti-phase boundaries do not play significant role in this heterostructures [26-28].

Motorola, in collaboration with IQE, has demonstrated GOS by placing a very thin layer (about 50 Å) of high-k dielectric strontium titanate (known as strontium titanium oxide, $SrTiO_3$ or STO) between them [29] with lattice mismatch falls roughly halfway (2.3 % with GaAs, and 1.7% with Si) between GaAs and Si, hence it compensates the large lattice mismatch. Moreover, between Si and STO, an amorphous layer of SiO_x (10-20 Å thick) forms, which helps to grow low stress heteroepitaxial layer, which absorbs the lattice mismatch strain [30], and allowing the crystalline STO to form a normal lattice without distortion from the underlying Si [31]. Research is being pursued at our lab in comparable transitional materials involving dilute alloys for heteroepitaxy of CS on Si.

3.2 InP/GaAs/Si

From Fig. 1, it is evident that one can choose many pathways using different III-V materials (containing In, Ga, Al, As, and P atoms) to gradually increase the lattice constant toward InP starting from GaAs (3.7 %. mismatch). A critical analysis of energy gap versus lattice constant diagram revealed that there are three ternary materials path, namely InGaAs, InAlAs (InGaAlAs), and InGaP to get high-quality ($\rho_t \leq 2 \times 10^6$ cm^{-2}) InP on GaAs [14]. Due to the extensive use of InGaAs material as channel layer, researchers prefer InAlAs material as buffer/charge supply layer for its higher band gap [32-34].

First pathway is to gradually addition of In with GaAs which causes slowly increase in the lattice constant from GaAs to InP. Suppression of phase separation with increased indium is necessary, which can also be affected by wafer orientation [31-33]. Second pathway from GaAs lattice constant to InP is through In(Ga)AlAs. Miscibility gap is repressed by the addition of Al to InGaAs and allowed for higher In content films without having composition variations strong enough to block dislocation glide in InGaAlAs materials [14]. Graded buffer quality deteriorates due to the substitution of Al for Ga. However, experimentation with the quaternary InGaAlAs showed that by increasing Al along with In, high-quality $In_{0.43}Ga_{0.14}Al_{0.43}As$ with $\rho_t \sim 10^6$ cm^{-2} could be achieved as evident in lattice constant with energy

bandgap diagram. An alternative third way starts with lattice-matched $In_{0.49}Ga_{0.51}P$ on GaAs, and gradually increasing the In composition to a final switch from $In_{0.82}Ga_{0.18}P$ to $In_{0.28}Ga_{0.72}As$ and beyond.

Tactically, lattice mismatch InP/GaAs/Si can be lowered by first growing an amorphous GaAs epitaxial layer on heated Si with good surface flatness, followed by an amorphous InP buffer layer having a good surface flatness and finally an InP mono-crystalline thin film is grown on the InP buffer layer [35].

3.3 GaN/Si growth

Research is still being carried out to find the appropriate buffer material for the GaN/Si interface. Lattice mismatch in GaN/Si depends on the orientation of the substrate. Si (111) is mostly preferred for AlN for their six fold atomic arrangement (three fold symmetry) at the surface. In heteroepitaxial growth, threading dislocation originates from the lattice mismatch. But in nitride growth case, the high mismatch leads to misfit dislocation which does not propagate vertically. But the mismatch causes tilt and twist to the device layer. Hence sometimes it is preferred to incorporate twisted or tilted arrangement for good quality epilayer growth. Si (110) may be proven as a good orientation for GaN growth because of very little lattice mismatch. The mismatch in the direction AlN [1100]/Si[100] and AlN[1120]/Si[110] is only 0.7% which is a good indication of using Si (110) [36].

AlN is widely used for thick growth of GaN on Si, however further research is needed for dislocation free growth. It was observed that low temperature AlN seed layer growth results step like surface for longer growth time and leads to nucleation formation like that of island growth. In both the cases the resultant surface becomes rough. Prevention of this defect comes from the solution of pre-deposition of Al seed layer for protecting Si surface [37]. After the exposure to ammonia during GaN growth, the Al layer is converted to AlN buffer. Nitronex's SiGaNtic process [38] uses similar buffer material to grow ~ 2 μm GaN growth on Si with crack free uniform surface. The process comprises of (AlGa)N nucleation layer with proprietary composition and growth-condition profiles.

However, it is important to nullify the compressive stress generated at the GaN/Si interface to achieve high quality GaN epilayer. It has been observed that impurity concentration drives the residual stress amount that enhances the tensile stress [39, 40]. If the tensile stress is comparable to the compressive stress then the device layers can be grown defect free. Another technique for reducing the stress is introduction of patterned substrate surface. In this case, Si_3N_4 or SiO_2 layer is deposited over Si substrate in a patterned way or deep trenches are prepared on masked material. As a result, the dislocations and cracks are guided by the etched layer and they effectively leave the epitaxial layer so as to end up with very good quality epilayer [41]. Also it has been demonstrated that introduction of AlGaN barrier on top of the AlN seed layer [42], superlattice structure [43] etc. can effectively reduce the stress. The mutual solubility of Si and Al is very high at buffer layer temperature which causes inter-diffusion at the surface. These result in unintentional doping and growth challenges with desired doping density. Hence other nucleation materials are investigated to make them compatible at GaN/Si interface. Out of them HfN [44], BP [45], intentional SiN_x [46] etc. are proven to be better for their different properties. Recent developments of

dilute semiconductors also have proven their usability in GaN growth on Si. Approximately lattice matched GaP with dilute nitride that is GaP(N) has been studied elaborately [46] to take strategic advantage of its use in the GaN/Si interface and the results were self-supporting.

4. DEVICE PERFORMANCE BASED DEVICE STRUCTURE OPTIMIZATIONS

The MHEMT device is at the heart of our integration strategy, providing the ability to tailor the lattice constant to any desired indium content channel which allows the device designer an additional degree of freedom to optimize the transistor for high frequency gain, power, and low noise applications. Higher In may lead to phase in-homogeneities [14] which degrades the desirable flat transconductance curve due to the onset of kink effects [48,49]. Improvements of metamorphic buffers for high indium percentage channel will eventually lead to higher mobility with high sheet charge as well as a flat transconductance (g_m) or linear transfer characteristics [50]. Scaling of vertical nano-MHEMT devices & increasing the indium mole fraction in the channel leads to improved performance, but at the cost of reduced gate-drain breakdown voltage (BV) [51], that can be removed by using composite channel structure. We have realized optimized composite channel structure with novel five Indium content channel, as in Fig. 2. Relatively high bandgap of the lower indium mole of InGaAs channel (0.75 eV) limits impact ionization effects and the high band gap of the InAlAs Schottky layer (2 eV) improves the turn on voltage [52], which results in a better on-state Breakdown Voltage (BV), a main limiting factor for power devices. High channel indium content is optimized by the aluminum content in spacer to avoid the kink effect while second next channel layer (x ~ 0.65) helps to introduce further indium content in the middle channel and middle $In_xGa_{1-x}As$ (x ~ 0.78) channel layer improves the electron mobility under low electric field. The two δ-doped layers, between top/bottom channel layers and spacer layer, which overall in turn increases the current density of the devices, therefore improved g_m flatness i.e. high linearity [49].

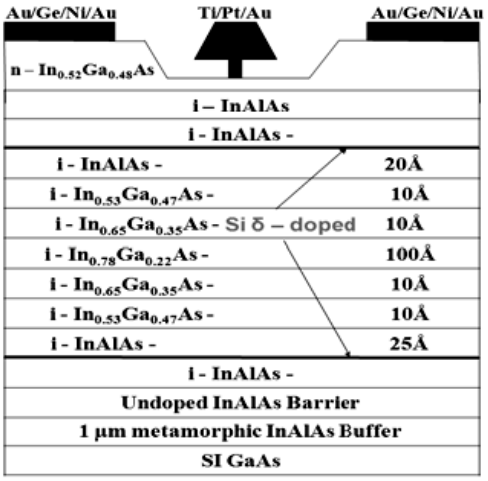

***Fig. 2** – $In_{0.78}Ga_{0.22}As$ composite channel MHEMT*

The simulation using SILVACO of this structure shows very high drain current of 1029 mA/mm and almost flat transconductance of 648 mS/mm for wide range in transfer characteristics [53] while operating at high frequency, ft of 125 GHz and f_{max} of 250 GHz [52]. Our structure shows high drain resistance i.e. less fluctuation at high voltage and high linearity than conventional PHEMTs and MHEMTs. Our structure has gate length, L_g of 0.25 μm, which is much higher than current technology, while achieving very high f_t which is remarkable. It can be attributed to the efficient device structure and choice of materials. This higher gate length leads to lower process costs with high performance devices which can be valuable for low cost wireless/space communications.

5. APPLICATIONS

Integration of III–V semiconductors on Si substrates has received significant interest due to the potential of combining complementary III–V device technologies, such as optoelectronics, with Si CMOS circuits onto a single chip. III–V integration onto Si is also of great interest for space solar cells, power amplifier and low noise amplifier in high frequency transceiver, where Si offers superior substrate properties compared to conventional GaAs or Ge substrates currently being used. Device performance optimization based integration of III-V on Si will open the market of less expensive RF devices, high-speed microprocessor-based and optical communications subsystems, complementing advanced low voltage baseband, low power mixed signal analog, integrated digital ICs and other "beyond Moore's" silicon electronics. Metamorphic technology based silicon III-V integration will usher in scalable, economical and compatible device processing. Comprehensive metamorphic structure study undertaken in our lab will allow analysis of novel buffer structures which have an optimized compatible active device structures for extracting "sought-after" RF and DC properties. Such a performance amalgamation will assimilate advanced silicon electronics with stand-alone CS devices in niche-III/V areas of automotive collision avoidance systems, image processing and vision systems, invasive and non-invasive medical electronics. Additionally it will bring in III-V devices into all-silicon domains, primarily the Moore's-constrained areas of next generation digital electronics, low power, high voltage, sensors/actuators systems particularly in high speed wireless and optical communication systems.

6. CONCLUSION

The momentum from Moore's Law in the silicon industry and requirements of higher device performance necessitates a holistic approach to integration of CS on Silicon. Various metamorphic and heteroepitaxial methods have been discussed with the unified theme towards higher device performance, which are typically disparate, without losing sight of the silicon substrate. Integration efforts on Silicon for GaN based Wide bandgap and InP based high speed devices should be the key focus to seamlessly integrate high performance front end devices including RF, sensors and actuators, with state-of-the-art economical silicon device technologies, particularly in mixed signal analog and other baseband technologies. ATLAS simulation has been used to optimize on existing MHEMT work from the group for achieving

uncompromised device performances on a metamorphic substrate amenable to integration on silicon. Structurally advanced and integration friendly MHEMT with composite channel structure shows greater utilization of the channel with high indium content, which eventually leads to higher power and efficiencies from higher carrier concentration, higher mobility and flat gm transfer characteristics.

7. INTEGRATION STRATEGY OF III-V ON SILICON AT IIT KHARAGPUR

We, HPDG (High Performance Device Group), are working towards establishing a Holistic integration of GaAs based, Indium Phosphide based, GaN based electronic/optical nano-devices on the versatile Si substrate. Blakeslee model guides us on allowable critical thickness for growing on lattice mismatch substrate. This model implies that InP supports lattice matched composition of InGaAs (53 %) & InAlAs (52 %), as in Fig. 1, where alloys can be used as the low bandgap channel and the high band gap barrier sub layers. GaAs based devices forms the backbone of our research as the 'via' medium between the under lying Si/SiGe domain to the over lying InP/GaN domains. Arsenide based nano-initiation layers and thicker metamorphically graded full As and dilute As layers are fundamentally important for novel integration such as Bi-FETs or a GaAs switch driven InP HEMT/HBT or a GaAs HEMT/HBT with GaN on-chip bias control or a GaAs PA with SiGe oscillator forms the basic theme of our high performance device strategy culminating in *system-on-heterogeneous-chip–on-wafer* (SOHCOW).

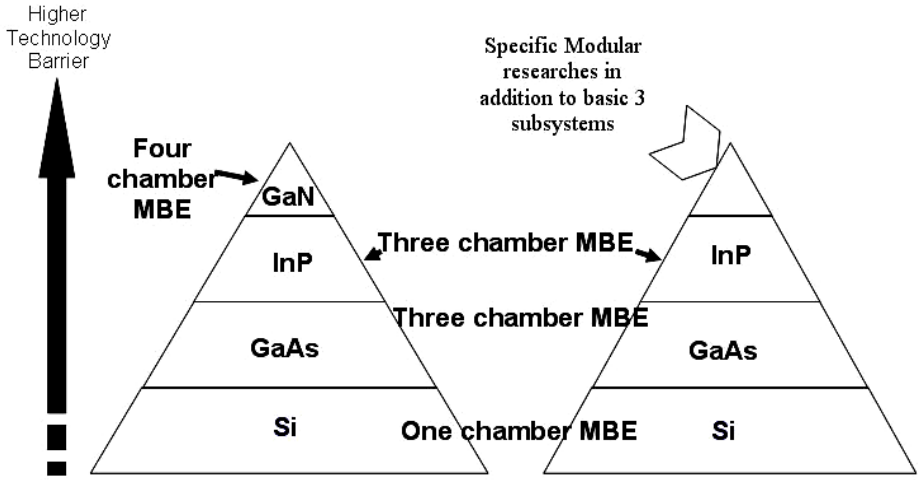

Fig. 3 *– Integration strategy of III-V/Si at IIT Kharagpur [©HPDG]*

GaAs is the best solution for the formation of the middle layer of base pyramid as shown in Fig. 3. It has a high resistivity semi-insulating property that reduces cross talk between devices in MMIC applications. This permits the integration of active (RF) devices, control (logic) devices, transmission lines & passive elements on a single substrate. We utilize the MBE cluster tool technique to vertically integrate on this technology barrier to combine the advantages of a high-frequency, low noise, sub 1 V turn on

voltage InP-based structures while high power, high isolation and possibly high linearity cubic GaN structure and a low-cost high-mechanical-strength GaAs substrate. It may be noted that our research covers wide bandgap (GaN = 3.4 eV) to narrow bandgap (InP = 1.35 eV) through medium bandgap (GaAs, Si etc), thereby covering high performance device for high power, low noise and high linearity between the several bandgap heterostructures.

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