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EFFECTIVE PASSIVATION OF c-Si BY INTRINSIC a-Si:H LAYER FOR HIT SOLAR CELLS

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*The influence of HF solution etching on surface roughness of c-*Si *wafer was investigated using AFM. Ultra thin(*2-3 *nm) intrinsic a-*Si:H *is necessary to achieve high* V_{OC} *and Fill factor, as it effectively passivates the defects on the surface of c-*Si *and increase tunneling probability of minority charge carriers. However, to achieve control over ultra-thin intrinsic a-*Si:H *layer thickness and passivation properties, the films were deposited by Hot-wire CVD. We used tantalum filament and silane (*SiH_4*) as a precursor gas, where as the deposition parameter such as filament temperature temperature was varied. The deposition rate, Dark and Photoconductivity were measured for all the films. The optimized intrinsic a-*Si:H *layer was inserted between p typed doped layers and n type c-Si wafers to fabricate HIT solar cells. The Current-Voltage characteristics were studied to understand the passivation effect of intrinsic layer on c-Si surface. The high saturation current density (*$J_{sat} > 10^{-7}$ *A/cm*^{2}*) and Ideality factor (*$n > 2$*) were observed. We achieved the efficiency of* 3.28 % *with the optimized intrinsic and doped a-*Si:H *layers using HWCVD technique.*

Keywords: *HIT SOLAR CELL, HWCVD, AFM, HF, AMORPHOUS SILICON.*

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1. INTRODUCTION

In 1991, a more advanced a stacked amorphous/crystalline silicon hetero-junction device structure was developed by SANYO Ltd. as the Hetero-junction with Intrinsic Thin-layer (HIT) cell, with a doped a-Si:H(doped)/a-Si:H(undoped)/c-Si structure [1]. It offers low cost alternative to crystalline silicon solar cells. Processing is also simple and requires low temperature (< 200 °C). Due to high potential of this technology presently, the conversion efficiency of standard HIT solar cell has reached a level of 23.0% for a practical size of substrate (100.4 cm^2) with open circuit voltage (V_{OC}): 729 mV, short circuit current (J_{SC}): 39.52 mA/cm^2, fill factor: 80.0 % demonstrated by Sanyo [2]. In HIT solar cells the passivation of c-Si surface and the reduction of a-Si:H/c-Si interface recombination is the most crucial. The abrupt ending of the crystal at the surface leads to defects, which are traps in forbidden band, giving rise to high recombination rate. These are saturated by removal of oxides and impurities on c-Si surface. The losses can be suppressed by a low defect density state at the interface [3]. These defect states can be modified by surface pretreatment of c-Si wafer or passivating defects by depositing ultra-thin intrinsic a-Si:H buffer layer prior to deposition of doped a-Si:H films. This intrinsic a-Si:H has a far lower density of defects than a doped a-Si:H layer. A lower density of mid-gap

trap states reduces the trap-assisted inter-band tunneling-recombination rate across the a-Si:H/c-Si interface, thereby suppressing deleterious saturation current [4], and hence enhances the performance of the cell. The cleaning of c-Si wafer before wafers are introduced into the reactor are very crucial prior to passivating layers are deposited. It is commonly accepted that hydrogenated terminated surface reduces the final defect density states [5]. Hence, wet chemical etching involving aqueous HF solution should be performed just before wafers load into the reactor.

In this work influence of HF solution on bare Si surface is evaluated from the point of view of surface roughness. We used Hot Wire CVD (HWCVD) technique which is a new technique to deposit device quality a-Si:H films. As compared to Plasma Enhance CVD (PECVD) technique it has some technical advantages like the absence of ion bombardment that reduces the damage of c-Si surface [6]. In this paper we present deposition process and charectization of quality intrinsic a-Si:H layer to achieve low deposition rate for HIT solar cell fabrication. We fabricated different HIT solar cells and measured I-V curves under different illuminations in order to show passivation effect of intrinsic a-Si:H layer on c-Si surface.

2. EXPERIMENTAL

The native oxide on n-type c-Si having a resistivity of 4-7 Ohm·cm, orientation of (100) and thickness of 525 μm removed by 2 min dip in 3% HF/Deionized (DI) water solution. Subsequently they are rinsed in DI water to remove fluorine resides on the wafer surface and finally dried by nitrogen flow. All the intrinsic a-Si:H thin films are deposited simultaneously on both substrates glass (Corning 7059) substrate and n-type c-Si. Before deposition of i-layer we cleaned substrates in methanol and DI Water. Substrates were dried using nitrogen flush and immediately loaded into load lock within 2 min. Deposition chambers were backed at least 2 hr before the deposition to get ultra high vacuum (1×10^{-6} mbar). Substrates were pre-treated by atomic hydrogen for 5 sec at the filament temperature 1700 °C and at the same substrate temperature of i-layer deposition. Atomic Force Microscopy (AFM) is used to study the roughness of samples after HF etching and 10 sec deposition of an intrinsic a-Si:H on c-Si substrate. Bare c-Si wafer is taken as a reference. Thicknesses of the films were measured using Dektak Profilometry. The dark conductivity (σ_{dark}) under dark and photoconductivity (σ_{photo}) under 100 mW/cm^2 (1 sun) light at room temperature were measured with coplanar Al electrode.

3. RESULTS AND DISSCUSSION

3.1 Microroughness By AFM

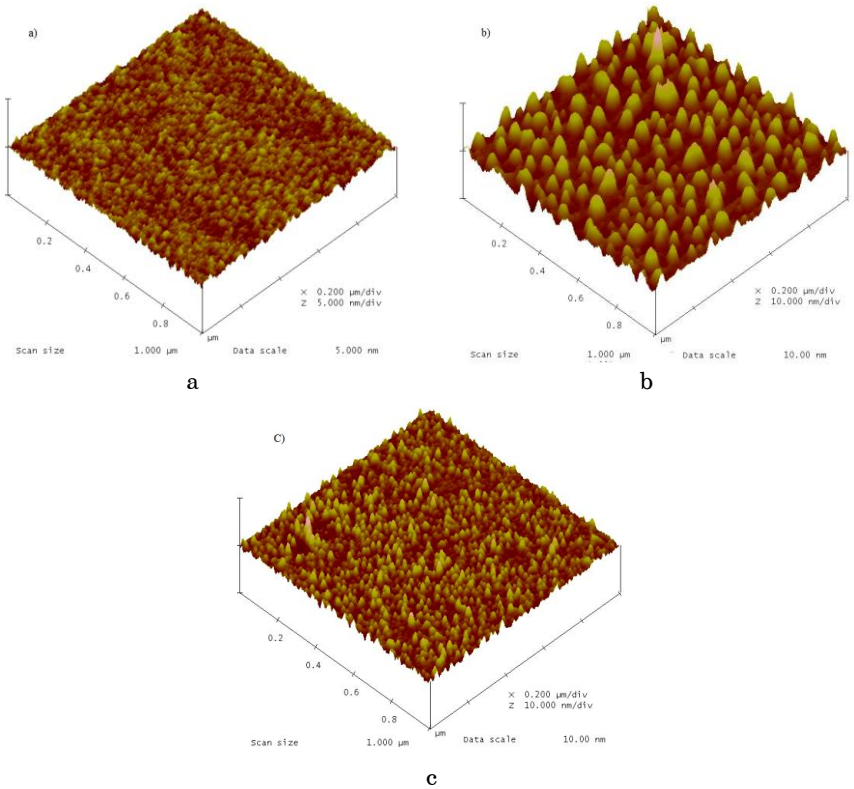
AFM images are shown in the Fig. 1 for the (a) c-Si wafer as a reference sample, (b) the sample treated in HF solutions (c) 10 sec deposited intrinsic a-Si:H layers on c-Si subsequently after HF treatment (process parameter see Table 2). It shows there is a significant increase in the surface microroughness occurred by HF treatment. For this rms surface roughness is about the one order higher than the reference sample (Table 1). Though surface oxide layer removed by HF, it has the disadvantages of increasing the organic contamination from solution and re-growth of an oxide layer on

the surface of a wafer. This re-oxidation diminishes surface passivation and increase the rms surface roughness. The growth of re-oxide may occur on the HF treated c-Si wafer during the sample load into load lock system. It could also be the reason that slight over etching by fluorine component in the solution causes increase in microroughness [7]. Therefore, samples should introduce to a load lock within a small time (1 min) after cleaning.

The surface microroughness after intrinsic a-Si:H layer deposition slightly increase than reference sample but it passivats over etched HF treated the c-Si surface. Therefore, 10 sec intrinsic a-Si:H layer deposition slightly passivates the c-Si surface but this microroughness may produce pits in the c-Si sample which act as deep states, leads the recombination centers and reduces saturation current, hence, performance of HIT solar cells.

Table 1 – *The rms surface roughness of c-Si wafer taken as a reference, 2 min 3 % HF etched surface of c-Si wafer and 10 sec deposition of intrinsic layer at* 1500 °*C on c-Si. Scan area:* 1000 × 1000 nm^2

Treatment	ref	HF	a-Si:H(i)
rms (nm)	0.180	1.014	0.488



a b c

Fig. 1 – *AFM images of bare c-Si waferas a reference* (a), *the 2 min 3 % HF etched c-Si wafer* (b), *10 sec intrinsic a-Si:H layer deposited on c-Si at* T_{Fil} = 1500 °*C* (c)

3.2 Optimization of Intrinsic a-Si:H Layer

In high-efficiency HIT Solar cells, a ultra-thin (3-5 nm) intrinsic a-Si:H layer must be interposed between the base c-Si wafer and the heavily doped a-Si:H emitter. The low deposition rate are desirable in order to control the growth of ultrathin a-Si:H films since high deposition rate leads to disorder and porous material. However, in an order to achieve low deposition rate for a good quality intrinsic layer, the films were deposited on glass (Corning 7059) using silane (SiH_4) as a precursor gas in Hot-Wire CVD chamber. We varied filament temperature from 1500 °C to 1650 °C keeping all other process parameters constant (table 2). All the observed films were amorphous in nature confirmed by Raman spectroscopy.

Table 2 *– Process parameters for intrinsic a-Si:H films*

Substrate Temperature (T_S)	180 ± 10 °C
Filament Temperature(T_F)	1500-1650 °C
Chamber Pressure (P)	10 mtorr
Silane Flow Rate	10 sccm
Substrate to filament distance	6.8 cm
Depositon time	10 min

Table 3 shows deposition rate (R_d) increases from 1 □/sec to 4 □/sec as filament temperature increases from 1500 °C to 1650 °C. The increase in deposition rate is due to temperature-dependent reaction taking place at the filament surface [8]. Therefore, the deposition rate can be controlled by using low filament temperature although that leads to silicide formation on filament surface which reduces the catalytic action of the hot filament.

Table 3 *– Deposition rate (R_d), Photoconductivity (σ_{Photo}), Dark conductivity (σ_{Dark}) and Photosensitivity of intrinsic a-Si:H films as a function of filament temperature (T_{Fil})*

T_{Fil} (°C)	Thickness (Å)	R_d (Å/sec)	σ_{Photo} (Ω-cm)$^{-1}$	σ_{Dark}(Ω-cm)$^{-1}$	Gain
1500	4300	1	3.47×10^{-4}	1.55×10^{-8}	2.25×10^{4}
1550	9500	2.5	1.2×10^{-4}	9.06×10^{-9}	1.21×104
1600	11000	3	1.72×10^{-3}	1.25×10^{-6}	1.37×10^{3}
1650	14400	4	1.67×10^{-4}	1.92×10^{-8}	8.66×10^{3}

The good quality intrinsic a-Si:H layer used as buffer layer in HIT solar cells attributes obtaining a non-defective layer with good passivation properties [9]. We observed low σ_{Dark} values in the range of ~ 10^{-8}-10^{-9} (Ohm·cm)$^{-1}$ indicating less electronically active impurities present in our films. On the other hand, σ_{photo} observed in the order of 10^{-4} (Ohm·cm)$^{-1}$ shows less recombination rate for generated charge carriers in the buck c-Si wafer (See Table 3). The photosensitivity gain taken as the ratio of photoconductivity to dark conductivity observed in the range of 10^3 to 10^4. We achieved the highest photosensitivity gain of $2.55 \cdot 10^4$ and lowest deposition rate of 1 Å/sec at the filament temperature 1500 °C. The variation of photoconductivity, dark conductivity and photosensitivity with filament temperature is shown in Fig. 2.

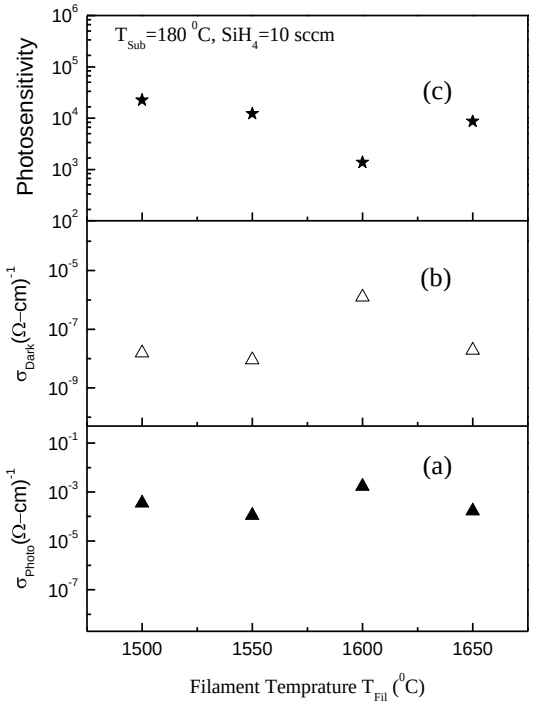


Fig. 2 *– Photoconductivity (σ_{Photo}) (a), Dark conductivity (σ_{Dark}) (b) and Photo-sensitivity of intrinsic a-Si:H films as a function of filament temperature (T_{Fil}) (c)*

3.3 Fabrication Of HIT Solar Cells

As a result of above characterization we choose filament temperature as 1500 °C to deposit good quality intrinsic a-Si:H buffer layer. To study the passivation effect of intrinsic a-Si:H layer on heterojuction diode performance we were fabricated three HIT solar cells as HIT16, HIT17, and HIT18 with different a-Si:H layer deposition conditions (Table 4). I-V characteristics of HIT solar cells were measured under dark and under AM1.5 illuminations conditions. The short circuit current (*Isc*) and open circuit voltage (*Voc*) were taken at the value of $V = 0$ and $I = 0$ respectively. The results in table 5 shows the ideality factor (n) and saturation current density (J_{sat}) obtained from different I-V curves of HIT Solar cells under different illuminations condition. For different curves we got different values of I_{SC} and V_{OC}. We used the following equation to plot the ln(I_{SC}) verses V_{OC} curves. Intercept of this curve gives I_{sat} and slope gives n.

$$V_{OC} = \frac{nKT}{q} \ln\left(\frac{I_{SC}}{I_{sat}}\right), \text{ for } I_{SC} > I_{sat}$$

The HIT16 shows the J_{sat} and n comparatively higher than others. It may due to higher thickness (15 sec) of intrinsic a-Si:H layer which may create for hindrance for tunneling the charge carriers. In case of HIT18 it is claim that

10 sec intrinsic layer passivats the interface a-Si:H/c-Si and increases tunneling probability of charge carrier generated in c-Si bulk material therefore, it shows good ideality factor and saturation current density (Table 5).

Table 4 – *HIT Solar Cells deposition parameters: Deposition pressure* 10 *mtorr were kept constant for all depositions*

Cells	T_{Fil} (°C)		T_{Sub} (°C)		SiH_4:B_2H_6 (sccm)		Deposition time (sec)	
	a-Si:H(i)	a-Si:H(p)	a-Si:H(i)	a-Si:H(p)	a-Si:H(i)	a-Si:H(p)	a-Si:H(i)	a-Si:H(p)
HIT16	1500	1600	180	200	10:0	10:2	15	40
HIT17	1500	1600	180	200	10:0	10:2	10	40
HIT18	1500	1600	180	200	10:0	10:2	10	30

Table 5 – *Saturation current densities (J_{sat}) and ideality factors (n) of the HIT solar cells*

Cells	Cell Area (cm^2)	Efficiency (%)	J_{sat} (A/cm^2)	n
HIT16	2.34	1.01	1.42×10^{-4}	2.96
HIT17	3.88	1.56	6.36×10^{-7}	2.07
HIT18	2.68	3.28	1.36×10^{-8}	1.45

It is observed that thick intrinsic a-Si:H layer reduces performance of cell and increases saturation current density and ideality factor. J-V characteristic of HIT18 cell is shown in 3 below. We achieved efficiency of 3.28% with V_{OC} = 500 mV, J_{SC} = 12.4 mA/cm^2 and Fill Factor = 0.52 with 10 sec intrinsic a-Si:H layer deposition. The comparatively higher V_{OC} of the cell may due to good buffer intrinsic layer and p type a-Si:H doped layer.

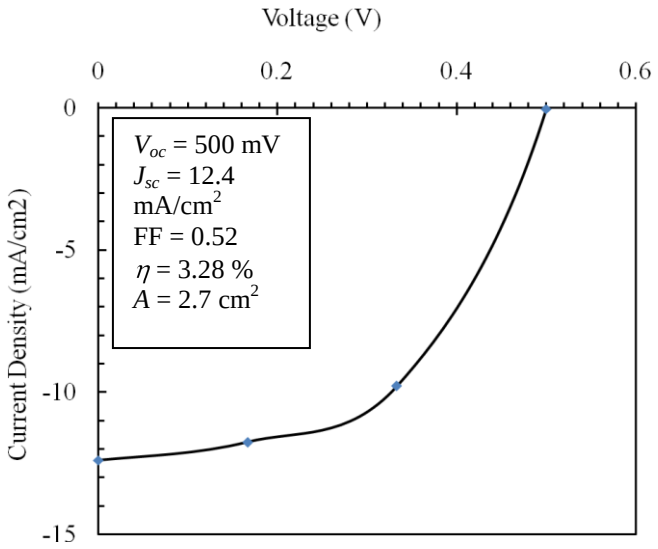


Fig. 3 – *J-V curve of HIT18 solar cell* 10 *sec intrinsic a-Si:H layer deposited at* 1500 °C

4. CONCLUSIONS

The over etching of 3 % HF increases the rms microroughness of c-Si wafer. Further attempts require bringing down roughness of c-Si surface after HF treatment. The rms roughness after intrinsic a-Si:H layer deposited for HIT cell on c-Si shows good passivation properties and can transport charge carriers. It is observed that quality of intrinsic a-Si:H layer is important for reducing recombination at the a-Si:H/c-Si interface in HIT solar cells. An intrinsic a-Si:H layer has been optimized at filament temperature 1500 °C with lowest deposition rate of 1 Å/sec and high photosensitivity of the order of 10^4 by HWCVD technique. For HIT18 the saturation current density $J_{sat} = 1.36 \times 10^{-8}$ A/cm^2 and ideality factor $n = 1.45$ were observed which colligated with c-Si surface passivation by 10 sec intrinsic a-Si:H layer. This result is concerned with AFM microroughness. We achieved 3.3 % efficiency with this intrinsic layer. Further work is necessary to improve performance of our HIT solar cells.

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