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Effect of Gate Length Scaling on Various Performance Parameters in DG-FinFETs: a Simulation Study

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This paper presents a simulation study on the gate length scaling of a double gate (DG) FinFET. To achieve channel lengths smaller than 20 nm, innovative device architectures will be necessary to continue the benefits previously acquired through scaling. In order to obtain desirable control of short channel effects (SCEs), the thickness or the horizontal width of a fin in a FinFET should be less than two-third of its gate length and the semiconductor fin should be thin enough in the channel region to ensure forming fully depleted device. The effect of decreasing gate length (Lg) is to deplete more of the region under the inversion layer, which can be easily visualized if the source and drain are imagined to approach one another. If the channel length L is made too small relative to the depletion regions around the source and drain, the SCEs associated with charge sharing and punch through can become intolerable. Thus, to make L small, the depletion region widths should be made small. This can be done by increasing the substrate doping concentration and decreasing the reverse bias. Drain induced barrier lowering (DIBL) increases as gate length is reduced, even at zero applied drain bias, because the source and drain form pn junction with the body, and have associated built-in depletion layers associated with them that become significant partners in charge balance at short channel lengths, even with no reverse bias applied to increase depletion width. The subthreshold slope increases as the device becomes shorter. In fact, when the device becomes very short, the gate no longer controls the drain current and the device cannot be turned off. This is caused by punch through effect. The subthreshold swing (SS) changes with the drain voltage.

Keywords: DGFinFET, Gate length, Short channel effects, DIBL, Subthreshold swing (SS).

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1. INTRODUCTION

Double gate field effect transistors (DGFETs) are one of the most promising devices which have two gates to control the channel. Its main advantage is improved gate-channel control and reduced SCEs, because the drain field lines are not able to reach the source due to the fact that the gate oxide has a lower dielectric constant than Si (assuming the oxide as SiO_2), and ultrathin body. Because of its greater resilience to SCEs and greater gate-channel control, the physical gate thickness can be increased (compared to planar MOSFETs). In recent years MOSFET devices have been aggressively scaled in combination with a complex design of the channel doping to avoid short channel effects (SCEs). Further scaling beyond the 0.1 μm process generation will be difficult if not impossible due to limitations given by lateral SCEs and gate insulator tunneling [1-6]. Thus it can also bring along reduced leakage currents (gate leakage as well as S/D leakage). SCEs limit the minimum channel length at which an FET is electrically well behaved. As the channel length of a DGFET is reduced, the drain potential begins to strongly influence the channel potential, leading to its inability to shut off the channel current. This SCE is mitigated by use of thin gate oxide and thin depletion depth to shield the channel from the drain. Thus, further reduction of the thickness would lead to unreasonable increase in power.

There are two types of DG MOSFETs: Symmetric (SDG), in which the gates have identical work function (Φ_M, intermediate to N + poly-Si and P + poly-Si work functions) Asymmetric (ADG), in which the gates have different work functions (N + poly-Si for the front gate, P + poly-Si for the back gate, for an n-channel device) [7]. Numerous structures for DG-FETs have been proposed and demonstrated. The non planar DGFET is also known as FinFET as the silicon resembles the dorsal fin of a fish. In this type the current carrying plane is parallel to the wafer and the width is in the vertical direction. The silicon body has been rotated on its edge into a vertical orientation such that only the source and drain regions are placed horizontally about the body, as in a conventional planar FET. Most important Features of a FinFET are:

1. Ultra thin Si fin for suppression of short channel effects.
2. Raised source/drain to reduce parasitic resistance and improve current drive.
3. Symmetric gates yield great performance, but can built asymmetric gates that target V_T.
4. The main advantage of the FinFET is the ability to drastically reduce the short channel effect. In spite of double gate structure, the FinFET is closed to its root, the conventional MOSFET in layout and fabrication.
5. Gate last process with low T, high k gate dielectrics.

In a typical double gate FinFET, a gate dielectric layer and a gate conductor are located upon each of the two semiconductor fin sidewalls facing each other. A spacer material of substantial thickness is located between the top surface of the fin and the top portion of an inverted U-shaped gate electrode such that the top surface of the fin is not controlled directly by the portion of the gate electrode above it. Device structures

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based on silicon-on-insulator (SOI) technology have emerged as an effective means of extending MOS scaling beyond bulk limits for mainstream highperformance or low-power applications. Partially depleted (PD) SOI was the first SOI technology introduced for high-performance microprocessor applications. The ultra-thin-body fully depleted (FD) SOI and the nonplanar FinFET device structures promise to be the potential "future" technology of choice. In SOI technology, an insulator SiO_2, isolates the bulk from the substrate. An extremely shallow junction is formed due to the depth limitation put by the insulator. SOI process is used to manufacture FinFETs.

2. DEVICE STRUCTURE AND SIMULATIONS

Like a traditional MOSFET, the FinFET is composed of a channel, a source, a drain, and a gate. It is more versatile than traditional single-gate field effect transistors because it has two gates that can be controlled independently. Usually, the second gate of the FinFET is used to dynamically control the threshold voltage of the first gate in order to improve circuit performance and reduce leakage power. However, we can also utilize the second gate to implement circuits with fewer transistors.

FinFETs are designed to use multiple fins to achieve larger channel widths. Fig. 1 shows the FinFET structure with various dimensions marked [8]. Source/Drain pads connect the fins in parallel. As the number of fins is increased, the current through the device increases. For example, a five fin device conducts five times more current than single fin device.

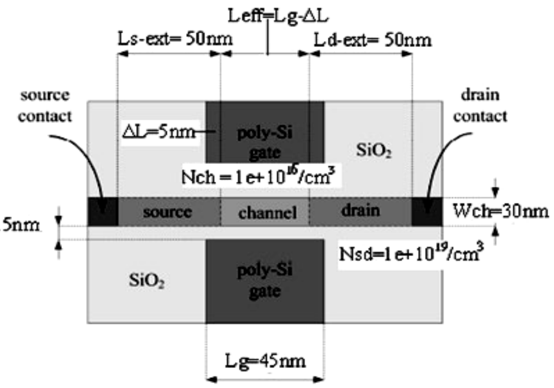

Fig. 1 – FinFET structure, with dimensions marked [20]

A gate can also be fabricated at the top of the fin (in a triple gate FET). The oxide above the fin can be made thick enough so that the gate above the fin is as good as not being present. It should be noted that the gate length L_g of a FinFET is similar as that in a conventional planar FET, the device width W is quite different. W can be defined as:

$$W = 2\,H_{fin} + T_{fin},$$

where H_{fin} and T_{fin} are the fin height and thickness respectively.

W as defined above is the width of the gate region that is in touch with the channel in the fin. This definition of device width is for a triple gate FinFET. If the gate above the fin is absent/ ineffective, then the Tfin term in the above definition is taken out. Increasing W also increases the Ion, which is a desirable feature. However, there is a definite range (in relation to T_{fin}) beyond which H_{fin} should not be increased so as to avoid SCEs [1-2]. Design parameters used for simulating a double gate FinFET are shown in Table 1.

Table 1 – Design Parameters used for DG FinFET Simulation

Design	Value used
L_g	10 – 45 nm
W_{ch}	30 nm
T_{ox}	2.5 nm
Ns/d	1×10^{19} cm^{-3}
N_{ch}	1×10^{16} cm^{-3}
Ls/d	50 nm
Φ	4.6 eV

In order to examine the various simulation results, this study has been performed using the multigate FET (*MuGFET)* online modeling software developed at Purdue University available through nanoHUB (www.nanohub.org), funded by the National Science Foundation's (NSF) Network for Computational Nanotechnology (NCN) [9]. MuGFET is a simulation tool for nano-scale multi-gate FET structure and can use either PROPHET or PADRE. It provides self-consistent solutions to the Poisson's and drift-diffusion equations. At the nanometer scale, quantum transport approaches are based on a full 3D Poisson-Schrodinger solution [10]. However, for devices that are 10 nm or larger, semi-classical approaches can provide some significant insight. For device domains 30 nm or larger, quantum approaches may not contain enough physics of scattering and dephasing. Therefore, there are some advantages in using classical simulation approaches over quantum simulation approaches for certain classes of device regimes. Drift-diffusion simulations are significantly faster than quantum ballistic simulations and fairly well fitted to experimental results [11].

3. RESULTS AND DISCUSSIONS

In this section, we have discussed the effect of the gate length scaling on the various performance parameters and characteristics of the FinFET. The whole motive behind these simulations is aimed at understanding the physics of DG FinFET structure through various simulation results obtained by varying various process and design parameters of original DG FinFET structure. The performance parameters studied are Threshold voltage (Vth), Subthreshold Swing (SS), Drain Induced Barrier Lowering (DIBL), On current (I_{on}), Off current (I_{off}), on/off current ratio ($I_{on/off}$), Transconductance (gm) and I-V Characteristics.

3.1 Effect of Gate Length (L_g) on Threshold Voltage (V_{Th})

As the channel length L is reduced, keeping all other parameters constant, the peak of the surface potential is reduced and is constant only over a small fraction of the channel length L. Since the peak potential is reduced, the current will increase. If V_{ds} is increased, this peak is further reduced and the region of constant potential is also reduced. From these observations the SCEs has been attributed to the penetration of the junction electric fields into the channel region, causing barrier lowering, which in turn leads to V_{th} reduction. This reduction in V_{th} depends linearly on V_{ds}. Further, as the channel length L reduces, the gate controls less charge by an amount ΔQi, resulting in a decrease in V_{th}. Fig. 2 depicts threshold voltage variations with the gate length. The distance between drain and source reduces with the gate-length and hence the channel potential becomes more pronounced to the drain electric field. So, the gate potential required to invert the channel is reduced because of the drain electric field encroachment on the channel region increases with decreased gate-length. Fig. 2 suggests that the V_{th} decreases more rapidly with the L_g from to 55 nm to 30 nm and gradually decreases with the L_g from 30 nm to 20 nm. The reason is that the barrier from source to channel is lowered as L_g decreases. Thus, we can say that V_{th} is a function of L_g and V_{ds}. As we have seen in the graph at $V_{ds} = 1V$, V_{th} has lower value as compared to $V_{ds} = 0.05V$.

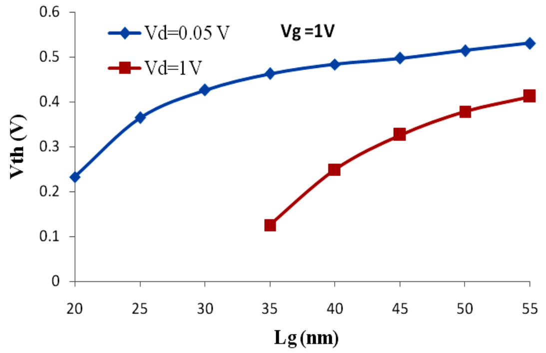

Fig. 2 – V_{th} variations w.r.t. gate length (L_g)

3.2 Effect of Gate Length (L_g) on DIBL

DIBL is a strong effect for short channel devices operated near threshold. Fig. 3 depicts DIBL variations with the gate-length (L_g). DIBL increases very sharply with decreased gate-length since the drain electric field encroachment on channel region increases at shorter gate-lengths. Therefore, we can say that lower the channel length or short gate length, higher the DIBL.

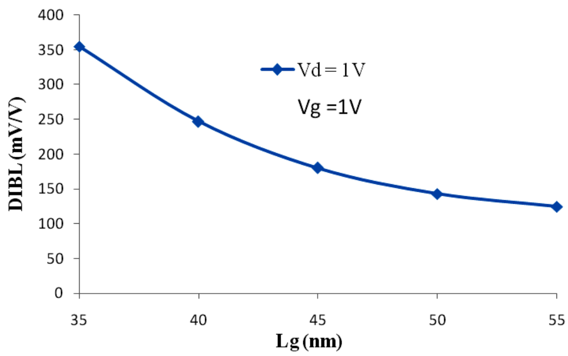

Fig. 3 – DIBL variation w.r.t. gate length (L_g)

3.3 Effect of Gate Length (L_g) on I_{on}, I_{off} and ($I_{on/off}$) ratio

In general, a logic transistor operates as a switch that toggles between an "on" state and an "off" state. For fast switching, a higher on current (I_{on}) is desired. To limit standby power consumption, the off current (I_{off}) must be minimized. It is in terms of I_{on} and I_{off} that the suitability of a transistor for logic should be assessed. I_{on} is determined by the product of the sheet electron concentration and the electron injection velocity, v_{inj}, at the "virtual source", the location on the channel that presents the highest energy barrier in the conduction band. This is the bottleneck to electron flow. Sheet carrier concentration also affects I_{on}. Concerns have been expressed about the limitation that a low effective mass imposes on the maximum sheet electron concentration that can be obtained. $I_{on/off}$ ratio gives better switching characteristics regardless of the value of the threshold voltage. It also requires low static power consumption which results from the better $I_{on/off}$ ratio of the device. But I_{off} is just as important as I_{on}. I_{off} is set by the subthreshold swing, SS, which quantifies the sharpness of the drop of the drain current below threshold. An important goal of scaling is to maximize I_{on} while maintaining an acceptable I_{off}. When discussing the suitability of different device technologies for logic applications, both values should be considered. A simple way is to refer to the I_{on} that can be obtained for a set value of I_{off} at a certain V_{DD}. In FinFET structure, the gate wraps around the channel from two directions for enhancing the channel conductivity and reducing the leakage current (I_{off}). Fig. 3 and 4 shows effect of L_g on I_{on} and I_{off} and Fig. 5 shows effect of L_g on $I_{on/off}$ ratio. Beyond $L_g = 35$ nm at $V_d = 0.05\ V$ and $1\ V$, value of $I_{on/off}$ going to be highly increased but below $L_g = 35$ nm, it gradually increases. As T_{body} is reduced, leakage paths far from the gate are eliminated. Off state leakage current thus increases and SCEs are minimized at small gate lengths. At $L_g = 55$ nm, $I_{on/off}$ attains maximum value.

3.4 Effect of Gate length (L_g) on Subthreshold Swing (SS)

The thinner the channel, the closer the subthreshold swing approaches its ideal value of ~ 60 mV per decade (that is, the current increases by a factor of 10 for every 60 mV increase in gate voltage) at room temperature. Interface states are electronic states that arise from disruptions to the ideal bonding structure of a semiconductor at its interface with a dielectric.

They affect device operation in several ways. Interface states below the edge of the conduction band increase the subthreshold swing, whereas those inside the conduction band trap electrons. Both effects reduce I_{on} for a given I_{off}. Interface states can also shift the threshold voltage, degrade the channel mobility and be a source of instability. As shown in Fig. 7, subthreshold swing also increases with decreased gate-length. The gate now has less control over channel in subthreshold region because of the channel barrier potential is now controlled by the drain potential also.

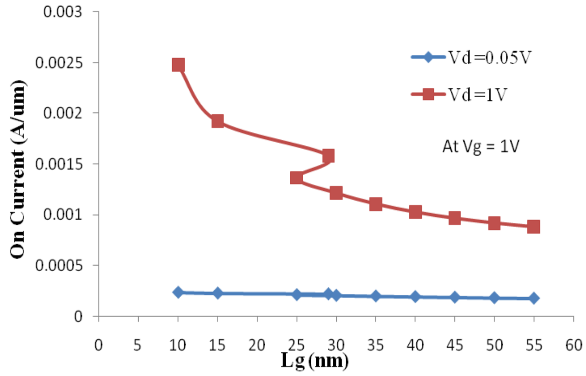

Fig. 4 – I_{on} variations w.r.t. gate length (L_g)

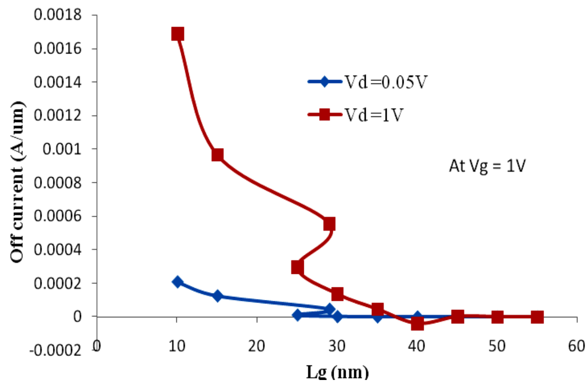

Fig. 5 – I_{off} variations w. r. t. gate length (L_g)

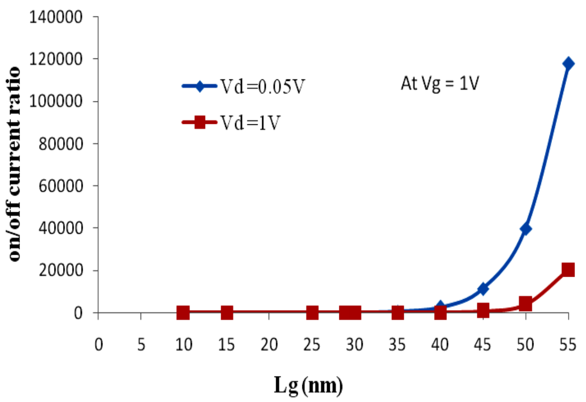

Fig. 6 – On/off current ratio variations w.r.t. gate length (L_g)

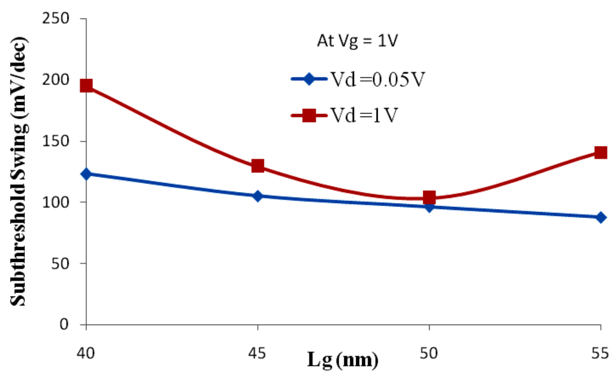

Fig. 7 – SS variation w.r.t. gate length (L_g)

3.5 Effect of gate length (L_g) on transconductance (gm)

Transconductance "gm" is an important parameter for a device. A large value of transconductance is always desired to obtain a high current handling capability with low gate derive voltage for achieving high frequency response. Fig. 8 and 9 shows transconductance (gm) variations. At $V_d = 0.05$ V, "gm" shows highest peak at $L_g = 45$ nm and at $V_d = 1V$, again show gm at high peak when $L_g = 45$ nm.

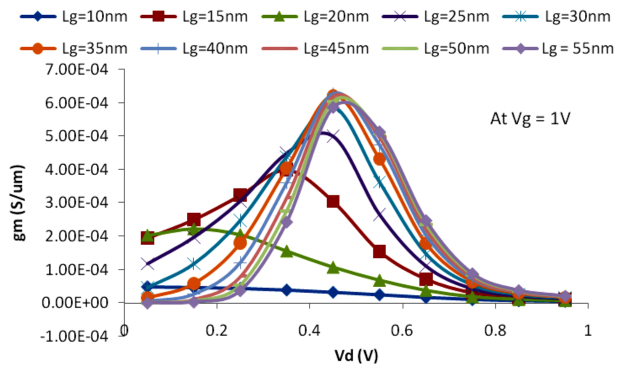

Fig. 8 – Transconductance variations w. r. t. various gate lengths at $V_d = 0.05$ V

3.6 Effect of gate length (L_g) on I-V Characteristics

Fig. 10 and 11 shows transfer characteristics of device at two different drain voltages i.e. $V_d = 0.05$V at 1V. At $L_g = 10$ nm, there is maximum drain current in both the drain voltages. I_d goes on increasing with the reduction of gate length.

4. CONCLUSIONS

Various simulation results for DGFinFET structure have been presented and the effect of scaling down L_g have been studied in terms of various performance parameters such as V_{th}, DIBL, SS, I_{on}, I_{off} and on/off current ratio. By comparing important results and characteristics from the proposed FinET, the following conclusions have been drawn:

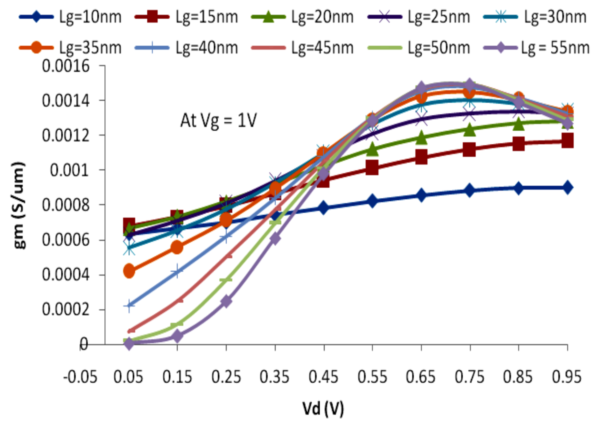

Fig. 9 – Transconductance variations w. r. t. various gate lengths at $V_d = 1V$

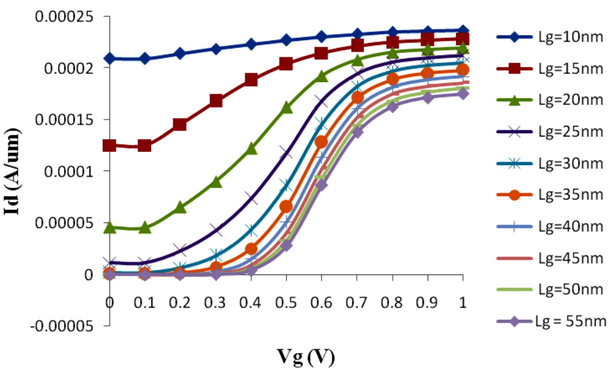

Fig. 10 – I-V Characteristics w.r.t. various gate lengths at $V_d = 0.05\ V$

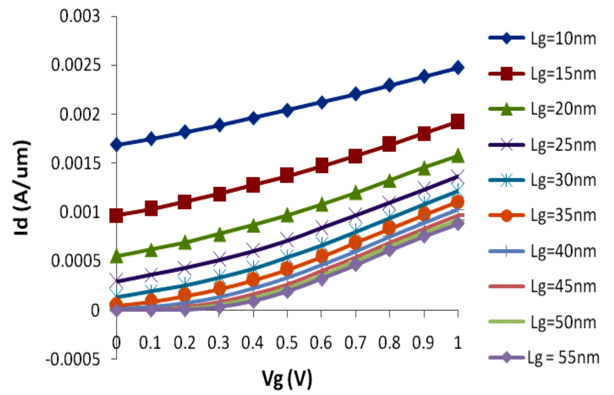

Fig. 11 – I-V Characteristics w.r.t. various gate lengths at $V_d = 1V$

1. Threshold Voltage (V_{th})

Low value of V_{th} decreases the vertical electric field, which increases carrier mobility. V_{th} increases with increase in L_g. Charge sharing models account for the reduction in V_{th} through the sharing of the channel depletion region between the gate and source-drain junctions.

2. Drain Induced Barrier Lowering (DIBL)

Drain induced barrier lowering increases as channel length is reduced, even at zero applied drain bias, because the source and drain form pn junction with the body, and so have associated built-in depletion layers associated with them that become significant partners in charge balance at short channel lengths, even with no reverse bias applied to increase depletion width. Higher V_{ds}, increases the SCEs due to DIBL effect.

3. Subthreshold Swing (SS)

A device with ideal subthreshold slope is the optimal device for subthreshold operation due to its smaller gate capacitance as well as the larger operating current for a given off-current. The near-ideal subthreshold behavior of FinFET indicates the potential application of FinFET on the ultralow-power scheme. For SS < 100 can be obtained when $W_{ch} < 25$ nm, and $N_{s/d} = 1 \times 10^{16}\,/\mathrm{cm}^{-3}$ and $1 \times 10^{17}\,/\mathrm{cm}^{-3}$. Subthreshold slope is an important parameter of the subthreshold region. This is the gate voltage swing required to reduce the current from its "on" value to an acceptable "off" value. This gate voltage swing also called subthreshold slope "SS" is defined as the change in the gate voltage V_{gs} required to reduce subthreshold current I_{ds} by one decade. For a device to have good tur-on characteristics SS should be as small as possible. SS lie in the range of 60 – 180 mV/dec. Use of substrate bias can improve subthreshold turn–off. The subthreshold slope increases as the device becomes shorter. In fact, when the device becomes very short, the gate no longer controls the drain current and the device cannot be turned off. This is caused by punch through effect.

4. Ion/off ratio

This ratio increases due to increase in L_g. Thus for deep submicron devices, the larger device dimension brings about the larger off-leakage current ratio, the size of the FinFET must be made as small as possible. This, however, changes the internal operating physics of FinFETs. Phenomenon's that are negligible in large devices become limiting factors as device geometries are reduced. It can be seen that the DGFinFET presents better switching characteristics regardless of the value of the threshold voltage. The $I_{on/off}$ ratio advantage of the DGFinFET becomes smaller as the threshold voltage is reduced, but it is still ten times larger than in the bulk transistor for a threshold voltage of 0.2V.

5. Transconductance

Transconductance "gm" in the linear region is independent of V_{gs}, while in reality it does depends on V_{gs} due to the mobility degradation factor. Interestingly gm peaks at 30 nm of Si fin width. This is because that while a thinner body increases the parasitic resistance; it also can increase the mobility and reduce the charge centroid, resulting in an optimum Si fin width or body thickness. Mobility degradation causes a decrease of the slope of the transfer characteristics. The effect of gate length scaling on various performance parameters has been shown below in Table 2.

Table 2 – Effect of L_g on various Performance Parameters

	Gate length, "L_g" (nm)					
At $V_d = 1V$	30	35	40	45	50	55
DIBL(mV/V)	0	354.8026	246.9657	179.9427	143.3106	124.8303
$I_{on/off}$	8.9379	23.97962	104.4061	644.1705	3955.264	117933.4
SS(mV/dec)			194.53	129.12	103.32	140.79
V_{th} (V)		0.12	0.24	0.32	0.37	0.41
I_{off} (A/µm)	0.0012	0.001106	0.001026	0.000965	0.000918	0.000881
I_{on} (A/ µm)	0.00014	4.61×10^{-5}	-4.00×10^{-5}	1.50×10^{-6}	2.32×10^{-7}	4.32×10^{-8}

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