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Influence of Impact Ionization Process on Current-Voltage Characteristics of Nanoscale Silicon *n*-Channel MOSFET

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The current-voltage characteristics of nanoscale silicon n-channel MOSFET with 50 nm channel length are calculated in the present study. Both the electron and hole transport are simulated by means of the ensemble Monte Carlo method. The importance of electron impact ionization process in the transistor channel for drain biases higher than 1 V is shown.

Keywords: Silicon MOSFET, Monte Carlo simulation, Impact ionization.

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1. INTRODUCTION

One of the most promising methods of charge transport simulation in semiconductor devices is the ensemble Monte Carlo method [1, 2]. The Monte Carlo procedure makes possible the simulation of nanoscale devices including all the dominant mechanisms of charge carrier scattering for both a three-dimensional and low-dimensional systems [3-5] with account of the different subtle physical effects [6-8]. The simulation can be done in a self-consistent manner [9, 10].

It is known that in numerical simulations of integrated circuit elements with the reduction of their dimensions, particularly MOSFETs, an account of the impact ionization process is essential. The latter is caused by the fact that the rate of impact ionization in such elements can be comparable or even greater than the rates of other considered scattering processes because of the presence of high electric field strengths [11].

The main purpose of this study is the estimation of impact ionization influence on the current-voltage characteristics of deep submicron (nanoscale) silicon n-channel MOSFET with 50 nm channel length.

2. SIMULATION MODEL

The considered MOSFET structure is presented in Fig. 1. MOSFET dimensions are denoted in the same figure. Other parameters used in the simulation are the following: gate oxide thickness is 10 nm, acceptor doping levels of the channel and substrate are equal to $5 \cdot 10^{23}$ m^{-3} and 10^{24} m^{-3} respectively, donor doping level of the source and drain regions is equal to 10^{25} m^{-3}. The calculations are performed for the room temperature $T = 300$ K.

Electron transport simulation in silicon conduction band is performed in the framework of effective mass approximation and includes X and L valleys with account of the nonparabolicity in the dispersion relation. Electron scattering processes are intravalley and intervalley scattering by phonons, ionized impurity scattering, plasmon scattering and impact ionization [12-14]. Hole transport in the valence band is simulated in the effective mass approximation in heavy, light and split-off bands. The scatterers for holes are phonons and ionized impurities. Nonparabolicity and anisotropy are taken into account [15-17].

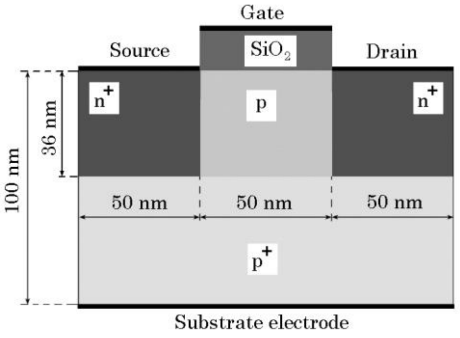

Fig. 1 – The cross-section of the simulated silicon MOSFET

Both the electrostatic potential and electric field strength are found via the solution of a corresponding two-dimensional Poisson equation which is self-consistently incorporated into the Monte Carlo transport simulation. The source, drain and substrate electrodes are modeled as ideal ohmic contacts. The metal gate is supposed to be aluminum. The boundary conditions for the Poisson equation include Dirichlet conditions for metal contacts and Neumann conditions for the rest boundaries.

3. RESULTS OF CALCULATION

To ascertain the influence of impact ionization process on current-voltage characteristics of the nanoscale n-channel MOSFET the process was included into Monte-Carlo simulation as additional scattering mechanism. In the framework of Keldysh impact ionization model [18] its scattering rate $W_{II}(E)$ is expressed by so-called Keldysh formula with given threshold energy E_{th}

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$$W_{\mathrm{II}}(E) = AW_{ph}(E_{th})\left(\frac{E-E_{th}}{E_{th}}\right)^2,$$

where E is electron energy, A is a fitting parameter, $W_{ph}(E_{th})$ is the total electron-phonon scattering rate at the energy equal to E_{th}. Thus the model has two fitting parameters A and E_{th} with $E_{th} = 1.2$ eV for "soft" and $E_{th} = 1.8$ eV for "hard" thresholds [19].

The effect of impact ionization process on some characteristics of a deep submicron MOSFET for both "soft" and "hard" threshold energy models was studied, particularly, in [20] but holes were treated in the quasi-equilibrium approximation. In the present simulation we used "soft" threshold model with $A = 0.38$ [11, 19]. The dependence of the drain current I_D versus the drain voltage V_D for several gate biases V_G for simulated MOSFET are presented in Fig. 2. Solid curves represent the results with the inclusion of impact ionization process, and dashed curves – neglecting the latter process. As it can be seen in the figure the sufficient influence of impact ionization process on the drain current is observed for drain voltages higher than 1 V. The results prove the necessity of inclusion of the process into simulation since for higher drain biases the latter can cause a sufficient degradation of MOSFET's current-voltage characteristics.

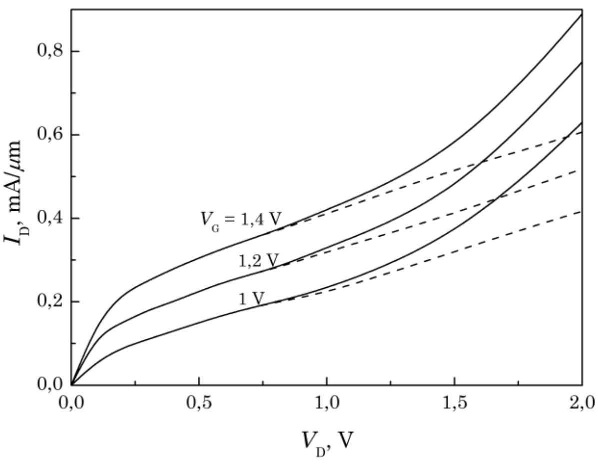

Fig. 2 – The current-voltage characteristics of the simulated MOSFET

4. CONCLUSION

The dependencies of the drain current versus the drain voltage for nanoscale n-channel silicon MOSFET with 50 nm channel length have been calculated with account of the electron impact ionization process. Importance of inclusion of the latter process into current-voltage characteristics calculation has been shown.

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