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An Analytical Universal Model for Symmetric Double Gate Junctionless Transistors

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An analytical surface potential based universal model for the drain current voltage characteristics of Symmetric Double gate (DG) junctionless field effect transistors is presented. This novel universal model is valid for all operating regions from depletion to inversion regions of operations. The primary conduction mechanism is governed by the bulk current where the channel becomes fully depleted in turning it off. This model has been validated by using TCAD device simulating software. The comparison shows high accuracy of the proposed model.

Keywords: Double Gate (DG) junctionless MOSFET, Drain current model, Surface potential, Semiconductor device modelling, Threshold voltage variation, TCAD Simulation.

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1. INTRODUCTION

In the recent years, the assets of junction less transistors have emerged as a promising candidature for stringent demands that has been arriving due to the shrinking of device dimensions in accordance to Moore's rule. Unlike conventional MOSFETs, junctions less transistor do not require any junctions. The source, drain and channel are uniformly doped with homogeneous doping polarity. It exhibits many advantages [3]-[6], such as the simplified flexible fabrication process, nearly ideal sub threshold slope, high ON-OFF-current ratio, low S/D series resistance and small drain-induced barrier lowering. Also, the JL transistor shows many interesting characteristics, like conductance oscillations at low temperature [7] and high temperature behaviour [2]. Recently the effects of Surface Roughness and Impurity Scattering in Double-Gate Junctionless Transistors has also been studied [8].

To understand the underlying physics, device characteristics and to use in circuit simulators an analytical compact current-voltage models are needed. An analytic model for DG-JLFETs has been proposed [9], in addition, a hybrid model has been proposed for DG-JLFETs [11]; but the hybrid approach may also show convergence problems [10]. To overcome these difficulties a model is needed which can continuously cover all operation regions. The Pao-Sah integral [12], which is based on Poisson's and current continuity equations and using gradual channel approximation can be used to describe all regions of operation as it includes both the drift and diffusion current components. Only a few studies have been done to develop a surface-potential-based compact model for the JL DGFET valid in all regions, which is more accurate in describing the transistor behaviour and also to use in the compact modelling applications.

2. STRUCTURE OF JL TRANSISTOR

The primary conduction mechanism in a JLFET depends on the bulk current and not on the surface; moreover, in turning it off, the channel needs to be fully depleted. Utilizing a single gate, it is rather difficult to fully deplete the channel, and acceptable threshold voltages are also difficult to obtain under such a condition. Therefore, a double-gate (DG) structure is a promising candidate for JLFETs due to its good electrostatic control of the channel [9].

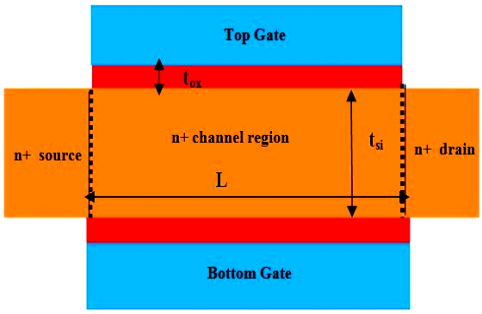

Fig. 1 – Schematic diagram of JLFET

We assume a JL DGMOSFET with channel length L, silicon thickness t_{Si}, oxide thickness t_{ox}, and a uniform impurity concentration N_{si} within the channel and S/D regions. The schematic diagram of a symmetric JL DGFET is shown in Fig. 1.

3. WORKING PRINCIPLE OF JL TRANSISTOR

A transversal view of a DG-JLFET with corresponding schematic band diagrams [1] for different gate voltages is depicted in Fig. 2. Both p+ polysilicon gates have the same work function, and the same voltage is also applied to each gate. The electron quasi-Fermi level of the source-drain is taken as a reference for the other energy levels. The work function difference between the gate and the channel is approximately given as $E_g/2 + qv_T \ln(N_{si}/n_i)$, where E_g is the band gap of silicon, v_T is the thermal voltage which is given as (kT/q), N_{si} is the doping concentration of the channel, and n_i is the intrinsic carrier density. When the gate voltage is below the threshold voltage, V_{TH}, the channel gets fully depleted and the device is in a sub-threshold state. As the gate voltage increases gradually and becomes equal to V_{TH}, the channel gets partially depleted and so current flows through the centre of channel by bulk condition mechanism. When the gate voltage equals the flat-band voltage, a complete neu-

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tral channel takes form and current can flow through the entire channel [1]. At a gate voltage larger than V_{FB}, the mobile carrier (electrons in NMOS) density is increased at the surfaces, and the surface current conduction is governed by the mobile carriers that accumulate at the channel interface. This way, in the linear and sub threshold regions, the DG-JLFET current mechanism is primarily composed of the bulk current. In contrast, electrons in conventional inversion-mode DGFETs are distinctively confined near the interface (surface inversion) in the linear region producing the surface current, whereas they are concentrated at the centre of the channel (volume inversion) in the sub threshold region.

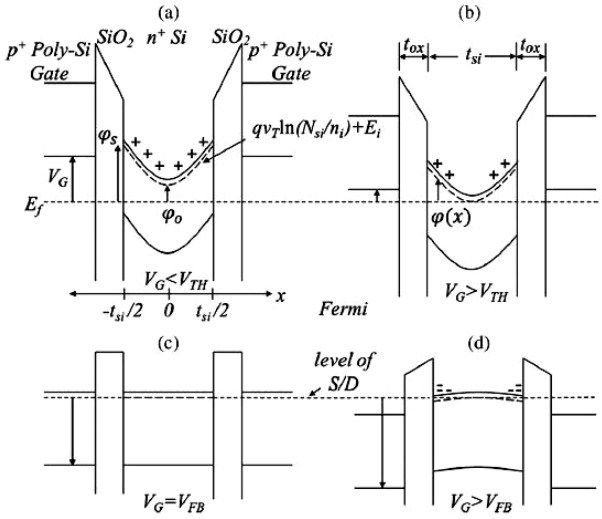

Fig. 2 – Schematic band diagrams for a symmetric DG-JLFET. (a) Fully depleted and downwardly bent channel in the sub threshold mode. Partially depleted and downwardly bent channel in the bulk current mode. (c) Flattened channel in the flat band mode. (d) Upwardly bent channel in the accumulation [2]

4. POTENTIAL BASED MODELING OF DG JLFET

To obtain an analytical expression, we assume the channel potential by a parabolic function as

$$\phi(x) = \phi_0 + \alpha x + \beta x^2 \tag{1}$$

Where 'β' is a constant which is to be determined by boundary conditions and φ_0 is the potential at the centre of the channel. The boundary conditions can be obtained as

$$\varepsilon_{ox}\frac{V_g - V_{fb} - \varphi_{s1}}{t_{ox}} = -\varepsilon_{si}\frac{d\varphi}{dx}\Big|_{x=-\frac{t_{si}}{2}} = \beta\varepsilon_{si}t_{si} \tag{2}$$

And

$$\varepsilon_{ox}\frac{V_g - V_{fb} - \varphi_{s2}}{t_{ox}} = \varepsilon_{si}\frac{d\varphi}{dx}\Big|_{x=\frac{t_{si}}{2}} = \beta\varepsilon_{si}t_{si} \tag{2'}$$

Where φ_{s1} and φ_{s2} are the surface potential of the front and back gate respectively, ε_{ox} is the oxide permittivity, ε_{si} is the silicon permittivity and t_{ox} is the oxide thickness. Solving (1) and (2) and assuming fully symmetric case i.e. without considering any form of asymmetry as discussed in [13, 14] the surface potential we can consider as $\varphi_{s1} = \varphi_{s2} = \varphi_s$ for which $\alpha = 0$ and we get the value of β as

$$\beta = \frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}t_{si}}(V_g - V_{fb} - \varphi_s) \tag{3}$$

So putting the value of β in (1) we can get the potential profile once φ_0 is known.

4.1 Derivation of the Potential (φ_s), (φ_0)

According to the classical Boltzmann statistics, Poisson's equation in the silicon body can be written as

$$\frac{d^2\varphi(x)}{dx^2} = \frac{qN_{si}}{\varepsilon_{si}}[e^{(\varphi(x)-V)/v_t} - 1] \tag{4}$$

Where $\varphi(x)$ is the channel potential and V is the electron quasi-Fermi potential. Now using (1), (4) and integrating it once from the limit $-t_{si}/2$ to $+t_{si}/2$ we get

$$\frac{d\varphi}{dx} = \frac{qN_{si}}{\varepsilon_{si}}\left(\sqrt{\frac{\Pi v_t}{\beta}}e^{\frac{\varphi_0 - V}{v_t}} - t_{si}\right) \tag{5}$$

Considering β/v_t is equal to or greater than one and for which the error function tends to be unity which is always valid, except when the applied gate voltage is approximately equal to the flatband voltage.

From (2) and (5) we have

$$\frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}}(V_g - V_{fb} - \varphi_s) = \frac{qN_{si}}{\varepsilon_{si}}\left(\sqrt{\frac{\Pi v_t}{\beta}}e^{\frac{\varphi_0 - V}{v_t}} - t_{si}\right) \tag{6}$$

Above equation can be solved to get the expression for surface potential as

$$\varphi_s = V_g - V_{fb} + \frac{qN_{si}t_{ox}t_{si}}{\varepsilon_{ox}} - \frac{qN_{si}t_{ox}\sqrt{\Pi v_t}e^{\frac{\varphi_0 - V}{v_t}}}{\varepsilon_{ox}\sqrt{\beta}} \tag{7}$$

Using Gauss's law and (2) we can write the total space charge density Q_s as

$$Q_s = 2\varepsilon_{si}\frac{d\varphi}{dx}\Big|_{x=\pm\frac{t_{si}}{2}} = -2c_{ox}(V_g - V_{fb} - \varphi_s) \tag{8}$$

Thus the mobile charge density Q_m can be calculated as

$$Q_m = Q_s - Q_f = -2c_{ox}(V_g - V_{fb} - \varphi_s) - qN_{si}t_{si} \tag{9}$$

Where $Q_f = qN_{si}t_{si}$ is the fixed charge density.

The applied gate voltage V_g will be utilized in developing the surface potential φ_s along with the drop across the oxide layer φ_{ox} and flatband voltages V_{fb} thus we can write

$$V_g = V_{fb} + \varphi_s + \varphi_{ox}$$

Or

$$V_g = V_{fb} + qN_{si}x^2/2\varepsilon_{si} + qN_{si}xt_{ox}/\varepsilon_{ox} \tag{10}$$

Thus the value of threshold voltage can be found by putting $x = t_{si}/2$ giving

$$V_{th} = V_{FB} - qN_{si}t_{si}^2/8\varepsilon_{si} - qN_{si}t_{si}t_{ox}/2\varepsilon_{ox} \tag{11}$$

The surface potential φ_s and the potential at the centre of the channel φ_0 can be correlated [2] as

$$\varphi_0 - \varphi_s = \frac{t_{si}}{8\varepsilon_{si}}(Q_m + qN_{si}t_{si}) \quad (12)$$

Equations (7) and (12) form a self-consistent equation that can be used to determine φ_s and φ_0.

5. POTENTIAL BASED UNIVERSAL DRAIN CURRENT MODEL

Making use of the gradual-channel approximation and then integrating $I_{DS}dy$ from the source to the drain, we can express the Pao-Sah integral as

$$\begin{aligned} I_{DS} &= -\mu\frac{W}{L}\int_0^{V_{DS}} Q_m dV \\ &= \mu\frac{W}{L}\int_0^{V_{DS}} [\frac{2\varepsilon_{ox}}{t_{ox}}(V_g - V_{fb} - \varphi_s) + qN_{si}t_{si}]dV \end{aligned} \quad (13)$$

This gives new universal drain current model which is valid for all regions of operations.

$$\begin{aligned} I_{DS} &= \mu\frac{W}{L}[(\varphi_{s0} - \varphi_{sL})\{qN_{si}t_{si} + \\ &+ \frac{2\varepsilon_{ox}}{t_{ox}}(V_g - V_{fb} + (\frac{\varphi_{s0} + \varphi_{sL}}{2}))\}] \end{aligned} \quad (14)$$

Where φ_{s0} and φ_{sL} are the values of φ_s at $V = 0$ and $V = V_{ds}$ respectively

6. RESULTS AND DISCUSSION

To confirm the proposed model, a numerical simulation using 2-D SILVACO has been carried out. Fig. 4 shows the device structure in SILVACO. The Shockley Read Hall Recombination model is used, which accounts for the field-dependence and doping effect. The Fermi-Dirac carrier statistics, along with band gap narrowing models, is used in the simulation. Throughout the simulations, the length of the channel and the width of the device are equal to 1 μm. In order to neglect the parasitic resistance effects, source and drain lengths are assumed to be very small. The parameters and values used for SILVACO simulation are kept the same as those which are used in analytical modelling. The value of mobility used in the model was extracted from the linear region and it comes out to be around 110 cm^2/Vs for doping concentrations of 1×10^{19} cm^{-3}.

For all the simulations the dotted lines shows the values obtained from Atlas device simulation whereas the solid lines depict the values obtained from the analytical model.

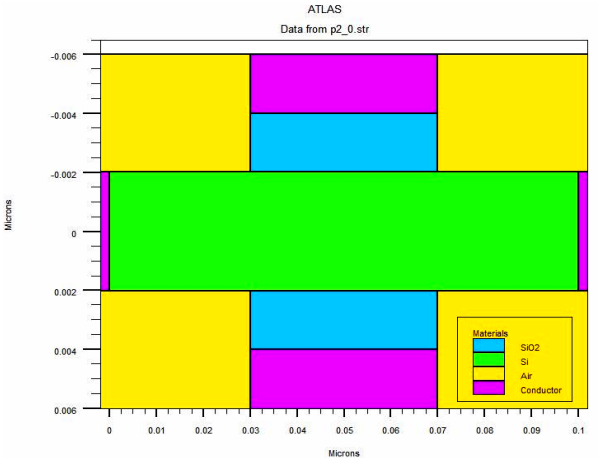

Fig. 3 – Atlas model of JLFET

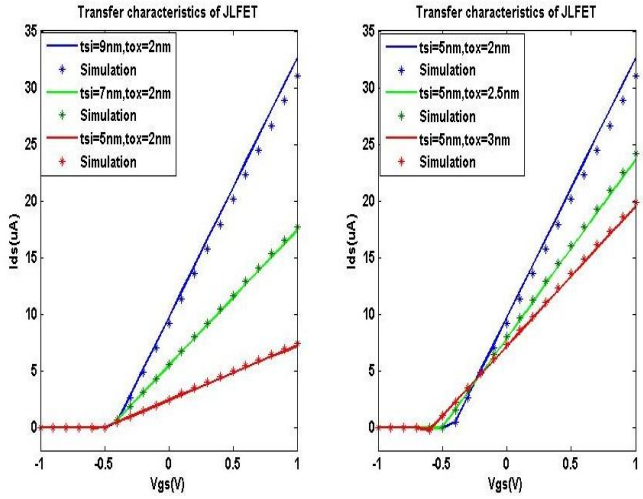

Fig. 4 – Transfer characteristics for the proposed model of DG JLFET taking into consideration different values of oxide thickness, silicon thickness and drain voltages

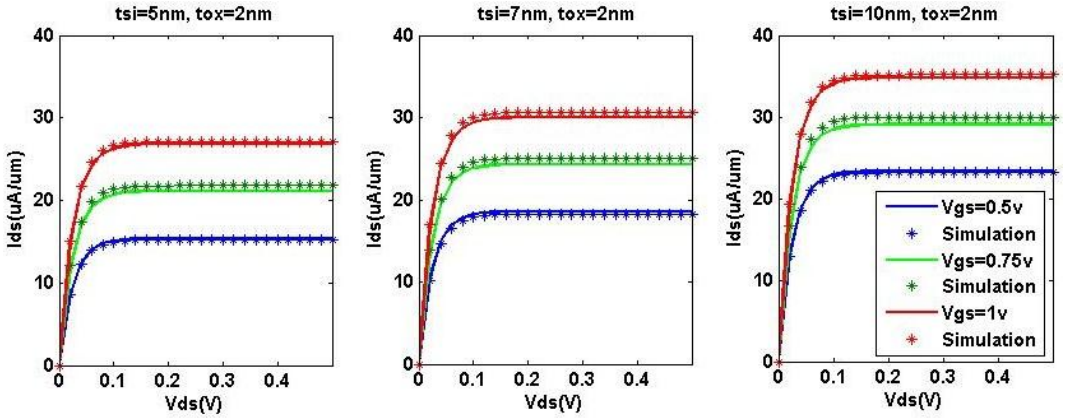

Fig. 5 – Output characteristics for the proposed model of DG JLFET taking into consideration different values of silicon thickness for three different values of gate voltages

Fig. 4 shows the transfer characteristics of the JL DGFET for different values of drain voltages, oxide thicknesses and silicon thicknesses. It is seen here that the variation is more in case of silicon thickness, followed by oxide thickness and then gate to source voltages. The simulation results is quite good in the whole range of the applied gate voltages, and transitions at the boundaries among the subthreshold, partial depletion, and accumulation results are relatively smooth.

The model (lines) shows good agreement with the simulation results (symbols).

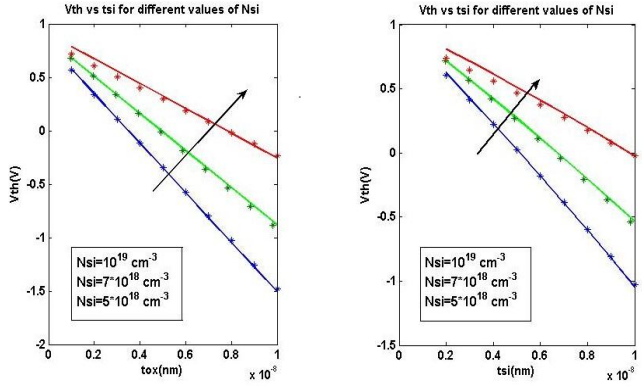

Fig. 6 – Variation of threshold voltage for the proposed model of DG JLFET taking into consideration different values of oxide thickness, silicon thickness and doping concentrations

From Fig. 5 shows the variation of drain current when the gate voltage is kept constant at three values, it is seen that as the drain voltages increases, the JL DGFET is saturated as is expected. Also the variation in drain current is more when the silicon thickness is increased which shows the increase in the bulk current with silicon thickness. The model (lines) shows good agreement with the simulation results (symbols).

Fig. 6 shows the threshold voltages obtained from (11) for different impurity concentrations, silicon thicknesses, and oxide thicknesses. We observe that the threshold voltage decreases with thicker oxide or silicon layer, as well as higher impurity concentration. The model (lines) shows good agreement with the simulation results (symbols).

7. CONCLUSION

An analytical model has been developed to calculate the surface potential and the drain current for a symmetric JL DGFET. The Short-channel and quantum effects are not included in the developed model. The model is valid in all regions of operation, i.e., the subthreshold, linear and saturation regimes. The simulation result shows improved performance of the model and is expected that the application of the JL DGFET proves promising candidate for future technology nodes.

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