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Effects of High-*k* Dielectrics with Metal Gate for Electrical Characteristics of SOI TRI-GATE FinFET Transistor

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In this paper, we present the results of a 3D-numerical simulation of SOI TRI-GATE FinFET transistor. 3D-device structure, based on technology SOI (Silicon-On-Insulator) is described and simulated by using SILVACO TCAD tools and we compare the electrical characteristics results for Titanium Nitride (TiN) fabricated on Al_2O_3 ($k \sim 9$), HfO_2 ($k \sim 20$) and La_2O_3 ($k \sim 30$) gate dielectric.

Excellent dielectric properties such as high-*k* constant, low leakage current, threshold voltage and electrical characteristics were demonstrated.

The implementation of high-*k* gate dielectrics is one of several strategies developed to allow further miniaturization of microelectronic components. From the simulation result; it was shown that HfO_2 is the best dielectric material with metal gate TiN, which giving better subthreshold swing (SS), drain-induced barrier lowing (DIBL), leakage current Ioff and Ion/Ioff ratio.

Keywords: Technology SOI, Short-channel effects (SCEs), Multi-gate SOI MOSFET, SOI TRI-GATE FinFET, High-*k* dielectric, Silvaco Software

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1. INTRODUCTION

With down-scaling of CMOS, the short-channel effects (SCEs) which are caused by the decreasing gate control over the channel are among the most important challenges in the semiconductor industry. In order to suppress the SCEs, novel device architectures have been proposed. Multiple-gate silicon-on insulator MOSFETS, have been proposed due to their ability to overcome several limitations like low speed and reduced short-channel effects (SCEs). The most important types of multiple-gate SOI MOSFET devices are summarized in (Figure 1), represented by the number of gates around the channel.

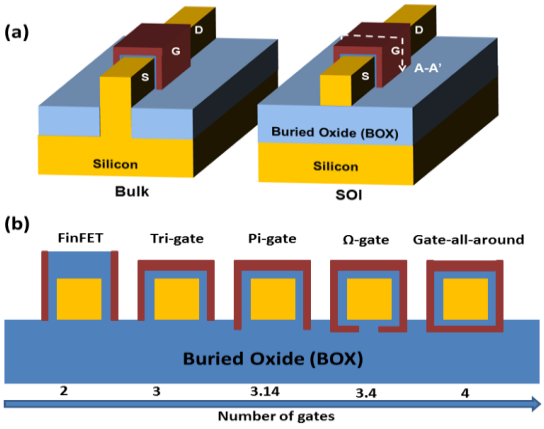

Fig. 1 – Schematic of (a) bulk and SOI multi-gate FETS, as well as, (b) cross-section of different multi-gate FETS and their corresponding effective number of gates [1]

The Fin field effect transistor (FinFETs) is a SOI based multiple gate structure, which is recently emerging as a leading structure to continue the scaling of CMOS technology into the nanometer regime. This promising multiple gate structure has not only the advantage of reducing short channel effects but also of being compatible with the conventional planar CMOS technology. The two most important FinFET structures are the double-gate (DG) SOI MOSFETs and triple-gate (TG).

Of all SOI MOSFET structures, triple-gate transistors are very promising because it combines good sub threshold characteristics with high on-currents and are considered to be very good alternatives to planar devices.

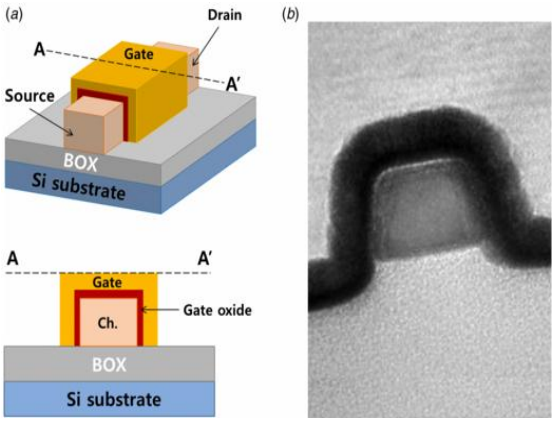

Fig. 2 – Schematic of SOI TRI-GATE FinFET

2. HIGH-K DIELECTRIC

Since the advent of the metal-oxide semiconductor system over 40 years ago, the SiO_2 gate oxide has been serving as the key enabling material in scaling silicon CMOS technology. With the continuous miniaturization of devices, in order to improve the capability of gate control and control the short channel effect, the gate dielectric thickness should be scaled down with channel length. Facing these challenges, scientists

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have already proposed some applicable solutions, including new materials, new technologies and device structure innovation. The major advances in Nanosize materials with high-k gate dielectric and metal gate to solve the problems existing in the gate stack and the low power issue [2].

Replacing the SiO_2 with a high-k material allows increased gate capacitance [3]. The electrical characteristics of the device performance are analyzed with several of high-k materials and the gate oxide thickness is scaled to get same Equivalent Oxide Thickness (EOT) defined as equation (1):

$$EOT = T_{M1}\frac{\varepsilon_{SiO_2}}{\varepsilon_{M1}} + T_{M2}\frac{\varepsilon_{SiO_2}}{\varepsilon_{M2}} \quad (1)$$

Where:

T_{M1} and T_{M2} are the physical thickness of metals-oxides M_1 and M_2, ε_{M1} and ε_{M2} are their relatives dielectrics constants respective, ε_{SiO2} is relative dielectric of the SiO_2.

Recently, many researchers are focused on metal oxide materials with high-k values that have the ability to be integrated in MOSFET process flow. There are many high-k materials that are being studied nowadays such as Al_2O_3, HfO_2, and La_2O_3 [4]. The best characteristics of gate dielectric should have high dielectric constant, large band gap with a favorable band alignment, low interface state density and good thermal stability. Among the high-k materials are compatible with silicon, and also materials have too low or high dielectric constant may not be adequate choice for alternative gate dielectric [5].

Among the high-k dielectrics which are currently most promising, as their dielectric permittivity are referred in Table 1.

Table 1 – High-k dielectrics with their dielectric permittivity

Material	Dielectric permittivity
HfO_2	20
Al_2O_3	9
Y_2O_3	15
La_2O_3	30
ZrO_2	25

Among all the potential candidates for metal gate, TiN is widely studied because of its superior performance such as stability when contacted with high-k dielectrics, low resistivity, and process compatibility [6].

In this paper, we compare the electrical characteristics results for Titanium Nitride (TiN) fabricated on Al_2O_3 ($k \sim 9$), HfO_2 ($k \sim 20$) and La_2O_3 ($k \sim 30$) gate dielectric with Equivalent Oxide Thickness EOT = 1.2 nm .In this simulations, Titanium nitride (TiN) is used as gate contact material and the work function of metal is kept 4.45 eV.

3. DEVICE STRUCTURE

SOI TRI-GATE FinFET structures with using high-k dielectrics Al_2O_3, HfO_2 and La_2O_3 are analyzed and compared by using 3D numerical device simulator SILVACO TCAD. Figure 3 show 3D illustrations of both structures with the cross-sectional views.

The different parameters of our structure are presented in Table 2. The electrical characteristics of the devices were simulated using the Atlas Silvaco software [7].

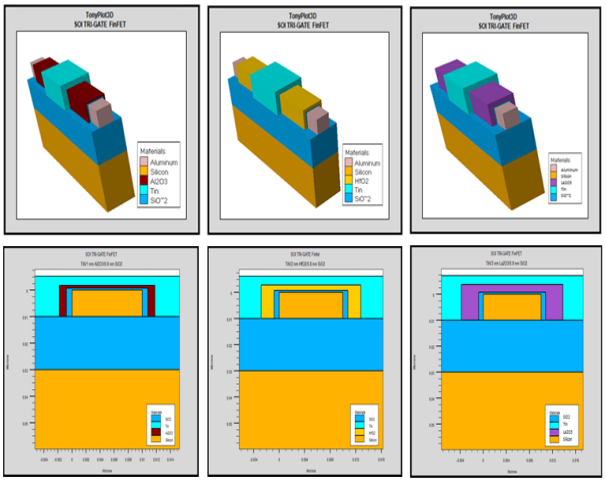

Fig. 3 – 3D device schematic view and Cross-section view of SOI TRI-GATE FinFET with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack, TiN/2 nm HfO_2/0.8 nm SiO_2 stack and with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack

Table 2 – The parameters used for the SOI TRI-GATE FinFET

Device Parameters	TiN /1 nmAl_2O_3 /0.8 nmSiO_2	TiN /2 nm HfO_2 /0.8 nm SiO_2	TiN /3 nmLa_2O_3 /0.8 nm SiO_2
Body Doping Concentration	$5 \times 10^{17}[cm^{-3}]$	$5 \times 10^{17}[cm^{-3}]$	$5 \times 10^{17}[cm^{-3}]$
Drain /Source doping concentration	$5 \times 10^{20}[cm^{-3}]$	$5 \times 10^{20}[cm^{-3}]$	$5 \times 10^{20}[cm^{-3}]$
Gate length	30 [nm]	30 [nm]	30 [nm]
Equivalent Oxide Thickness EOT	1.2 [nm]	1.2 [nm]	1.2 [nm]
Fin Width	10 [nm]	10 [nm]	10 [nm]
Fin Height	10 [nm]	10 [nm]	10 [nm]
Buried oxide thickness	20 [nm]	20 [nm]	20 [nm]
Substrate thickness	30 [nm]	30 [nm]	30 [nm]
Work function Φ_{TiN}	4.45 [ev]	4.45 [ev]	4.45 [ev]

4. SIMULATION AND RESULTS

4.1 Drain Source Saturation Current (Idsat)

Simulation results show that there is an increase in Id sat for SOI TRI-GATE FinFET when we use High-k dielectrics Al_2O_3 ($k \sim 9$), HfO_2 ($k \sim 20$) and La_2O_3 ($k \sim 30$).

The devices have been simulated for a drain bias of 0 to 0.6 V and for a gate bias of 0.8 V (Figure 4).

Idsat for SOI TRI-GATE FinFET out to be $1.82\ e^{-5}$ A with TiN/2 nm HfO_2/0.8 nm SiO_2 stack and $2.02\ e^{-5}$ A with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack but reduced to $1.69\ e^{-5}$ A with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack.

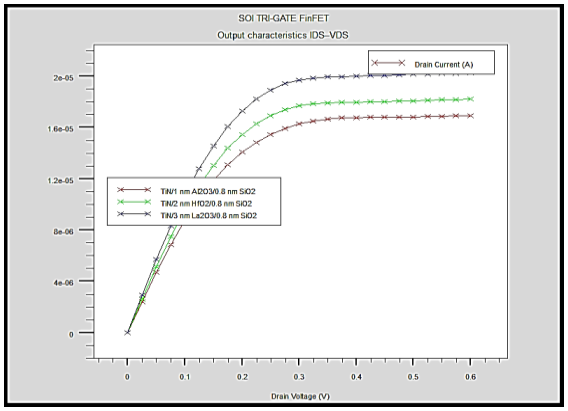

Fig. 4 – I_{DS}-V_{DS} characteristics of SOI TRI-GATE FinFET with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack, TiN/2 nm HfO_2/0.8 nm SiO_2 stack and with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack

4.2 Input Threshold voltage (V_{th})

Simulation results show increasing threshold voltage for SOI TRI-GATE FinFET when we have use Al_2O3, HfO_2 and La_2O_3 as gate dielectric.

Threshold voltage has been calculated for drain source voltage of 0.1 V, while varying gate source voltage from 0 V to 0.6 V (Figure 5).

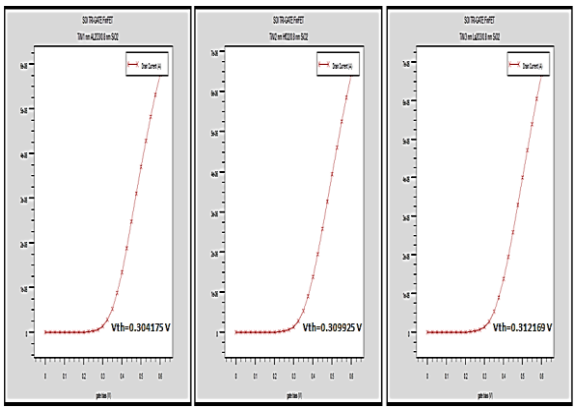

Fig. 5 – I_{DS}-V_{GS} characteristics of SOI TRI-GATE FinFET with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack, TiN/2 nm HfO_2/0.8 nm SiO_2 stack and with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack

Threshold voltage for SOI TRI-GATE FinFET out to be 0.304175 V with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack and to 0.309925 V with TiN/2 nm HfO_2/0.8 nm SiO_2 stack and to 0.312169 V with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack.

4.3 Subthreshold Slope

Sub threshold slope or swing is an important parameter reveals how better the device functions as a switch.

The lower the value of SS, the more efficient and rapid the switching speed of the device from the off state to the on state. It is easily seen that SS is the inverse of the slope of the weak-inversion part of the Log I_{DS} vs V_{GS} in Figure 6, the expression for sub threshold slope is given by Equation (2) [8]:

$$S = \frac{dV_{GS}}{d(\log I_{DS})} \quad (2)$$

Where dV_{GS} is change in gate voltage, dI_{DS} is change in drain current.

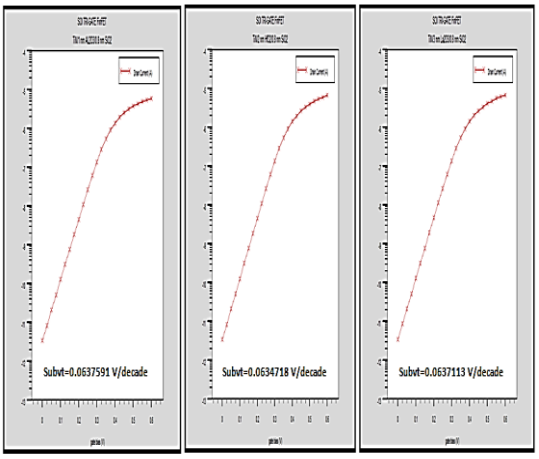

Fig. 6 – I_{DS}-V_{GS} subthreshold voltage of SOI TRI-GATE FinFET with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack, TiN/2 nm HfO_2/0.8 nm SiO_2 stack and with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack

Simulation results show that there is an improvement in subthreshold slope for SOI TRI-GATE FinFET with HfO_2 dielectric compared to SOI TRI-GATE FinFET with Al_2O_3 and La_2O_3 dielectrics.

Subthreshold slope for SOI TRI-GATE FinFET comes out to be 63.7591 mv/decade with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack and to 63.4718 mv/decade with TiN/2 nm HfO_2/0.8 nm SiO_2 stack and to 63.7113 mv/decade with TiN/3 nm La_2O_3/0.8 nm SiO_2/stack.

4.4 Drain Source off Current (I_{off})

One of the biggest challenges faced by MOSFET scaling is high value of off state current or high leakage current resulting in high power consumption.

Simulation results infer that there is decrease in off state current for SOI TRI-GATE FinFET with HfO_2 dielectric compared to SOI TRI-GATE FinFET with Al_2O_3 and La_2O_3 dielectrics.

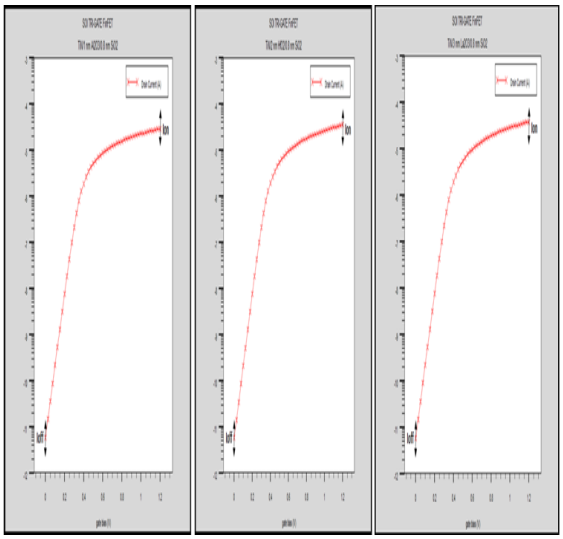

Fig. 7 – I_{DS}-V_{GS} curve of SOI TRI-GATE FinFET with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack, TiN/2 nm HfO_2/0.8 nm SiO_2 stack and with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack

Off state current has been calculated for drain source voltage (V_{DS} = 1.2 V) and gate source voltage from (V_{GS} = 0 V).

With the integration of high-k dielectrics into SOI TRI-GATE FinFET, the performance of the device is further enhanced and improved.

Off state current of SOI TRI-GATE FinFET out to be 6 e^{-12} A with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack and to 5.79 e^{-5} A with TiN/1nm Al_2O_3/0.8 nm SiO_2 but reduced to 5.6 e^{-12} A with TiN/2 nm HfO_2/0.8 nm SiO_2 stack.

4.5 Drain Source on Current (I_{on})

On state current is also one of the important parameter of a device, which determines fan out & fan in capabilities of a circuit, etc. Simulation results show that there is significant improvement in on state current for SOI TRI-GATE FinFET when La_2O_3 is used as dielectric as compare to Al_2O_3 and HfO_2 in SOI TRI-GATE FinFET.

On state current has been calculated for drain source voltage (V_{DS} = 1.2 V) and gate source voltage (V_{GS} = 1.2 V) (Figure 7).

On state current of SOI TRI-GATE FinFET out to be 3.53 e^{-5} A with TiN/2 nm HfO_2/0.8 nm SiO_2 stack and to 3.72 e^{-5} A with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack but reduced to 2.88 e^{-5} A with TiN/1 nm Al_2O_3/0.8 nm SiO_2.

4.6 Ratio of Drain Source on Current to Drain Source off Current (I_{on}/I_{off})

The on/off current ratio is very important for the digital VLSI design. It will determine the speed-power performance parameter of the circuit. The higher the ratio, the better will be the performance of the circuit in terms of speed and power. Simulation results infer improvement in the SOI TRI-GATE FinFET with stacking TiN/2 nm HfO_2/0.8 nm SiO_2. The ratio has been calculated for drain source voltage (1.2 V) and gate source voltage from 0 V to 1.2 V (Figure 7).

I_{on}/I_{off} ratio of SOI TRI-GATE FinFET out to be 6.3 e^6 with TiN/2 nm HfO_2/0.8 nm SiO_2 stack and to 6.2 e^6 with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack but reduced to 5 e^6 with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack.

4.7 DIBL (Drain Induced Barrier Lowering)

The fundamental electrical limitation in VLSI will be the spacing of the surface diffusions that form p-n junctions. Reverse bias on one diffused junction creates a field pattern that can lower the potential barrier separating it from an adjacent diffused junction. When this barrier lowering is large enough, the adjacent diffusion behaves as a source, resulting in an unwanted current path.

It is obtained by carrying out the difference on threshold voltage for two voltages drain, a first is the low drain voltage (V_{DS1} = 0.1 V) and the second the high drain voltage (V_{DS2} = 1.2 V).

$$DIBL = \frac{V_{th}|_{V_{DS2}} - V_{th}|_{V_{DS1}}}{V_{DS2} - V_{DS1}} \quad (3)$$

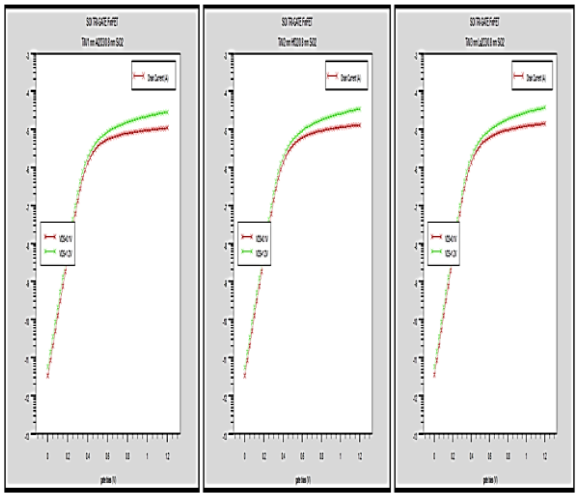

Fig. 8 – DIBL effect in SOI TRI-GATE FinFET with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack, TiN/2 nm HfO_2/0.8 nm SiO_2 stack and with TiN/3 nm La_2O_3/0.8 nm SiO_2 stack

DIBL of SOI TRI-GATE FinFET out to be 44 with TiN/1 nm Al_2O_3/0.8 nm SiO_2 stack and to 42 with TiN/3 nm La_2O_3/0.8 nm SiO2 stack but reduced to 40 with TiN/2 nm HfO_2/0.8 nm SiO_2 stack.

5. CONCLUSION

SOI TRI-GATE FinFET structures were successfully designed and stimulated to study the several dielectric materials on metal gate of device performance. The performance of the three dielectric materials, Al_2O_3, HfO_2 and Al_2O_3 with TiN as metal gate were compared.

HfO_2 is the best dielectric material with metal gate TiN, which shown better subthreshold swing (SS), drain-induced barrier lowing (DIBL), leakage current I_{off} and I_{on}/I_{off} ratio, for this reasons, HfO_2 is the best dielectric material for the future nano-scale Multi-gate SOI MOSFETs devices technology.

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