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A Two Dimensional Surface Potential Model for Triple Material Double Gate Junctionless Field Effect Transistor

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In this paper, a two dimensional analytical Surface Potential model for the triple material double gate (TMDG) junctionless-field effect transistor (JLFET) in sub-threshold region has been presented. The effect of source and drain depletion width has also been taken into account. We have solved two-dimensional Poisson's equation for the Surface Potential. Then the centre potential and the electric field is also obtained. We have calculated the surface potential for different channel lengths. All the modelled results are then compared with the simulated results of the 2D device simulator TCAD.

Keywords: Triple Material Double Gate (TMDG), Junctionless field effect transistor (JLFET), Surface Potential, Centre potential.

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1. INTRODUCTION

With the need of smaller dimension of the transistor for modern technology, the complexity of formation of abrupt source/drain junction with the channel, the leakage current, and short channel effects (SCEs) are increasing. To deal with these problems the Junctionless Transistor (JLFET) is a suitable candidate in submicron regime. The temperature performance and electrical performances of Junctionless Transistor are discussed in [1], [2]. The Junctionless transistor has improved short channel effects, low thermal budget and of course there is no need to form any source/drain junctions, thus the complexity of fabrication is also reduced. But the junctionless transistor also comes to have lower carrier mobility which in effect reduces the current and the trans-conductance of junctionless transistor [3-5].

Meanwhile Dual material gate (DMG) structured devices has been studied in previous, Which has better carrier mobility, improved trans-conductance, improved Short Channel Effects (SCEs) over the single material gate devices [6-10]. Dual material gate has higher drain current, and there is a step in surface potential because of different work functions of gate, an enhanced electric field in the channel [6, 7]. The peak electric field near the drain is also reduced and a smaller peak arises near the source region, which provides more acceleration to mobile charge carrier (electrons), and hence increasing carrier velocity [6]. A surface potential based model of dual material double gate junctionless transistor is presented in [10].

Further improvement in the performance of junctionless transistor can be achieved by using triple material for gate. Triple Material Double Gate (TMDG) structure has been studied for MOSFET [11, 12] which shows improved short channel effects, better drain current, transconductance. Triple Material Double Gate Structure is studied for JLFET in [13]. This shows better transconductance, higher drain current, improved electric field and increase in gate bandwidth product. So far, no model has been proposed to model the surface potential of TMDG-JLFET. So in this paper, we propose the surface potential model for the same. The numerical solution is then compared with results of the 2D device simulator ATLAS.

2. SURFACE POTENTIAL MODEL

In this section the surface potential model for subthreshold region is presented. The device structure is shown in Fig. 1. In this L_1, L_2 and L_3 are the lengths of gate with materials of work function ϕ_{m1}, ϕ_{m2} and ϕ_{m3} respectively, t_{ox} is oxide thickness, t_{si} is silicon channel thickness. Total length of gate is $L = L_1 + L_2 + L_3$ and L is 90 nm. The material near the source is of highest work function, and the material near the drain is of lowest work function. We have taken the values for ϕ_{m1}, ϕ_{m2} and ϕ_{m3} as 5.27, 4.9 and 4.7 respectively. The silicon channel and source/drain regions are doped with n-type impurity and have a concentration of 1.1×10^{19}cm^{-3}. The silicon thickness and oxide thickness are 8nm and 2nm respectively.

Two dimensional Poisson's equation for the channel can be written as:

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{qN_D}{\varepsilon_{si}}\left[e^{\left(\frac{\phi-V}{V_t}\right)}-1\right] \quad (1)$$

Where $\phi(x,y)$ represents the potential at any point (x,y) within the channel, N_D is channel doping concentration, V is the quassi fermi potential which is equal to built in potential, ε_{si} is silicon dielectric constant and V_t is thermal voltage.

K.K. Young has demonstrated in his paper [14] that the potential profile in vertical y-direction is parabolic. The solution of the Poisson's equation has to be obtained for different channel regions under gate materials with work function ϕ_{m1}, ϕ_{m2} and ϕ_{m3}. So the solution to the equation can be given as:

$$\phi(x,y)=\phi_{sk}(x)+a_{k1}(x)y+a_{k2}(x)y^2 \quad (2)$$

Here $k = 1,2$ and 3 for the regions under gate materials with work functions ϕ_{m1}, ϕ_{m2} and ϕ_{m3} respectively, $\phi_{sk}(x)$ is the surface potential at $y = 0$.

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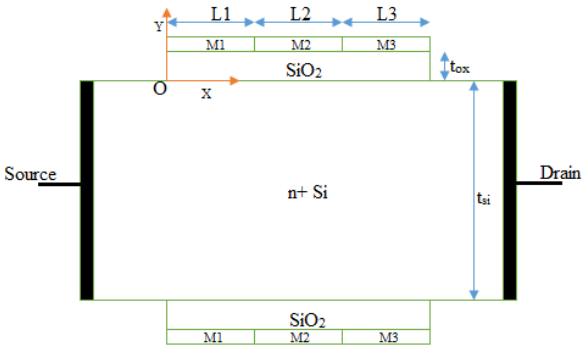


Fig. 1 – Schematic view of TMDG-JLFET. The boundary conditions for the device are as follows

1. At the gate-oxide interface the electric field is continuous for all gate regions, and is given as:

$$\frac{\partial \phi_k(x,y=0)}{\partial y} = \frac{\varepsilon_{ox}(\phi_{sk}(x)-V_{gs}+V_{fbk})}{t_{ox}\varepsilon_{si}} \quad (3)$$

Here V_{gs} is applied gate voltage, V_{fbk} is flat band voltage of kth region, ε_{ox} is permittivity of oxide region and t_{ox} is the thickness of oxide region.

2. The potential within the channel is continuous. So the potential at the interface of two dissimilar metal is also continuous. Therefore

$$\phi_1(L_1,0) = \phi_2(L_1,0) \quad (4)$$

$$\phi_2(L_1+L_2,0) = \phi_3(L_1+L_2,0) \quad (5)$$

3. The electric flux is also continuous at the metal interfaces, which can be written as

$$\frac{\partial \phi_1(L_1,y)}{\partial x} = \frac{\partial \phi_2(L_1,y)}{\partial x} \quad (6)$$

$$\frac{\partial \phi_2(L_1+L_2,y)}{\partial x} = \frac{\partial \phi_3(L_1+L_2,y)}{\partial x} \quad (7)$$

4. The potential at the source end is

$$\phi_{s1}(0) = \mathrm{V} - \frac{qN_b d_s^2}{2\varepsilon_{si}} \quad (8)$$

Where d_S represents the extra depletion taken into consideration for source region [15].

5. Similarly for the drain end the potential is

$$\phi_{s3}(L_1+L_2+L_3,0) = V + V_{ds} - \frac{qN_b d_D^2}{2\varepsilon_{si}} \quad (9)$$

d_D is extra depletion into Drain and V_{ds} is drain to source voltage [15].

For the subthreshold region, i.e. for the applied gate voltage (V_{gs}) less than Threshold voltage (V_{th}), there is a completely depleted channel. So there are no free mobile charge carriers. Hence equation (1) can be written as

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = -\frac{qN_b}{\varepsilon_{si}} \quad (10)$$

Moreover the electric field at the centre of the device is zero, because of the symmetry along the y-axis. Therefore

$$\frac{\partial \phi_k(x,y=t_{si}/2)}{\partial y} = 0 \quad (11)$$

Using the equations (3) and (11), we can find out the values of $a_{k1}(x)$ and $a_{k2}(x)$

$$\mathrm{a_{k1}}(x) = \frac{\varepsilon_{ox}(\phi_{sk}(x)-V_{gs}+V_{fbk})}{t_{ox}\varepsilon_{si}} \quad (12)$$

$$\mathrm{a_{k2}}(x) = \frac{\varepsilon_{ox}(\phi_{sk}(x)-V_{gs}+V_{fbk})}{t_{si}t_{ox}\varepsilon_{si}} \quad (13)$$

Putting (12) and (13) in (2) we get

$$\phi(x,y) = \phi_{sk}(x) + \frac{\varepsilon_{ox}(\phi_{sk}(x)-V_{gs}+V_{fbk})}{t_{ox}\varepsilon_{si}}\left(y - \frac{y^2}{t_{si}}\right) \quad (14)$$

Now Putting (14) in (10), we get

$$\frac{\partial^2 \phi_{sk}(x)}{\partial x^2} - \alpha\phi_{sk}(x) = \beta \quad (15)$$

Where

$$\alpha = \frac{2\varepsilon_{ox}}{t_{si}t_{ox}\varepsilon_{si}} \quad (16)$$

$$\beta = -\left(\frac{qN_b}{\varepsilon_{si}} + \alpha(V_{gs}+V_{fbk})\right) \quad (17)$$

Solution to the equation (14) can be given [8]

$$\phi_{s1}(x) = A_1 exp(\gamma x) + B_1 \exp(-\gamma x) - \frac{\beta_1}{\alpha} \quad (18)$$

$$\phi_{s2}(x) = A_2 exp(\gamma(x-L_1)) + B_2 \exp(-\gamma(x-L_1)) - \frac{\beta_2}{\alpha} \quad (19)$$

$$\phi_{s3}(x) = A_3 exp\big(\gamma(x-L_1-L_2)\big) + B_3 \exp(-\gamma(x-L_1-L_2)) - \frac{\beta_3}{\alpha} \quad (20)$$

Where $\gamma = \sqrt{\alpha}$ and $\phi_{s1}(x), \phi_{s2}(x)$ *and* $\phi_{s3}(x)$ are Surface Potentials for regions under gate material of work functions ϕ_{m1}, ϕ_{m2} and ϕ_{m3} respectively.

Values of constant A_1, B_1, A_2, B_2, A_3 and B_3 can be calculated by solving for boundary conditions (4)-(9)

$$B_1 = -\left[\frac{\left[V_d' - \left(V_s' + \frac{\beta_1}{\alpha}\right)\exp[\gamma(L_1+L_2+L_3)] + \sigma_1 \cosh[\gamma(L_2+L_3)] + \sigma_2 \cosh(\gamma L_3) + \frac{\beta_3}{\alpha}\right]}{2\sinh[\gamma(L_1+L_2+L_3)]}\right] \quad (21)$$

$$A_1 = V_s' + \frac{\beta_1}{\alpha} - B_1 \quad (22)$$

$$A_2 = A_1\exp(\gamma L_1) - \frac{\sigma_1}{2} \quad (23)$$

$$B_2 = B_1\exp(-\gamma L_1) - \frac{\sigma_1}{2} \quad (24)$$

$$A_3 = A_2\exp(\gamma L_2) - \frac{\sigma_2}{2} \quad (25)$$

$$B_3 = B_2\exp(-\gamma L_2) - \frac{\sigma_2}{2} \quad (26)$$

Where

$$V_d' = V + V_{ds} - \frac{qN_b d_D^2}{2\varepsilon_{si}} \quad (27)$$

$$V_s' = V - \frac{qN_b d_S^2}{2\varepsilon_{si}} \quad (28)$$

$$\sigma_1 = \frac{\beta_1 - \beta_2}{\alpha} \quad (29)$$

$$\sigma_2 = \frac{\beta_2 - \beta_3}{\alpha} \quad (30)$$

Values of d_S and d_D can be calculated as [10]

$$d_S = \frac{\frac{-qN_D}{\varepsilon_{si}\gamma} + \sqrt{\left(\frac{-qN_D}{\varepsilon_{si}\gamma}\right)^2 - \frac{2qN_D(-\frac{\beta_1}{\alpha} - V)}{\varepsilon_{si}}}}{\frac{qN_D}{\varepsilon_{si}}} \quad (31)$$

$$d_D = \frac{\frac{-qN_D}{\varepsilon_{si}\gamma} + \sqrt{\left(\frac{-qN_D}{\varepsilon_{si}\gamma}\right)^2 - \frac{2qN_D(-\frac{\beta_2}{\alpha} - V - V_{ds})}{\varepsilon_{si}}}}{\frac{qN_D}{\varepsilon_{si}}} \quad (32)$$

3. CENTRAL POTENTIAL MODEL

Equation (14) gives the potential within the channel. If we want to find the potential at the center of device, put $y = t_{si}/2$ in (14). Therefore the center potential $\phi_{ck}(x)$ for kth region under kth gate material is given as

$$\phi_{ck}(x) = \phi_{sk}(x)\left[1 + \frac{\varepsilon_{ox}}{4C_{si}}\right] - \frac{C_{ox}}{4C_{si}}\left(V_{gs} - V_{fb}\right) \qquad (33)$$

Where

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \text{ and } C_{si} = \frac{\varepsilon_{si}}{t_{si}}$$

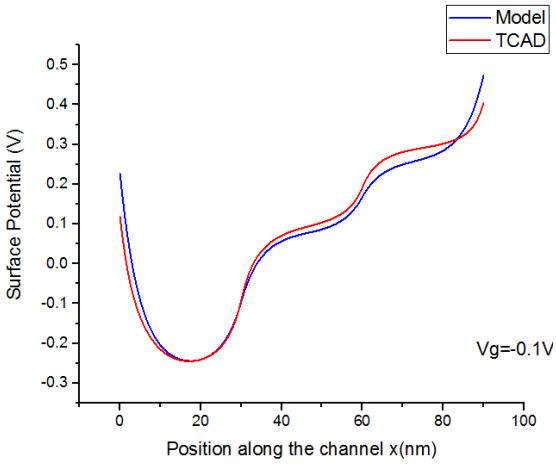
The electric field within the channel along the x-axis can be obtained by differentiating the surface potential (18-20) with respect to x. The electric field $E_k(x)$ for region under k^{th} gate material is

$$E_k(x) = -\frac{d\phi_{sk}(x)}{dx} \qquad (34)$$

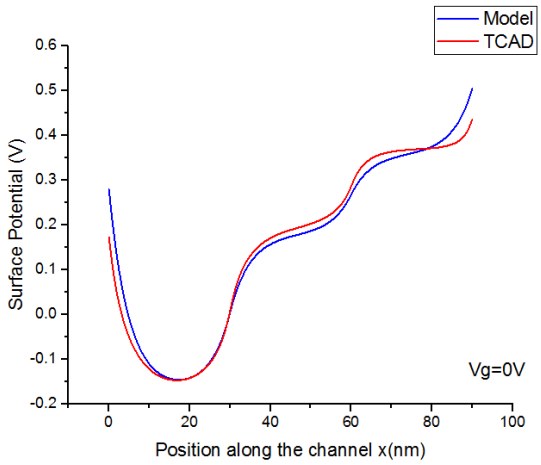
4. RESULTS AND DISCUSSION

In this section we present the results of the model. The surface potential, centre potential and electric field are calculated along the channel. The modelled results are compared with the results of 2D device simulator ATLAS [16]. The Fermi-Dirac statistic model, drift-diffusion model, field dependant mobility model are used for simulations. The workfunctions of gate materials ϕ_{m1}, ϕ_{m2} and ϕ_{m3} as 5.27, 4.9 and 4.7 respectively. L_1, L_2 and L_3 are the channel lengths for three gate materials and are 30 nm each. The drain voltage (V_{ds}) for all the cases is taken at 0 V. Fig. 2(a) and (b) shows the surface potential for an applied gate voltage – 0.1 V and 0 V respectively. The model is in good agreement with the results of TCAD. There are three step profiles within the channel and the potential near the source is lower than potential at the drain. This is because of the high workfunction of material near source. So the surface potential near the source is effectively screened from the drain potential because of two screen gates near drain.

Fig. 3. Shows the centre potential for gate voltages -0.2 V and – 0.1 V taken at $y = t_{si}/2$. Fig. 4 (a) and (b) shows the Electric Field along the channel (along x-axis) at $y = 0$. This shows the steps in the peak electric



(a)



(b)

Fig. 2 – Surface potential for gate voltage (V_{gs}) (a) at – 0.1 V and (b) at 0 V

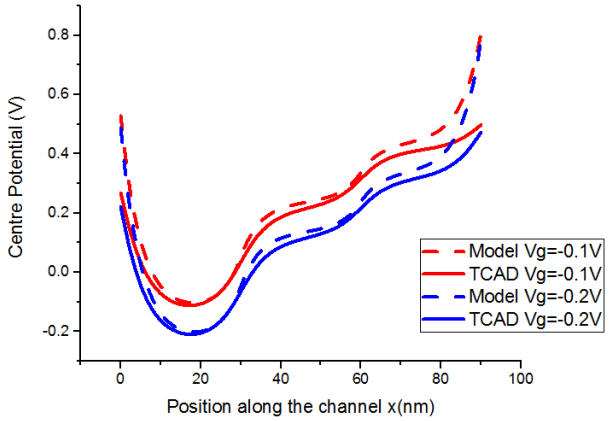
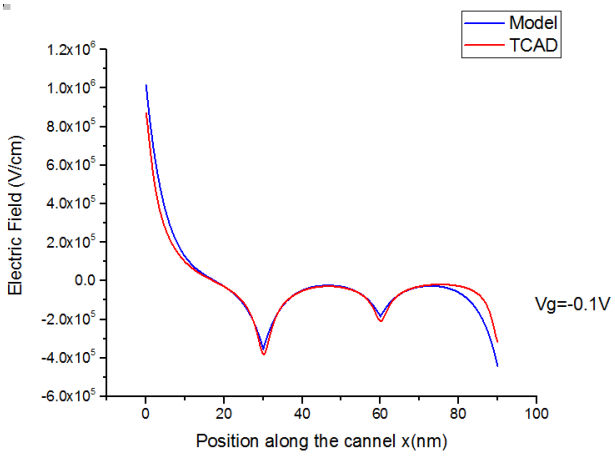
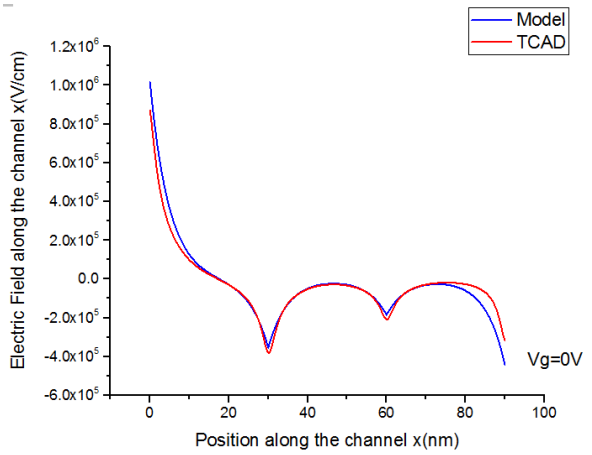


Fig. 3 – Centre potential at gate voltage V_{gs} – 0.2 V and – 0.1 V



(a)



(b)

Fig. 4 – Electric Field along the channel for gate voltage V_{gs} (a) – 0.1 V and (b) 0 V

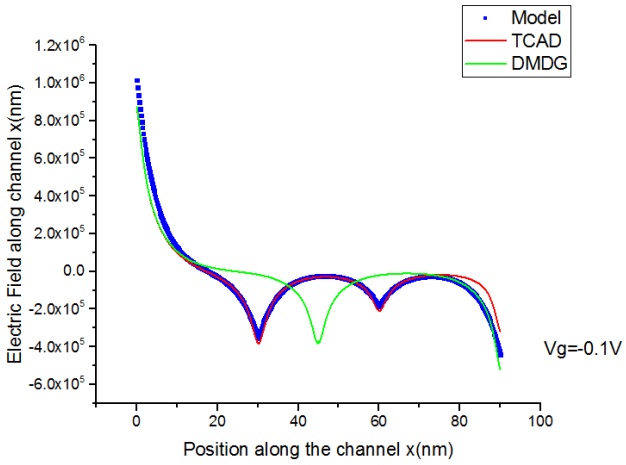


Fig. 5 – Comparison of Electric Field of Dual Material Double Gate JLFET and TMDG-JLFET

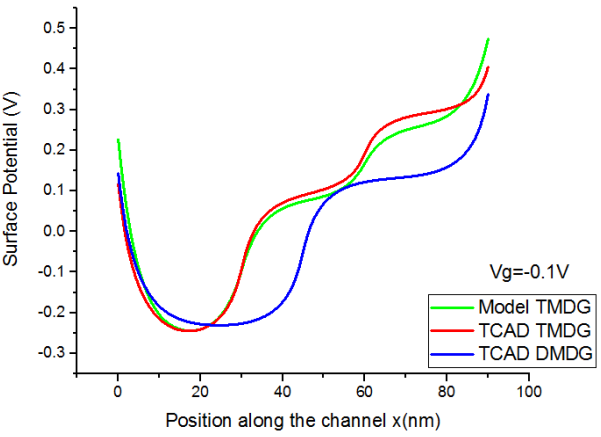


Fig. 6 – Comparison of DMDG-JLFET surface potential profile with TMDG-JLFET surface potential

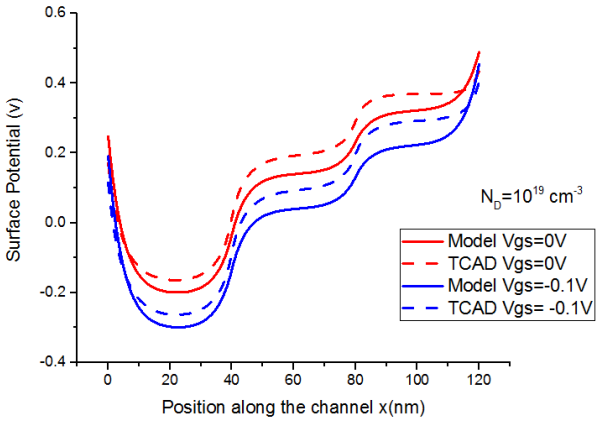


Fig. 7 – Surface Potential for channel length 120 nm and doping concentration (N_D) 10^{19} cm^{-3}

field because of different materials used in gate. Fig. 5 depicts the comparison of electric field of dual material double gate (DMDG) JLFET with the TMDG-JLFET. Here DMDG-JLFET is taken with channel length of 90 nm and the material have workfunctions ϕ_{m1}, and ϕ_{m2} as 5.27, and 4.9 respectively. Length of each gate portions is in ratio of 1 : 1. This is clear from the fig. 5. that peak electric field near the drain is lower for TMDG-JLFET than the electric field of DMDG-JLFET. Also there is one more peak electric field step near the source for TMDG-JLFET.

In figure 6, the comparison of surface potential profile of Dual Material Double Gate JLFET is given with the surface potential of the TMDG-JLFET. The channel length for DMDG-JLFET is also 90nm and the material have workfunctions ϕ_{m1}, and ϕ_{m2} as 5.27, and 4.9 respectively. The channel length (L_1 and L_2) for workfunctions ϕ_{m1}, and ϕ_{m2} are 45nm each. In figure 7 the surface potential is presented for a channel length of 120 nm. The ratio for different channel material is again 1:1:1. But the doping concentration for this case is taken to be 10^{19} cm^{-3}. Two profiles have been compared with simulated results from TCAD, at gate voltages of – 0.1 V and 0 V.

5. CONCLUSION

A two dimensional surface potential model is presented for Triple Material Double Gate JLFET for first time. We have seen the value of peak electric field near the drain is lower for the TMDG-JLFET structure than the DMDG-JLFET. Also the comparison between the surface potential of DMDG-JLFET and TMDG-JLFET is presented in the paper.

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