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Design of Novel Efficient Multiplexer Architecture for Quantum-dot Cellular Automata

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One of the promising emerging technology at nanoscale level to replace the conventional CMOS technology is Quantum-dot Cellular Automata (QCA). It has several advantages compared to conventional CMOS technology. Whereas multiplexers play a vital role in digital circuit implementations, this paper presents and evaluates a modular design methodology to build the high-performance 2^n:1 multiplexer. An efficient 2:1 QCA multiplexer architecture is proposed as the basic logic unit, which is utilized to present new and efficient 4:1, and 8:1 QCA multiplexer architectures. The proposed architectures have been implemented on the QCADesigner version 2.0.1. Our implementation results show that the proposed QCA multiplexer architectures have the best performance compared to other multiplexer architectures and outperform most of them in terms of area and clock zones.

Keywords: Quantum cellular automata, Nanotechnology, Multiplexer, Wire crossing, Combinational logic, QCADesigner.

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1. INTRODUCTION

The conventional CMOS technology is facing with some serious challenges, due to the CMOS technology in nanoscale is not feasible since it introduces an anomalous quantum behavior beyond 10-nm [1], [2]. Quantum-dot Cellular Automata (QCA) is a promising technology suitable for the development of Moore's law and it can be suitable alternative for the conventional CMOS technology. In the QCA technology, the binary information is coded using appropriate formation of the charges instead of current [1], [3]. As a result, circuit design in this technology aims toward small dimensions, fast operation, and low energy consumption [1], [3], [4]. This technology has received widespread attention due to a number of promising applications such as efficient design of QCA full adder [3], [5-7], QCA multiplier [8], [9], and QCA multiplexer [1], [10-30].

In addition, the multiplexers play a vital role in digital circuit implementations [19, 24]. The first QCA multiplexer architecture was proposed by Gin et al. [22] in 1999. They have proposed hierarchical layout methods which combines fundamental QCA devices into more complex devices. After that, several efforts has been presented with target to improve the design of 2:1 QCA multiplexer architectures [1], [10-20], [23], 4:1 QCA multiplexer architectures [1, 12, 14, 15, 18, 20, 21, 24, 25, 29, 30], and 8:1 QCA multiplexer architectures [1, 15, 18, 21, 29] in terms of number of cells and delay in the QCA technology.

In this paper, novel and efficient multiplexer architectures are presented and evaluated. The main contributions are as follows.

a) Presents novel architecture for 2:1 QCA multiplexer as the basic logic unit.
b) Presents novel architectures for 4:1, and 8:1 QCA multiplexer based on this basic logic unit.
c) Implements and verifies the robustness of the proposed QCA multiplexer architectures using the QCADesigner version 2.0.1.

Our implementation results show that the proposed multiplexer architectures present the best performance compared to other modified multiplexer architectures and outperform most of them in terms of area and clock zones.

The rest of this paper is organized as follows. Background of the QCA technology and implementation of multiplexer in this technology are briefly described in section 2. Section 3 presents the proposed QCA multiplexer architectures. Section 4 provides implementation results. The proposed architectures are evaluated in section 5. Finally, section 6 concludes this paper.

2. BACKGROUND

2.1 The QCA cells

The fundamental element in the QCA technology is a four-dot squared cell, which composed of two free identical charges [1, 3, 20, 21]. Figure 1 shows the states of cell polarizations, $P = -1$ and $P = +1$ in a four-dot squared cell.

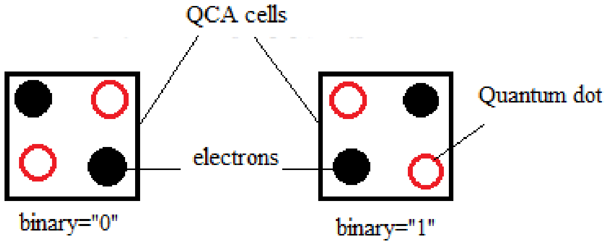

Fig. 1 - Two polarizations of a QCA cell [1], [3]

In this technology, when QCA cells are located near

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each other, the polarization of each cell can influence the polarization of other cells. Interconnection among the electrons of intercell establishes two stable arrangements, $p = 1$ and -1 that are assigned to encode logic "1" and "0" states, respectively [1, 3, 20, 21].

2.2 The QCA Wire

Information are transferred via two types of wires in the QCA technology: (a) coplanar crossing wire, and (b) multilayer crossing wire. Figure 2 shows these two types of QCA wires [26].

As it is illustrated in figure 2, while coplanar crossing wires are utilized a single layer, multilayer crossing wires are required at least three layers [20, 26].

2.3 The QCA Gates

The basic gates in the QCA technology can be classified into three groups: (a) Rotate Majority Gates (RMGs), (b) Original Majority Gates (OMGs), and (c) Inverter Gates (IGs) [3]. Figure 3 illustrates the various fundamental gates in this technology.

These gates are often utilized in the implementation of digital circuits. The output of the majority gates are as follows [1, 3].

$$out = ab + ac + bc \tag{1}$$

It should be noted that the output of the majority gates is "1" when at least two inputs are "1". As a result, these majority gates can works as 2-input OR gates or 2-input AND gates by applying 1 or -1 to input a, respectively [1, 3].

2.4 Clocking in the QCA Circuits

The clocking is used to provide synchronization in operation pipelining in the QCA circuits. The clocking mechanism in these circuits consists of four clock phases with equal frequencies, which are as follows: (a) relax phase, (b) switch phase, (c) hold phase, and (d) release phase. Figure 4 shows the QCA clock phases [3, 20].

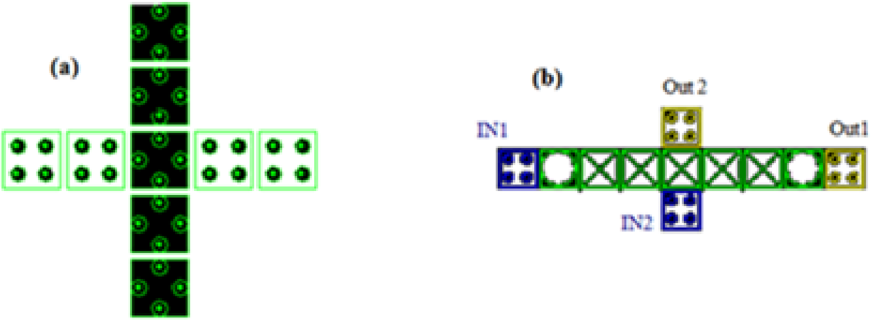

Fig. 2 - The various QCA wire types (a) coplanar crossing wires type, and (b) multilayer crossing wires type [20, 22]

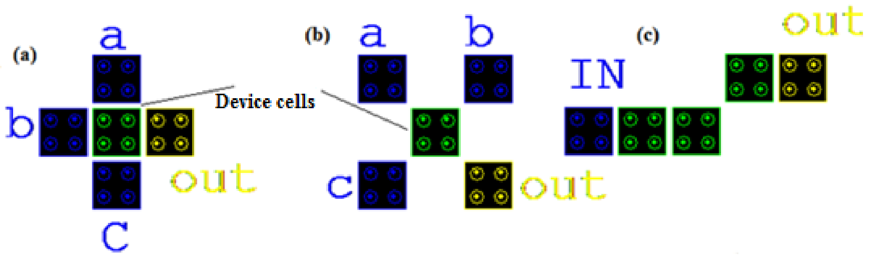

Fig. 3 - Types of QCA Gates (a) original majority gate, (b) rotate majority gate, and (c) inverter gate [1, 3]

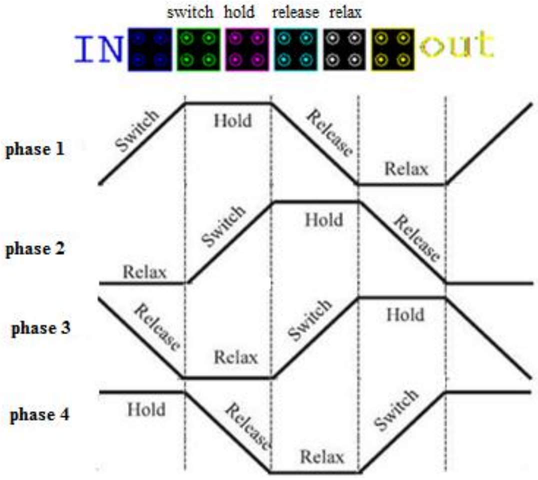

Fig. 4 - Clocking in QCA [3]

The QCA cell starts to rise the tunneling barrier between quantum dots during switch phase. In the hold phase, the tunneling barriers are high enough to prevent carriers from tunneling. In the release phase, the reduction in the cell polarization is started and the cell loses its polarity. Finally, in relax phase, when the clock is low, there is no inter dot barrier and keep the QCA cell in unpolarized state [3, 20]. It should be noted that, the delay in the QCA circuits is determined based on the number of zones in the critical path [3, 20].

3. THE PROPOSED QCA MULTIPLEXER ARCHITECTURES

This section presents novel architecture for the 2:1 QCA multiplexer. It also explores its effectiveness in realizing higher-order 2^n:1 multiplexer architecture for 4:1 and 8:1 QCA multiplexer architectures.

3.1 The Proposed 2:1 Multiplexer Architecture

The proposed architecture for the 2:1 QCA multiplexer is shown in figure 5.

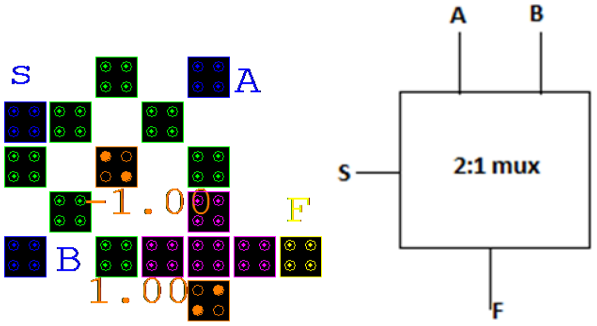

Fig. 5 - The proposed 2:1 QCA multiplexer architecture

In this architecture, the inputs are A and B, and the output is *F*. The signal *S* is utilized as address line. It is easy to verify that, when *S* = 0, input A is selected and when *S* = 1, input B appears at the output. Hence, we implement the proposed 2:1 multiplexer architecture using two RMGs, an OMG and an IG. The output of the proposed 2:1 QCA multiplexer architecture can be shown as follows:

$$F = A\bar{S} + BS \qquad (2)$$

This function can be represented as follows:

$$F = \mathrm{Maj}(\mathrm{Maj}(\bar{S},A,0),\ \mathrm{Maj}(S,B,0),\ 1)$$

We referred to this architecture as the basic logic unit in this paper. The proposed architecture only used two QCA clock zones and 17 QCA cells.

3.2 The Proposed 4:1 QCA Multiplexer Architecture

The proposed architecture for 4:1 QCA multiplexer is based on the basic logic unit. Figure 6 shows the proposed 4:1 QCA multiplexer.

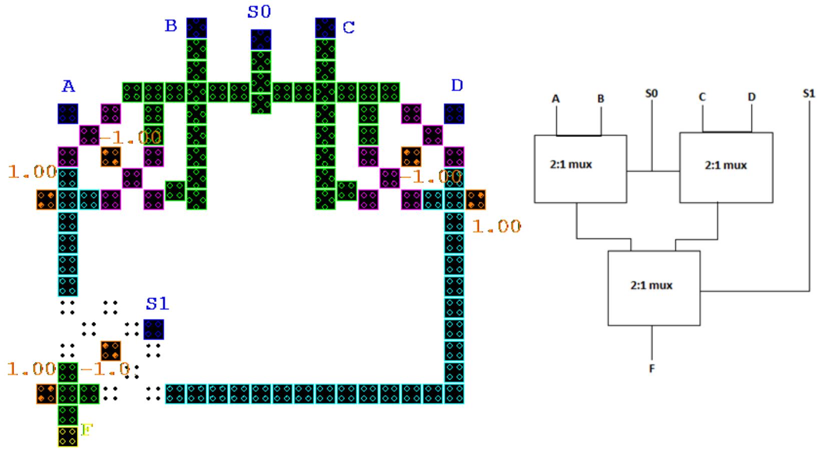

Fig. 6 - The proposed 4:1 QCA multiplexer architecture based-on the basic logic unit

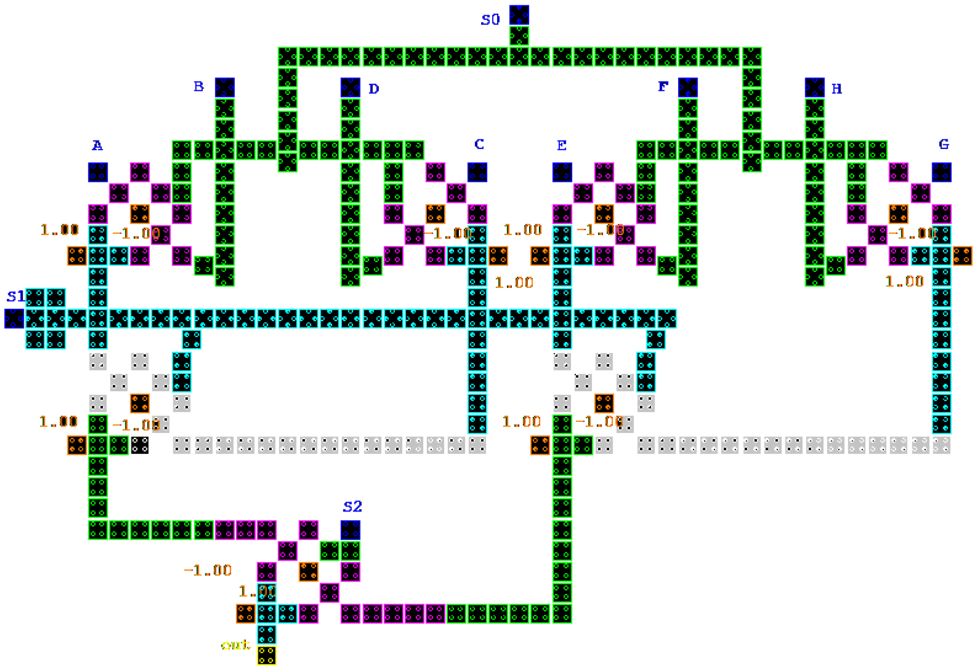

Fig. 7 - The proposed 8:1 QCA multiplexer architecture

The proposed 4:1 QCA multiplexer architecture, which is shown in figure 6, contains three proposed 2:1 QCA multiplexer architecture. In this architecture, inputs are A, B, C and D, and the output is F. In addition, signals S0 and S1 are utilized as address lines. Note that, when $S0 = S1 = 0$, the output will become A. When $S0 = 1$ and $S1 = 0$, the input B is selected and is shown at the output. When $S0 = 0$ and $S1 = 1$, input D is selected to appear at the output, and when $S0 = S1 = 1$, input C is selected to appear at the output. The output of the proposed architecture can be shown as follows.

$$F = \bar{S}0\bar{S}1.A + S0\bar{S}1.B + \bar{S}0S1.D + S0S1.C \tag{3}$$

The proposed architecture used five QCA clock zones and 107 QCA cells.

3.3 The Proposed 8:1 QCA Multiplexer Architecture

The proposed architecture for the 8:1 QCA multiplexer is shown in Figure 7.

In this architecture, the inputs are A, B, C, D, E, F, G, and H, and the output is OUT. Signals S0, S1 and S2 are used for address lines. The output of the proposed architecture is determined as follows:

$$\begin{aligned} \boldsymbol{OUT} &= \left(\bar{\boldsymbol{S}}2.\bar{\boldsymbol{S}}1.\bar{\boldsymbol{S}}0\right)\boldsymbol{A} + \left(\bar{\boldsymbol{S}}2.\bar{\boldsymbol{S}}1.\boldsymbol{S}0\right)\boldsymbol{B} \\ &+ \left(\bar{\boldsymbol{S}}2.\boldsymbol{S}1.\bar{\boldsymbol{S}}0\right)\boldsymbol{C} + \left(\bar{\boldsymbol{S}}2.\boldsymbol{S}1.\boldsymbol{S}0\right)\boldsymbol{D} \\ &+ \left(\boldsymbol{S}2.\bar{\boldsymbol{S}}1.\bar{\boldsymbol{S}}0\right)\boldsymbol{E} + \left(\boldsymbol{S}2.\bar{\boldsymbol{S}}1.\boldsymbol{S}0\right)\boldsymbol{F} \\ &+ \left(\boldsymbol{S}2.\boldsymbol{S}1.\bar{\boldsymbol{S}}0\right)\boldsymbol{G} + \left(\boldsymbol{S}2.\boldsymbol{S}1.\boldsymbol{S}0\right)\boldsymbol{H} \end{aligned} \tag{4}$$

The proposed architecture used seven QCA clock zones and 324 QCA cells.

4. THE IMPLEMENTATION RESULTS

4.1 The Proposed 2:1 Multiplexer Architecture

The proposed 2:1 QCA multiplexer architecture is implemented and verified using QCADesigner version 2.0.1 [27]. Note that, there are two types of implementation engines in QCAdesigner [27]: (a) bi-stable implementation engine and (b) coherence vector implementation engine. The proposed 2:1 QCA multiplexer architecture is implemented in the bi-stable implementation engine. It is because in bi-stable implementation engine, the implementation is done faster. The following parameters are utilized for this implementation: cell size = 18nm, Clock high: 9.8e-22, clock low: 3.8e-22, number of required samples = 448000, convergence tolerance = 0.001000, radius of effect = 41.000000, and maximum iterations per sample = 1000. The rest of the parameters are selected as default. The implementation results are shown in figure 8.

Our implementation results show that the area of the proposed architecture for 2:1 QCA multiplexer is 0.02 μm^2. In addition, the proposed 2:1 QCA multiplexer doesn't have attenuation in the output amplitude.

4.2 The Proposed 4:1 Multiplexer Architecture

The proposed 4:1 QCA multiplexer architecture is implemented and verified using QCADesigner version 2.0.1 [27]. This architecture contains three proposed 2:1 QCA multiplexer architecture. The following parameters are utilized for this implementation: cell size = 18nm, clock high: 9.8e – 22, clock low: 3.8e – 22, number of required samples = 448000, convergence tolerance = 0.001000, radius of effect = 65.000000, and maximum iterations per sample = 100. The rest of the parameters are selected as default.

Our implementation results show that the area of the proposed 4:1 QCA multiplexer architecture is 0.17 μm^2.

4.3 The Proposed 8:1 Multiplexer Architecture

The proposed 8:1 QCA multiplexer architecture is implemented and verified using QCADesigner version 2.0.1 [27]. The proposed 8:1 multiplexer architecture contains two proposed 4:1 QCA multiplexer architecture and a proposed 2:1 QCA architecture. The following parameters are utilized for this implementation: cell size = 18 nm, clock high: 9.8e – 22, clock low: 3.8e – 22, number of required samples = 448800, convergence tolerance = 0.001000, radius of effect = 65.000000, and maximum iterations per sample = 100. The rest of the parameters are selected as default.

Our implementation results show that the area of the proposed 8:1 QCA multiplexer architecture is 0.58 μm^2.

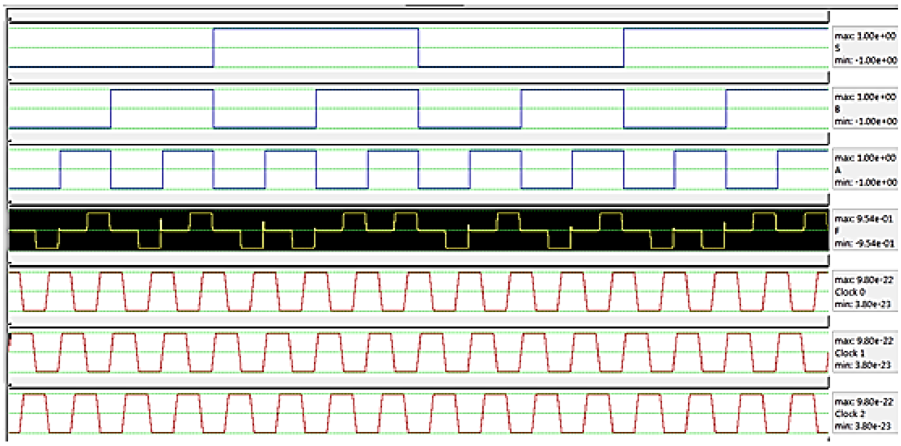

Fig. 8 - The implementation results of the proposed 2:1 QCA multiplexer architecture

5. THE PERFORMANCE COMPARISON

5.1 The Proposed 2:1 Multiplexer Architecture

Table 1 shows the implementation results of the proposed 2:1 QCA multiplexer architecture in comparison with other 2:1 QCA multiplexer architectures in [1], [10-20], [23] and 2:1 CMOS multiplexer architecture in [28].

In this table, complexity is shown in terms of the number of required cells, area is shown in terms of μm^2, and delay is shown in terms of the number of required clock zones.

Based on our implementation results that are shown in table 1, the proposed architecture provide an improvement on the resulting complexity in comparison with recent 2:1 QCA multiplexer architectures in [1], [10-20], [23]. In addition, the proposed architecture provide an improvement on the required area compared to recent 2:1 CMOS multiplexer architectures in [28].

5.2 The Proposed 4:1 Multiplexer Architecture

Table 2 shows the implementation results of the proposed 4:1 multiplexer architecture compared to other 4:1 QCA multiplexer architectures in [1, 12, 14, 15, 18, 20, 21, 24, 25, 29, 30] and 4:1 CMOS multiplexer architecture in [28].

Similar to table 1, in this table, complexity is shown in terms of the number of required cells, area is shown in terms of μm^2, and delay is shown in terms of the number of required clock zones.

Based on our implementation results that are shown in Table 2, the proposed architecture provide an improvement on the resulting complexity, area and delay in comparison with recent 4:1 QCA multiplexer architectures in [1, 12, 14, 15, 18, 20, 21, 24, 25, 29, 30]. In addition, the proposed architecture provide an improvement on the required area compared to recent 4:1 CMOS multiplexer architectures in [28]. It should be noted that only 4:1 QCA multiplexer architectures in [20, 25, 30] have a slightly better complexity and area compared to our proposed 4:1 QCA multiplexer architecture. However, these advantages came from the increased number of layers in layout, which are used in logic structures and interconnections, and they do not came from logic design. Although multilayer crossover gives better implementation results, it may not be as easily fabricated as in coplanar crossovers.

5.3 The Proposed 8:1 Multiplexer Architecture

Table 3 shows the implementation results of the proposed 8:1 QCA multiplexer architecture compared to other 8:1 QCA multiplexer architectures in [1, 15, 18, 21, 29].

Similar to tables 1 and 2, in this table, complexity is shown in terms of the number of required cells, area is shown in terms of μm^2, and delay is shown in terms of the number of required clock zones.

Based on our implementation results that are shown in Table 3, the proposed architecture provide an improvement on the resulting number of cells, area and delay in comparison with recent 8:1 QCA multiplexer architectures in [1, 15, 18, 21, 29]. Note that, only 8:1 QCA multiplexer architecture in [21] for coplanar version has similar area compared to our proposed 8:1 QCA multiplexer architecture. However, the complexity and delay in this architecture is bigger than the proposed 8:1 QCA multiplexer architecture. In addition, the only 8:1 QCA multiplexer architecture that has similar delay is the 8:1 QCA multiplexer architecture of [1]. However, the complexity and area in this architecture is bigger than the proposed 8:1 QCA multiplexer architecture.

The implementation results show that the proposed QCA multiplexer architectures have an improvement in complexity, area, and delay in comparison with other modified QCA multiplexer architectures.

Table 1 - The comparative table for the 2:1 QCA multiplexer architectures

Reference	Complexity (# cells)	Area (μm^2)	Delay (# clock zones)	Wire crossing
[28] CMOS 45-nm	-	1.76	-	-
[1]	23	0.02	2	Coplanar
[10] using QCALG	146	0.28	8	Multilayer
[10] handmade	88	0.14	4	Multilayer
[11]	46	0.08	4	Multilayer
[12]	67	0.14	4	Coplanar
[13]	36	0.06	4	Multilayer
[14]	35	0.04	4	Coplanar
[15]	56	0.07	4	Coplanar
[16]	27	0.03	3	Coplanar
[17]	19	0.02	3	Coplanar
[23]	23	0.02	3	Coplanar
[18]	26	0.02	2	Coplanar
[19]	19	0.02	2	Coplanar
[20]	23	0.01	2	Multilayer (3-layer)
[20]	22	0.01	2	Multilayer (4-layer)
This paper	17	0.02	2	Coplanar

Table 2 - The comparative table for the 4:1 QCA multiplexer architectures

Reference	Complexity(# cells)	Area(μm^2)	Delay (# clock zones)	Wire crossing
[28] CMOS 45-nm	-	4.23	-	-
[1]	155	0.24	5	Coplanar
[12]	215	0.25	6	Coplanar
[14]	124	0.25	8	Coplanar
[15]	290	0.35	7	Coplanar
[18]	271	0.37	19	Coplanar
[30]	114	0.056	4	Multilayer
[20]	103	0.08	7	Multilayer(3-layer)
[20]	94	0.07	6	Multilayer(4-layer)
[21]	251	0.2	5	Multilayer
[21]	199	0.27	6	Coplanar
[29]	223	0.22	6	Coplanar
[24]	246	0.25	5	Multilayer
[25]	154	0.15	4	Multilayer
This paper	107	0.17	5	Coplanar

Table 3 - The comparative table for the 8:1 QCA multiplexer architectures

Reference	Complexity (# cells)	Area (μm^2)	Delay(# clock zones)	Wire crossing
[29]	576	0.82	9	Coplanar
[15]	633	0.67	11	Coplanar
[18]	1312	1.83	42	Coplanar
[1]	462	0.87	7	Coplanar
[21]	608	0.71	9	Multilayer
[21]	494	0.58	9	Coplanar
This paper	324	0.58	7	Coplanar

6. CONCLUSIONS

This paper presented and evaluated novel architecture for 2:1 QCA multiplexer as the basic logic unit, and then novel 4:1, and 8:1 QCA multiplexer architectures have been developed based on this basic logic unit. The proposed 2:1, 4:1, and 8:1 QCA multiplexer architectures consist of 17, 107 and 324 cells, respectively. The designs have been implemented and verified using QCADesigner version 2.0.1. Results confirmed that the proposed QCA multiplexer architectures have improvements compared to other modified QCA multiplexer architectures and CMOS multiplexer architecture in terms of design complexity, area and latency.

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