JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. 9 No 1, 01022(4pp) (2017)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том 9 № 1, 01022(4cc) (2017)

# Design Device for Subthreshold Slope in DG Fully Depleted SOI MOSFET

Neha Goel[1,*], Manoj Kumar Pandey[2,†]

[1] *Research Scholar, SRM University NCR Campus Ghaziabad, India*
[2] *Department of ECE, SRM University NCR Campus Ghaziabad, India*

(Received 24 October 2016; revised manuscript received 07 February 2017; published online 20 February 2017)

In this paper, we discuss how a short channel effects can be suppressed and how a threshold voltage fluctuation can be minimized and better control of subthreshold slope by the impact of the back gate bias and control of gate work function of a fully depleted SOI (Silicon-On-Insulator) MOSFET. The fluctuation in the threshold voltage and subthreshold slope are due to short channel effects. The Back gate voltage plays a significant role on the threshold voltage and thin buried oxide is used to suppress the short-channel effects and is used to keep a low value of the subthreshold slope are described in this paper. It is shown that how short channel effects can be suppressed in order to improve subthreshold slope.

**Keywords:** Fully depleted silicon on insulator (FDSOI), Threshold voltage, Sub threshold slope.

DOI: 10.21272/jnep.9(1).01022 PACS number: 85.30.De

## 1. INTRODUCTION

The Increasing demand for ultra low power consumption, high density opened new opportunities in the high performance range for CMOS. This demand can be gained successfully by continuous scaling down of the MOSFET to smaller physical dimensions. when MOSFET have become smaller, they have become faster, cheaper, provide more functions per unit area of silicon and consume less power. Results, there is an improvement in the performance of MOSFET. But as MOSFET is scaled down, there is a rise in the problem of short channel effects (SCE), like threshold voltage (VTH) roll-off i.e. reduction in threshold voltage with a reduction in channel length [6, 7] and drain- induced barrier lowering (DIBL) i.e. reduction in VTH at higher drain voltage (VDS) due to reduction of the source-channel potential barrier by the drain voltage. Thus becoming a serious concern for high-performance circuits [9]. However, the requirement of continuous improved performance in advanced technologies could not be achieved with bulk CMOS due to the high isolation between the substrate and leading to, the active region can push forward silicon-on- Insulator (SOI) technology to be a promising choice for high- frequency ,high- speed and very low power of system-on-chip integrated circuits [1, 2].

Thin film double gate fully depleted silicon on insulators (SOI) MOSFETs extremely attractive in terms of superior electrical performances like excellent latchup immunity, high speed, low power consumption, radiation-hard, improved isolation & reduced parasitic capacitances compared to bulk silicon technology [3]. The architecture of double gate SOI MOSFETs is more flexible compared to bulk CMOS because more parameters such as thicknesses of film and buried oxide, substrate doping, and back gate bias can be used for optimization and scaling.

Simulations have shown the double gate fully depleted silicon on insulator MOSFET to be good technology for nanoscale technologies [4-6]. Scaled double gate fully depleted silicon on insulator MOSFET has an inherent capability to suppress short channel effects as it have one extra gate due to which gate to channel coupling is doubled and the small influence of source and drain on the channel is observed.

Advantage of Double gate SOI MOSFET over conventional Single Gate MOSFET can be describe in terms of performance and potential for ultimate Scaling, it is expected to provide smaller short-channel effects (SCE), near ideal sub-threshold slopes and higher drive currents when compared to single-gate (SG) transistors.

There are two device design issues arises in fabrication of fully depleted double gate SOI MOSFET, firstly, the adjustment of threshold voltage and second is to keep the steep subthreshold slope. For the adjustment of threshold voltage, the device parmeters such as work function control of gate electrodes, effect of back gate bias provide the superior SCE. On the other hand, for subthreshold slope, ultra thin SOI, thin buried oxides have been proposed to suppress SCE and to keep a low value of subthreshold slope.

## 2. THEORETICAL MODEL

Below is the structure of Double Gate FD SOI MOSFET considered in our analysis as shown in Fig. 1.

In this figure, $t_{si}$ = SOI film thickness ,the front Si-$SiO_2$ interfaces are located at $x = 0$ and back Si-$SiO_2$ interfaces are located at $x = t_{si}$, $L_{eff}$ is the effective channel length , The source-SOI film junction is located

* 17nehagoel@gmail.com
† mkspandey@gmail.com

 © 2017 Sumy State University

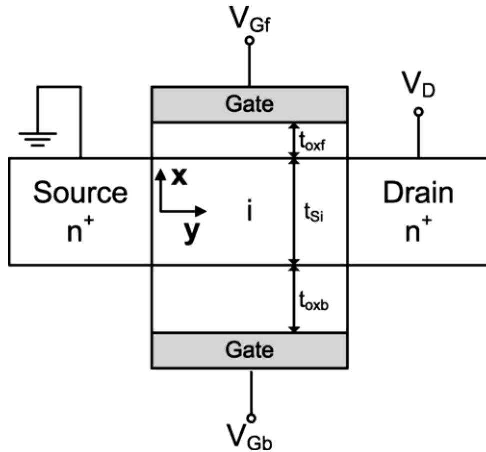


**Fig. 1** – Structure of Double Gate FDSOI MOSFET

at $y = 0$ and drain-SOI film junctions is located at $y = L_{eff.}$, $t_{oxf}$ = gate oxide thickness (front), and $t_{oxb}$ = gate oxide thickness (back), $V_{gf}$ = Applied potential at front gate, $V_{gb}$ = Applied potential at back gate at first, 3D poisson's equation is solved using appropriate boundary condition to obtain threshold voltage and subthreshold slope [16].

### 2.1 Threshold Voltage

The MOSFETs need an external control and is called a switch, which can define the on and off nature. We know, DC voltage is used as the external control and hence MOSFET may be called as voltage controlled device. The threshold voltage is that dc voltage which is needed to switch on the MOSFET at which a reasonable drain current is achieved.

In addition to that, Threshold voltage of the n-channel double gate SOI MOSFET is defined as the gate voltage at which the channel gets inverted and electron gets injected from source to channel which depends on dimensions of the device. Some authors have analyzed the effect of SOI film thickness, drain bias, back gate bias and doping concentration on the threshold voltage roll off, varying SOI film thickness [14]. Their results show that SCE are considerably reduced with thinner SOI film thickness because of the good control of the gate over the channel region, but for thicker SOI film, SCE is serious because thicker SOI film is more like bulk structure. In SOI MOSFET devices, short channel effects are less but they are not eliminated completely. These effects can be controlled by using thin film SOI MOSFET so that SCE can be reduced. Scaling of gate oxide thickness has also been used in controlling SCE, as we increase Oxide thickness, Gate Controllability increases and hence Short channel effects reduces. The behavior of threshold voltage with respect to Back gate voltage has been shown in Fig 2.1 to study the short channel effects.

### 2.2 Subthreshold Slope

In the design of SOI MOSFET, Subthreshold slope is a most important parameter of subthreshold characteristics for analog and digital applications [10-13]. As we know, MOSFET is a voltage controlled device, but drain current increases gradually with gate voltage instead of step increase. Subthreshold current is basically weak inversion current is the magnitude of drain current below threshold voltage. It is also called as subthreshold leakage, as it is not on current instead flow through drain with no required gate bias applying. Subthreshold current can be useful in analog circuits to generate different functions [17], but mostly degrade digital circuits made using MOS device.

The subthreshold slope is a measure of rate of increase of threshold voltage with Drain current of and is measured on log scale as V/Decade and has ideal magnitude of 60.

## 3. RESULTS AND DISCUSSION (EXPERIMENTAL)

Due to Short channel effects subthreshold voltage swing increases and threshold voltage decreases and hence causes to have limitation of scaling. Simple analytical models can be used to have short channel behavior through studying device operation.

### 3.1 Threshold Voltage

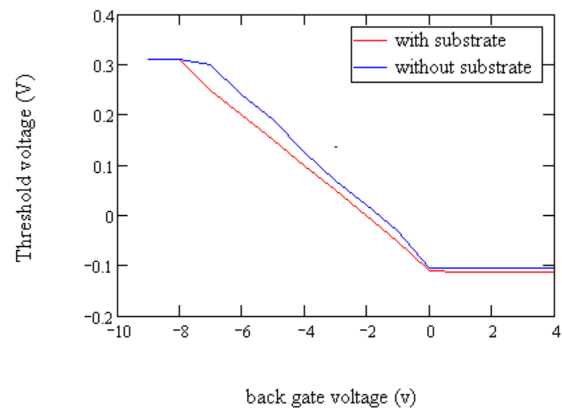


**Fig. 2.1** – Change in threshold voltage with back gate voltage considering substrate effect

Fig 2.1 shows the Controllability of Threshold voltage on application of back gate bias voltage with and without substrate. We can see from the figure that before application of negative Back Gate bias voltage graph behavior are same for both with and without substrate effect, as back gate voltage is applied a voltage drop occurs across the substrate occurs which caused develop a finite drop in the Substrate and hence threshold voltage decreases, causing the graph to slightly downwards.

### 3.2 Subthreshold Slope

Due to scaling down the device length in nm range, sub threshold slope caused to increase, so this is limiting factor which reduces the performance of device on scaling

down the dimensions. This can be effectively controlled by changing the SOI Film Thickness and application of Back gate bias voltage. The most advantageous feature of FD SOI MOSFETs is its steep subthreshold slope.

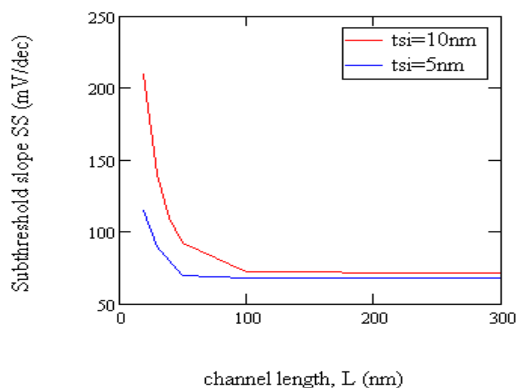


**Fig. 2.2** – Variations in Subthreshold Slope with channel length at different $t_{si}$

As Shown in Fig. 2.2, Sub threshold Slope Variation with Scaling down the Gate length is studied at Different SOI Film thickness, at 5 nm and at 10 nm. It can be seen that subthreshold slope get decreases with lower SOI film thickness, Graph get shifted to downwards and hence subthreshold slope can be controlled by reducing the SOI thickness.

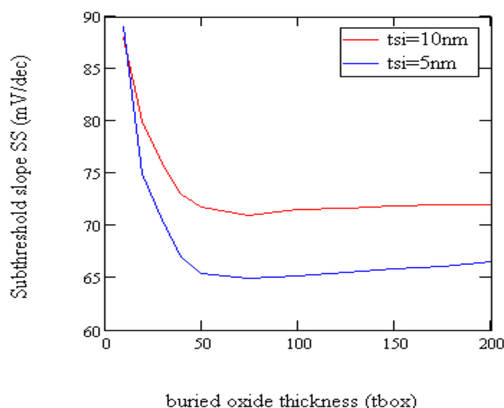


**Fig. 2.3** – Variations in Subthreshold Slope with buried oxide thickness at different $t_{si}$

As shown in Fig. 2.3, subthreshold Slope Variation with buried Oxide thickness has been studied at Different SOI Film thickness, at 5nm and at 10 nm, It can be seen that subthreshold slope get decreases with lower SOI film thickness, Graph get shifted to downwards and hence subthreshold slope can be controlled by reducing the SOI thickness. It can also be notice from here that subtreshold slope swing is having less value with respect to buried oxide thickness as compare to Gate length.

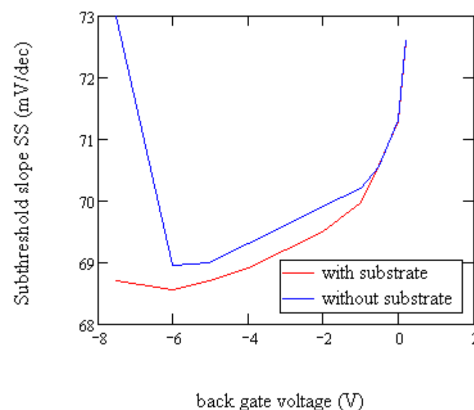


**Fig. 2.4** – Variations in Subthreshold Slope with Back Gate Voltage at different $t_{si}$

As Shown in Fig. 2.4, Sub threshold Slope Variation with Substrate and Without Substrate effect has been studied with respect to Back gate Voltage, It is seen that sub threshold slope is having lower values in case of with substrate effect.

## 4. CONCLUSION

Short channel effects suppression through better control on fluctuations of threshold voltage and minimize of subthreshold voltage slope has been studied. It has been shown that Subthreshold swing and threshold voltage fluctuations are reduced when substrate effects are considered. Also subthreshold slope can be considerably reduce by reducing the SOI film thickness.

## ACKNOWLEDGMENT

This Research Work is recognized by SRM University, Chennai.

## REFERENCES

1. W. Yang, Z. Yu, L. Tian, *IEEE T. Electron Dev.* **54**, 1140 (2007).
2. X. Liang, Y. Taur, *IEEE T. Electron Dev.* **51**, 1385 (2004).
3. Y. Omura, H. Konishi, S. Sato, *IEEE T. Electron Dev.* **53**, 677 (2006).
4. R. Zhang, K. Roy, *IEEE T. Electron Dev.* **49**, 852 (2002).
5. N. Barin, M. Braccioli, C. Fiegna, E. Sangiorgi, *IEEE T. Nanotechnol.* **6** (2007).
6. A. Lazarol, A. Cerdeira, M. Estrada, B. Nael, *Spanish Conf. Electron Dev.* **1**, 1 (2009).
7. K. Roy, S. Mukhopadhya H. Mahmoodi, *Proc. IEEE,* **91**, 305 (2003).
8. J. Bansal, N. Sharma, S.P. Kumar, R. Chaujar, M. Gupta, R.S. Gupta, *Proc. Int. Conf. Microwave* (2008).
9. T. Ernst, S. Cristoloveanu, G. Ghibaudo, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, K. Murase, *IEEE T. Electron* **50**, 2003.
10. T. Numata, *IEEE T. Electron Dev.* **51** (2004).

11. S.A. Vitale, P.W. Wyatt, N. Checka, J. Kedzierski, C.L. Keast, *IEEE Proc.* **98**, 333 (2010).
12. N. Fasarakis, T. Karatsori, D.H. Tassis, C.G. Theodorou, F. Andrieu, O. Faynot, G. Ghibaudo, *IEEE T. Electron Dev.* **61**, 969 (2014).
13. J. Widiez, J. Lolivier, M. Vinet, T. Poiroux, B. Previtali, F. Daugé, *IEEE T. Electron Dev.* **52**, 1772 (2005).
14. S.K. Vishvakarma, A.K. Saxena, S. Dasgupta, T.A. Fjeldly, *International Workshop on Electron Devices and Semiconductor Technology* (2009).
15. H. Lee, H. Nah, J.H. Lee, D.G. Kang, Y.J. Park, H.S. Min, *Solid State Electron.* **46**, 1169 (2002).
16. G. Katti, N. DasGupta, A. DasGupta, *IEEE T. Electron Dev.* **51**, 22 (2004).
17. X. Liang, Y. Taur, *IEEE T. Electron* **51**, 8 (2008).
18. N. Goel, M.K. Pandey, *J. Nano- Electron. Phys.* **8**, 01041 (2016).
19. N. Goel, M.K. Pandey, *Int. J. Electron. Electrical Comp. Syst.* **9** (2014).