JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. 9 No 1, 01030(4pp) (2017)
ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том 9 № 1, 01030(4cc) (2017)

Two Dimensional Modeling of III-V Heterojunction Gate All Around Tunnel Field Effect Transistor

Manjula Vijh[1,2], R.S. Gupta[3], Sujata Pandey[4,*]

[1] *Amity University Uttar Pradesh, Noida, India*
[2] *Amity School of Engineering and Technology, New Delhi, India*
[3] *Maharaja Agrasen Institute of Technology, New Delhi, India*
[4] *Amity Institute of Telecom Engineering and Management, Amity University Uttar Pradesh, Noida, India*

(Received 06 December 2016; revised manuscript received 08 February 2017; published online 20 February 2017)

Tunnel Field Effect Transistor is one of the extensively researched semiconductor devices, which has captured attention over the conventional Metal Oxide Semiconductor Field Effect Transistor. This device, due to its varied advantages, is considered in applications where devices are scaled down to deep sub-micron level. Like MOSFETs, many geometries of TFETs have been studied and analyzed in the past few years. This work, presents a two dimensional analytical model for a III-V Heterojunction Surrounding Gate Tunneling Field Effect Transistor. 2-D Poisson's equation in cylindrical coordinates has been solved to derive the expression of Surface Potential and threshold voltage of the device. A broken gap GaSb/InAs heterostructure has been considered in this work. Variation of potential profiles are shown with different gate and drain biases, by varying radius of the transistor,and different gate metals. Also, variation of threshold voltage is shown with respect to channel length and radius of the nanowire.

Keywords: Surrounding gate Tunnel FET, Heterojunction, Surface Potential, Threshold Voltage, Broken-gap.

DOI: 10.21272/jnep.9(1).01030 PACS numbers: 67.72.uj, 61.82.Fk, 71.55.Eq,85.30.De

1. INTRODUCTION

Due to an increasing demand for low power consumption in electronic circuits, semiconductor devices have been scaled down tremendously in the past few years. As device dimensions are scaling down, traditional MOSFETs are facing certain design challenges such as, high subthreshold slope (SS), high leakage currents, and many other short channel effects. This miniaturization of semiconductor devices has led to extensive research in the field of device physics where researchers are modeling new devices which can replace existing devices. One of these devices is Tunnel Field Effect Transistor (TFET), which is considered as a suitable replacement of traditional MOSFET. The main difference between MOSFETs and TFETs lie in the working phenomenon of both these devices. The mechanism of raising or lowering an energy barrier to control the flow of current is the main working principle of a MOSFET. On the other hand, Tunnel FETs work on the principle of tunneling, where carriers tunnel through a potential barrier between source and the channel. Due to this built in tunnel barrier, Tunnel FETs are more immune to short channel effects, show small leakage current and provide SS below 60 mV/decade. These advantages come with a trade-off, and that is, TFETs are afflicted to low ON current. To improve the I_{ON} of a TFET, many design modifications have been proposed by researchers. These include, alterations in device geometry (DGTFETs, GAA TFETs), Band-Gap engineering, Heterojunction TFET, carbon nanotube TFETs etc. III-V semiconductor compounds have also gained a tremendous attention in improving Ion of TFETs. In comparison to homojunction TFET, heterojunction TFETs can achieve high tunnel current. [1-4].

This paper proposes a mathematical model of a III-V Heterojunction Surrounding Gate Tunnel FET, by solving 2-D Poisson's equation in cylindrical coordinates. A broken gap alignment of GaSb-InAs junction at the source end has been taken into consideration. Broken gap alignment gives better performance as compared to notched gap and staggered gap alignments. [5-6]

2. DEVICE STRUCTURE AND MODEL

The cross-sectional view of GaSb-InAs Heterojunction Gate All Around Tunnel FET is shown in Fig. 1. It is an *n*-channel device with Channel length (L) = 22 nm, Radius (R) = 10 nm, oxide thickness (T_{ox}) = 5 nm, body doping (N_a) = 10^{21}/cm^3, source/drain doping (N_s/N_d) = 10^{15}/cm^3, and gate work function = 5.1 eV.

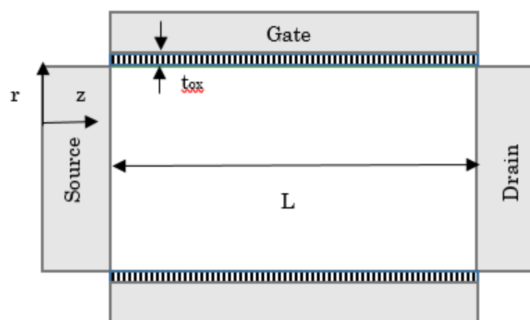

Fig. 1 – A GaSb-InAs Heterojunction GAA TFET: Cross sectional view

2.1 Analytical Model

The potential profile in the channel region is modeled

* spandey11@gmail.com

 © 2017 Sumy State University

by solving 2-D Poisson's equation in cylindrical coordinates, which is given by:

$$\frac{1}{r}\frac{\partial\left[r\frac{\partial\psi(r,z)}{\partial r}\right]}{\partial r}+\frac{\partial^2\psi(r,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{InAs}} \quad (1)$$

where z is the position along the channel, r is the radial distance, q is the charge of an isolated atom, N_a is the acceptor concentration, $\psi(r, z)$ is the potential of the device and ε_{InAs} is the permittivity of InAs channel.

The potential can be expressed as a sum of two terms, i.e. $\psi_0(r)$, and $\psi_1(r, z)$; where $\psi_0(r)$ is the solution of 1-D Poisson equation, and $\psi_1(r, z)$ is the solution of homogeneous Laplace equation [7-8]. Hence, the potential can be written as:

$$\psi(r,z)=\psi_0(r)+\psi_1(r,z) \quad (2)$$

where

$$\frac{\partial^2\psi_0(r)}{\partial r^2}+\frac{1}{r}\frac{\partial\psi_0(r)}{\partial r}=\frac{qN_a}{\varepsilon_{InAs}} \quad (3)$$

$$\frac{\partial^2\psi_1(r,z)}{\partial r^2}+\frac{1}{r}\frac{\partial\psi_1(r,z)}{\partial r}+\frac{\partial^2\psi_1(r,z)}{\partial z^2}=0 \quad (4)$$

Equations (3) and (4) can be solved by using the following boundary conditions:

- Electric field at the center of the channel is zero, i.e.

$$\left.\frac{\partial\psi(r,z)}{\partial r}\right|_{r=0}=0 \quad (5)$$

- The electric field displacement at the gate and channel interface is given by:

$$\left.\varepsilon_{InAs}\frac{\partial\psi(r,z)}{\partial(r)}\right|_{r=R}=C_{ox}\left[V_{GS}-\varphi_{MS}-\psi(r=R,z)\right] \quad (6)$$

where V_{GS} is the gate to source voltage, φ_{MS} is the work function between the metal and semiconductor layer, and C_{ox} is the oxide capacitance.

- The potential at the source side, i.e. at z=0 is given by:

$$\psi(r,0)=V_{biSource} \quad (7)$$

- The potential at the drain side, i.e. at z=L is given by:

$$\psi(r,L)=V_{biDrain}+V_{DS} \quad (8)$$

where V_{DS} is the drain to source voltage.

The expression for surface potential can be derived by solving equation (2) for $\psi_0(r)$ and $\psi_1(r, z)$ respectively.

$\psi_0(r)$ is the solution of 1D Poisson's equation and can be easily obtained using parabolic approximation method. Expressing $\psi_0(r)$ as a second order polynomial:

$$\psi_0(r)=x_0+x_1r+x_2r^2 \quad (9)$$

where x_0, x_1 and x_2 are arbitrary constants. Using boundary conditions (5) and (6), solution of equation (3) can be obtained as:

$$\psi_0(r)=\frac{qN_ar^2}{4\varepsilon_{InAs}}+V_{GS}-\varphi_{MS}-\frac{qN_aR}{2C_{ox}}-\frac{qN_aR^2}{4\varepsilon_{InAs}} \quad (10)$$

To obtain $\psi_1(r, z)$, we solve equation (4) by variable separable method, i.e.

$$\psi_1(r,z)=G(r)*H(z) \quad (11)$$

Solving for $G(r)$ and $H(z)$ we get a generalized solution as:

$$\psi_1(r,z)=\sum_{n=1}^{\infty}\left(Ae^{\frac{\lambda_n z}{R}}+Be^{\frac{-\lambda_n z}{R}}\right)*J_m\left(\frac{\lambda_n r}{R}\right) \quad (12)$$

where J_m is the Bessel Function of order m, and λ_n is the Eigen value that satisfies the relation:

$$\frac{\varepsilon_{ox}R}{t'_{ox}\varepsilon_{InAs}}J_0(\lambda_n)-J_1(\lambda_n)\lambda_n=0 \quad (13)$$

where t'_{ox} = R ln $(1 + t_{ox}/R)$. By solving equation (12) using the boundary conditions given by (7) and (8), we can get the value of coefficients A and B as:

$$A=\frac{Y_0(V_{biSource}e^{\frac{-\lambda_nL}{R}}-V_{biDrain})-Y_0V_{DS}-Y_1(e^{\frac{-\lambda_nL}{R}}-1)}{2\sinh(\frac{-\lambda_nL}{R})} \quad (14)$$

$$B=\frac{Y_0(V_{biDrain}-V_{biSource}e^{\frac{\lambda_nL}{R}})-Y_0V_{DS}-Y_1(1-e^{\frac{\lambda_nL}{R}})}{2\sinh(\frac{-\lambda_nL}{R})} \quad (15)$$

where

$$Y_0=\frac{2J_1(\lambda_n)}{J_1^{\,2}(\lambda_n)\lambda_n} \quad (16)$$

and

$$Y_1=y_1+y_2+y_3 \quad (17)$$

where

$$y_1=V_{GS}Y_0 \quad (18)$$

$$y_2=[(-\varphi_{MS}-\frac{qN_aR}{2C_{ox}}-\frac{qN_aR^2}{2\varepsilon_{InAs}})Y_0] \quad (19)$$

$$y_3=-[\frac{qN_a(R^2\lambda_nJ_1(\lambda_n)-2R^2J_2(\lambda_n))}{2\varepsilon_{InAs}J_1^{\,2}(\lambda_n)\lambda_n^2}] \quad (20)$$

Substituting equation (10) and equation (12) in equation (2), we get the complete expression of surface potential of the device.

After calculating the surface potential of the device, the expression for threshold voltage can be obtained using constant current method.

Finally, drain current of this device can be calculated

by calculating the tunneling rate given by Kane's Model [9], and integrating it over the volume of the device.

2.2 Simulated Model

The proposed mathematical model for TFET is validated using TCAD simulations. The simulations have been carried out on SILVACO ATLAS device simulator. The models that have been used are Concentration dependent mobility model, SRH recombination, Auger recombination, Electric field dependent mobility model, Band gap narrowing, and Kane's model for band to band tunneling [10]. Tunneling parameters A_{Kane} and B_{Kane} are used as mentioned in [8, 9].

3. RESULTS AND DISCUSSION

3.1 Surface Potential

Potential profile of the device has been simulated for different gate and drain biases, by varying the radius, and by using different gate materials. The results of the analytical and simulated model are and results are in agreement with each other.

Fig. 2 shows the surface potential profile with varying Vgs, keeping Vds constant. It can be seen that for low Gate voltages tunneling does not take place in the channel region of the device. As the gate bias increases, potential in the intrinsic channel increases and tunneling starts to take place. This results in the formation of lateral electric field.

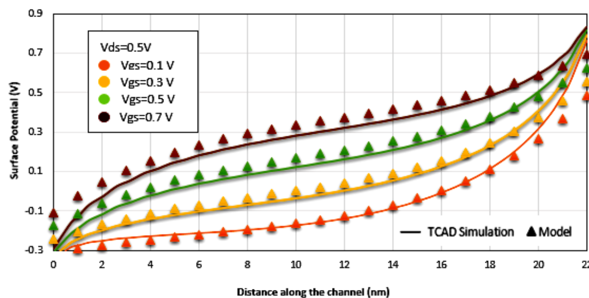

Fig. 2 – Potential profile with varying V_{gs}

Fig. 3 shows the potential profile for different drain voltages, keeping gate to source voltage as constant. As there is an increase in drain voltage, the potential near the drain end increases, but there is not a noticeable change in the potential near the source-channel junction. We can infer that the drain voltage does not impact the tunneling rate at the source side.

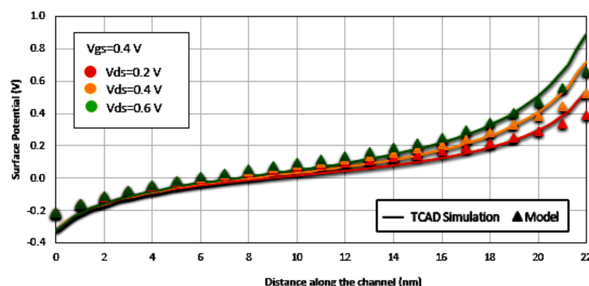

Fig. 3 – Potential profile with varying V_{ds}

Next, the effect of radius on the potential profile is depicted in Fig. 4, 5 and 6. We have simulated the potential for different radii of 5 nm, 7 nm, 10 nm, by varying Gate bias and keeping the drain to source voltage as constant. The channel length is 22 nm for all the simulations. It can be clearly seen that increasing the radius of the TFET for increasing gate voltage, increases the potential along the channel.

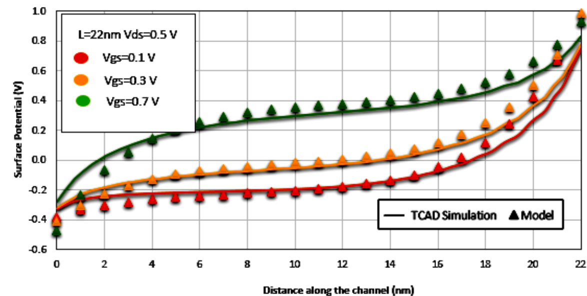

Fig. 4 – Potential profile with Radius = 5 nm

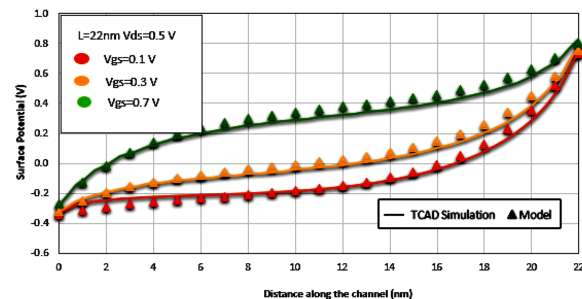

Fig. 5 – Potential profile with Radius = 7 nm

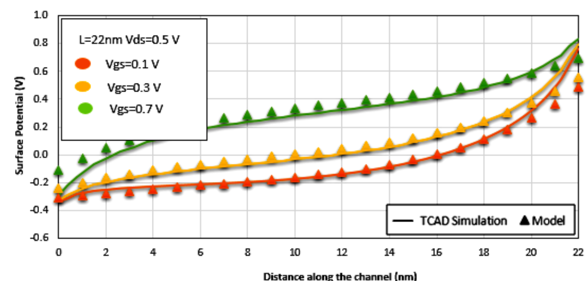

Fig. 6 – Potential profile with Radius = 10 nm

Fig. 7 shows the variation of potential along the channel of the TFET by varying metal work function. It is evident that, with the reduction in metal work function, the tunneling width narrows down which leads to an increase in tunneling probability at the source side, thus increasing the current.

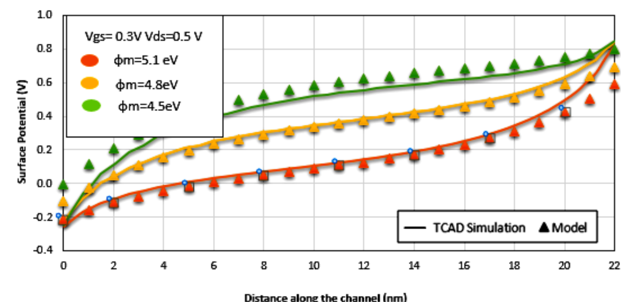

Fig. 7 – Potential profile with different gate metals

3.2 Threshold Voltage

The variation of threshold voltage by changing channel length and radius of the device, is shown in Fig. 8 and 9. Here, gate to source voltage is kept fixed and drain to source voltage is varied. Fig 7 shows that the threshold voltage decreases with increasing drain voltage. Also, as the channel length increases, the threshold voltage increases. Fig.8 shows that as the radius of the channel is increased, threshold voltage decreases.

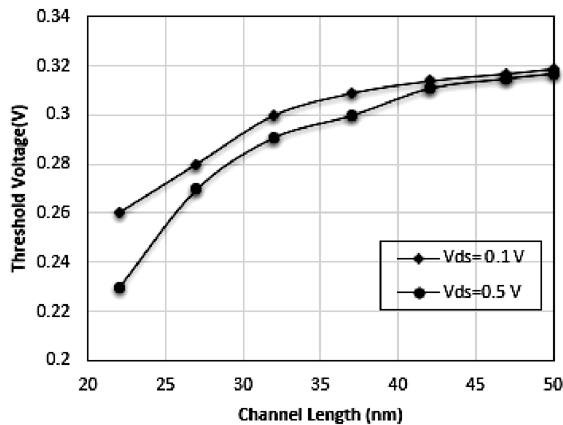

Fig. 8 – Threshold voltage with varying channel length

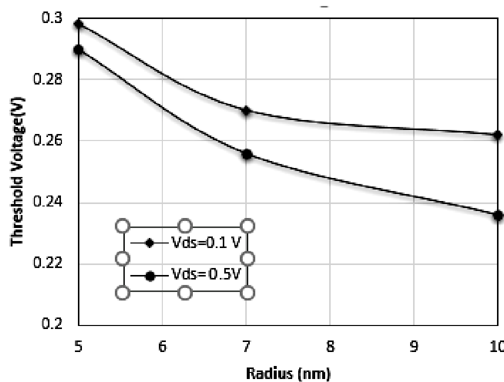

Fig. 9 – Threshold voltage with varying channel radius

3.3 Drain Current

Fig. 9 shows the variation of drain current with applied gate bias. It is seen that a high on current has been achieved in heterojunction surrounding gate tunnel field effect transistor. It is also observed that drain current increases by increasing drain voltage.

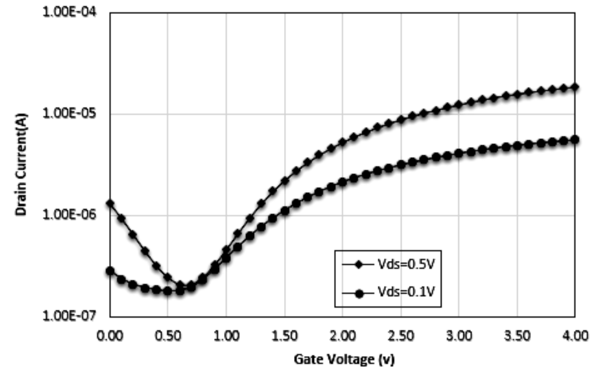

Fig. 10 – Variation of drain current with applied gate voltage

4. CONCLUSION

A III-V Heterojunction Gate All Around Tunnel Field Effect Transistor has been modeled and validated in this work. The analytical model is derived by solving 2-D Poisson's equation in cylindrical coordinates. The expression for surface potential has been derived, and its dependence on various parameters such as gate and drain voltages, channel radius, various gate metals has been discussed. Based on the potential, the threshold voltage of the device has been calculated and modulation of threshold voltage with channel length and radius has been observed. Also, the variation of drain current with gate voltage has been depicted. The results are validated using SILVACO ATLAS device simulator. This work can further be extended to obtain the frequency of the device.

REFERENCES

1. R. Vishnoi, M.J. Kumar, *IEEE T. Electron. Dev.* **61**, No 9, 3054 (2014).
2. T.S. Arun Samuel, N.B. Balamurugan, S. Sibitha, R. Saranya, D. Vanisri, *JEET* **8** No 6, 1481 (2013).
3. M. Luisier, G. Klimeck, *Int. El. Devices Meet (IEDM),* 913 (Maryland, USA: IEEE: 2009).
4. E. Lind, E. Memisevic, A.W. Dey, L.-E. Wernersson, *J-EDS* **3** No 3, 96 (2015).
5. S.O. Koswatta, S.J. Koester, W. Haensch, *IEEE T. Electron. Dev.* **57**, 3222 (2010).
6. Ajay, M. Gupta, S. Bhattacharya, S. Pandey, *India Conference (INDICON),* 1 (New Delhi, India: IEEE: 2015).
7. H.A.E. Hamid, B. Iniguez, *IEEE T. Electron. Dev.* **54**, 572 (2007).
8. R. Vishnoi, M.J. Kumar, *IEEE T. Electron. Dev.* **61**, 2599 (2014).
9. E.O. Kane, *J. Phys. Chem. Solids* **12** No 2, 181 (1960).
10. *ATLAS Device Simulation Software*, Silvaco Int (Santa Clara: CA, USA: 2012).