Journal of Nano- and Electronic Physics
Vol. **9** No 3, 03034(7pp) (2017)

Журнал нано- та електронної фізики
Том **9** № 3, 03034(7cc) (2017)

A Novel Enhanced-Majority-Voter Universal Gate in Quantum Dot Cellular Automata with Energy Dissipation Analysis

S. Umira[1], R. Qadri[1], Z.A. Bangi[1,*], M. Tariq Banday[1], G. Mohiuddin Bhat[2]

[1] *Department of Electronics and IT, University of Kashmir, (J&K), India-190006*
[2] *Faculty of Applied Science and Technology, University of Kashmir, (J&K), India-190006*

(Received 03 April 2017; revised manuscript received 24 April 2017; published online 30 June 2017)

The Quantum effects instigate to dominate device recital when transistor geometries are abridged. Sometimes, transistors refrain to have the properties that mark them beneficial for computational designs. With the intention of keeping pace with Moore's Law, diverse assessing elements must be developed. An alternative prototype to transistor-based logic is Quantum dot cellular automata. This technology has an enormous capability to provide ultra-high density and extremely low power dissipation. These features allow us to develop high-speed, small and high performance circuits for computation and integration. Architectures made in quantum dot cellular automata have been designed by exploiting either the inverter and the majority gate or universal gates like And-Or-Inverter, NAND-NOR-Inverter, FNZ and AIN. A new universal logic gate called as Enhanced Majority Voter Gate is presented in this paper which enjoys better performance with respect to previously announced universal gates. Design of several logic utilities via the proposed Enhanced Majority Voter Gate is also demonstrated. The functionality and power analysis of this universal gate is verified by the QCA Designer and QCA Pro simulation tool where a comprehensive comparison with the hitherto stated designs confirms the reliable performance of the proposed designs. The proposed Enhanced Majority Voter Gate helps us in framing various cryptographic and security based circuits in Quantum dot cellular automata.

Keywords: Nanotechnology, Novel, Quantum-dot Cellular Automata, Universal, Power.

DOI: 10.21272/jnep.9(3).03034 PACS number: 85.35.Be

1. INTRODUCTION

Quantum-dot Cellular Automata (QCA), a field of nanotechnology, has recently been recognized as one of the top six emerging technologies with potential applications for future development of computers [1-3]. Several studies have reported that QCA can be used to design general-purpose computational and memory circuits [4, 5]. QCA has been proposed by Lent et al. at first, and verified experimentally. QCA is expected to achieve precisely high switching speed, high device density and enormously low power consumption.

QCA technology is centered on the communication of bi-stable QCA cells created from four quantum dots. The QCA cell is charged with free electrons, which are able to tunnel between adjacent dots. These electrons have a tendency to reside in the antipodal sites due to their communal electrostatic repulsion. Therefore, there exist two equivalent energetically minimal arrangements of two electrons in QCA cell, as shown in Fig. 1. These two arrangements are signified as cell polarization $P = +1$ and $P = -1$ which represents logic "1" and logic "0", respectively. And then the binary information can be encoded in the charge configuration of the QCA cell.

In order to implement all sequential and combinational logic functions, QCA cells are arranged in such a manner that the polarization of one cell sets the polarization of a nearby cell [2]. According to previous studies, several logic gates and computing devices [6] have already implemented in QCA. Basic implementations that have been reported are the binary wire,

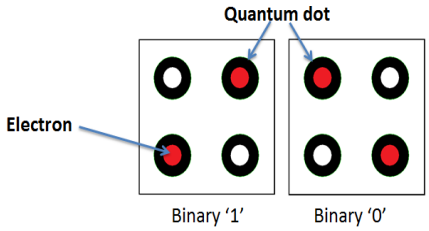


Fig. 1 – Encoding of Binary Information into Two Fully Polarized Diagonals by the QCA Cell [26]

the majority gate, AND gate, OR gate, NOT gate, XOR gate [7], bit-serial adder [8, 9], full adder [7-11], multiplier [12], multiplexer [10, 14], flip-flop [15-17], serial memory [18, 19], parallel memory [20], Arithmetic Logic Unit [10, 20], microprocessor [21], Programmable Logic Array (PLA) [22], etc.

2. RELATED WORK

Momenzadeh et al [23] proposed the design, test, and characterization of a novel complex, yet efficient, QCA logic gate, the Universal AOI gate. A detailed simulation-based analysis and a characterization of QCA defects have been presented. Testing at logic level has also been addressed and appropriate test sets have been developed. Moreover, many two level logic functions can be directly implemented by a single AOI gate. Unlike a conventional MV, the AOI gate operates quite favorably in terms of digital logic synthesis. Simulation results have shown that the Universal AOI gate is robust to manufacturing-

* zubifayaz@gmail.com

process variations and complex designs using the AOI gates resulted in an up-to-23.9% area reduction, while the overall delay has also improved up to a 33.4% reduction.

Bibhash Sen and Biplab K. Sikdar [24] proposed a QCA structure realizing the Universal Gate NAND-NOR-Inverter NNI (A, B, C) = A'B+BC'+C'A'. The functional completeness of NNI has been demonstrated through implementation of logical NAND, NOR and Inverter functions. The characterization of NNI has been reported to focus on the reward of using such gate in designing the QCA based logic circuits.

Bangi et al [25] proposed a novel universal FNZ gate using QCA Designer tool. Various logic functions have been designed and simulated in QCA which are simple combinational logic functions. The designs presented can be used for sequential as well as complex combinational circuits. The proposed design offered fast response, less latency, less power consumption, less area and less cell count.

Ghosal and Biswas [26] proposed the universal structure which is more robust when compared with AOI structure having greater tolerance to misalignment. Adequate operation has been made in accordance with the acceptable levels of polarization which is similar as the noise margin in digital circuits.

Gupta et al [27] proposed a new AIN Gate. Using this gate, one can design various sequential and combinational circuits including logic gates. Further, the proposed designs have been simulated using QCADesigner tool and the comparison of the Universal AIN gate with CMOS, MV, NNI, AOI, and FNZ has also been described.

Mukherjee et al [28] proposed new procedure with its appropriate waveform named as Layered T gate. Gallium Arsenide Layered T is preferred due to its stable noiseless outputs. This gate has also been verified by the standard functions (one/two minterms). Comparison of 2 × 1 multiplexer in terms of fabrication area with other designs has also been done with 37.3% improvement in layout.

3. ACHIEVEMENTS OF THE PAPER

a) A novel universal EMV gate using QCA Designer tool has been proposed.
b) The implementation of different logic functions in QCA using Universal EMV gate has been described.
c) Designs of various QCA universal gates have been compared in order to evaluate the significance of the novel universal EMV gate.
d) Power analysis has been done on the actual universal EMV gate in order to check the various parameters of power dissipation.

4. NOVEL UNIVERSAL EMV (ENHANCED MAJORITY VOTER) GATE DESIGN

Logic gates are the building blocks of digital circuits. In order to understand the computer logic, it is necessary to master the logic operators. A logic gate is an idealized or physical device implementing a Boolean function, that is, it performs a logical operation on one or more logic inputs and produces a single logic output. The output will appear at the output of gate only for certain input signal combinations. Three basic gates such as AND, OR and NOT represent the base of all other gates.

Sometimes, for the cause of a particular design, practicality, existing record or technology, one has to go for other gates viz., NAND and NOR. Charles Sanders Peirce (winter of 1880–81) showed that NOR gates or NAND gates alone can be used to reproduce any logical Boolean expression or functions of all the other logic gates if designed in a suitable way. Therefore, NAND and NOR gates are called the Universal Gates.

There are a number of advantages of universal gates which includes reduction in the hardware (AND & NOT), increase in the speed of circuit design, inexpensive than basic gates, faster switching time, ability to rectify noise and beneficial due to their use in real time applications in order to solve intricate logical issues. Consequently, it is possible to implement all logic gates in Quantum Dot Cellular Automata (QCA) by properly arranging QCA cells in such a way that the polarization of one cell cliques the polarization of a neighboring cell.

The QCA implementation of the universal EMV gate and its symbol is exposed in Fig. 2, comprising of 10 cells via three inputs and one output. The logic function realized by the Universal EMV Gate is as,

$$F = \overline{AB + BC + CA}.$$

The universal EMV gate enjoy vivid advantages of less cell count, less latency, one clock zone, high polarity, fast response, overall area and less power consumption as compared to the designs employed by AOI, NNI, FNZ and AIN universal gates and proved much robust and advantageous. The virtual reality and power analysis of the novel universal EMV gate has been done with the help of QCA Designer and QCA Pro.

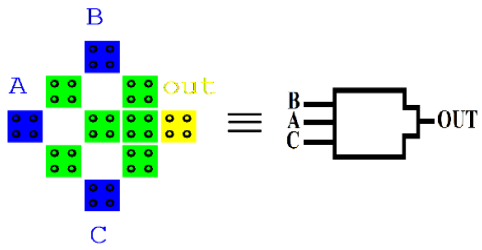


Fig. 2 – QCA Implementation of the universal EMV gate and its symbol

The truth table of the Universal EMV gate is given in Table 1 and simulation results obtained through QCA Designer tool are demonstrated in Fig. 3.

Table 2 lists various logic functions with the implementations achieved by setting the three inputs of Universal EMV gate to different logic states using QCA Designer tool.

Since the EMV gate is universal gate so any logic gate can be implemented. The number of cells, area covered and cell area to overall area for each of the obtained logic functions are given in Table 3.

Table 1 – Truth Table of the Universal EMV Gate

A	B	C	O
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

The QCA implementations of the logic functions using the universal EMV gate have been compared with the conventional CMOS and majority gate, AOI, NNI, FNZ and AIN based QCA methodologies and the comparison results are given in Table 4.

From Table 4, it is clear that the design implementations using the Universal EMV gate are having the advantage in terms of the number of gates. The QCA implementations of various logic functions using novel universal gate are shown in Fig. 4a-h.

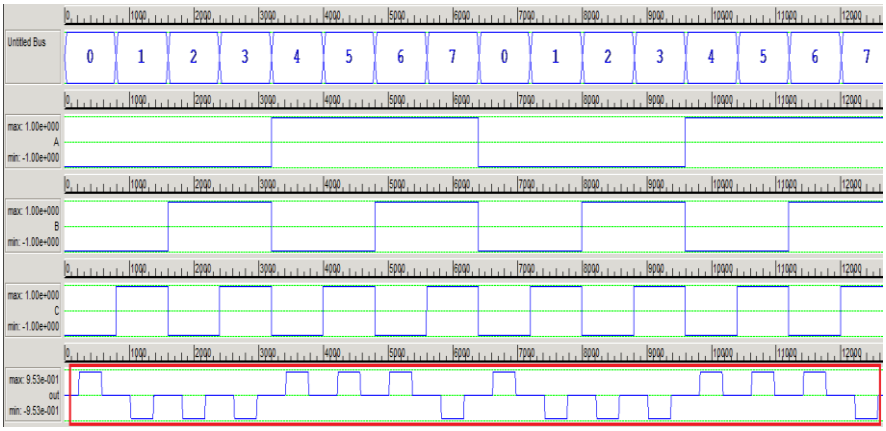


Fig. 3 – Simulation Result of the Universal EMV Gate

Table 2 – Logic Functions obtained from Universal EMV Gate

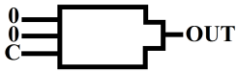
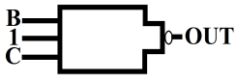
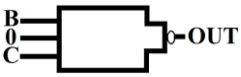
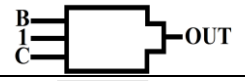
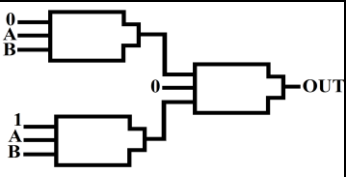
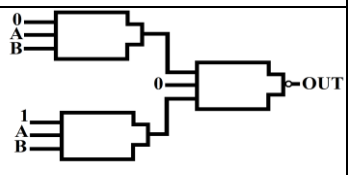
S. No	Gate	Function	Expression Using EMV Gate	EMV Gate Implementation
1	NOT	A'	$EMV(0,0,C)$ or $EMV(B,0,0)$	
2	AND	AB	$(EMV(1,B,C)'$	
3	OR	$A+B$	$(EMV(0,B,C)'$	
4	NAND	$(AB)'$	$(EMV(1,B,C)$	
5.	NOR	$(A+B)'$	$(EMV(0,B,C)$	
6.	XOR	$(A \oplus B)$	$EMV(0, EMV(0, A.B), EMV(1, A, B))$	
7.	XNOR	$(A \oplus B)'$	$EMV(0, EMV(0, A.B), EMV(1, A, B))'$	

Table 3 – Various Logic Functions Using Universal EMV Gate

S. No	Gate	Function	Total Number of Cells	Cell Area (nm^2)	Total Area (nm^2)	Cell Area / Total Area	Number of Clock Zone
1	NOT	A'	10	3240	9604	0.337	1
2	AND	AB	10	3240	9604	0.337	1
3	OR	$A + B$	10	3240	9604	0.337	1
4	NAND	$(AB)'$	10	3240	9604	0.337	1
5	NOR	$(A + B)'$	10	3240	9604	0.337	1
6	XOR	$(A \oplus B)$	35	11340	39204	0.289	2
7	XNOR	$(A \oplus B)'$	35	11340	39204	0.289	2

Table 4 – Comparison of the EMV Gate Design with Previously Reported Designs

Design Type	Number of Gates Required for the Design of Logical Structure						
	Inverter	AND	OR	NAND	NOR	XOR	Ex-NOR
CMOS Design	Transistors						
	2	4	4	4	4	8	8
Majority Gate (MG) Design	NA	1MG	1MG	1MG & 1 NOT Gate	1 MG & 1 NOT Gate	3 MG & 2 NOT Gate	3 MG & NOT Gate
AOI Gate Design [23]	1	2	2	1	1	4	3
NNI Gate Design [24]	1	4	4	4	4	4	4
FNZ Gate Design [25]	1	2	2	1	1	3	3
DPNNI Gate Design [26]	1	2	2	1	1	NA	NA
AIN Gate Design [27]	1	2	2	1	1	NA	NA
Layered T Gate Design [28]	1	2	2	1	1	NA	NA
Proposed Gate Design	1	1	1	1	1	3	3

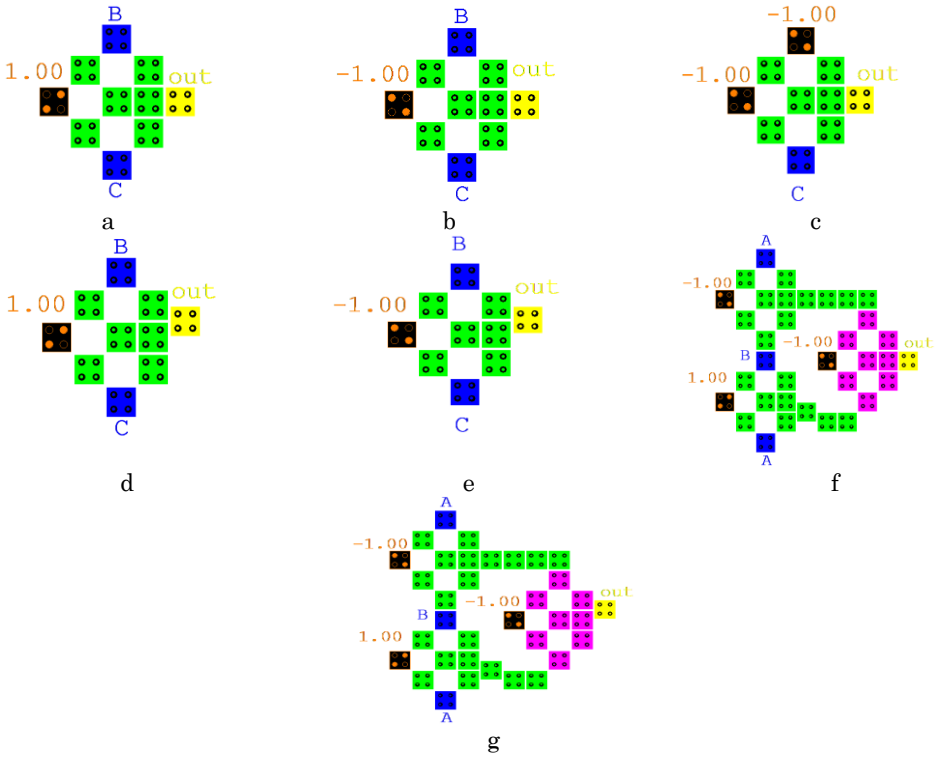


Fig. 4 – Implementation of Logic Functions shown in Table 2 using the Universal EMV gate (a) NAND Gate (b) NOR Gate (c) NOT Gate (e) AND Gate (f) OR Gate (g) XOR Gate (h) XNOR Gate

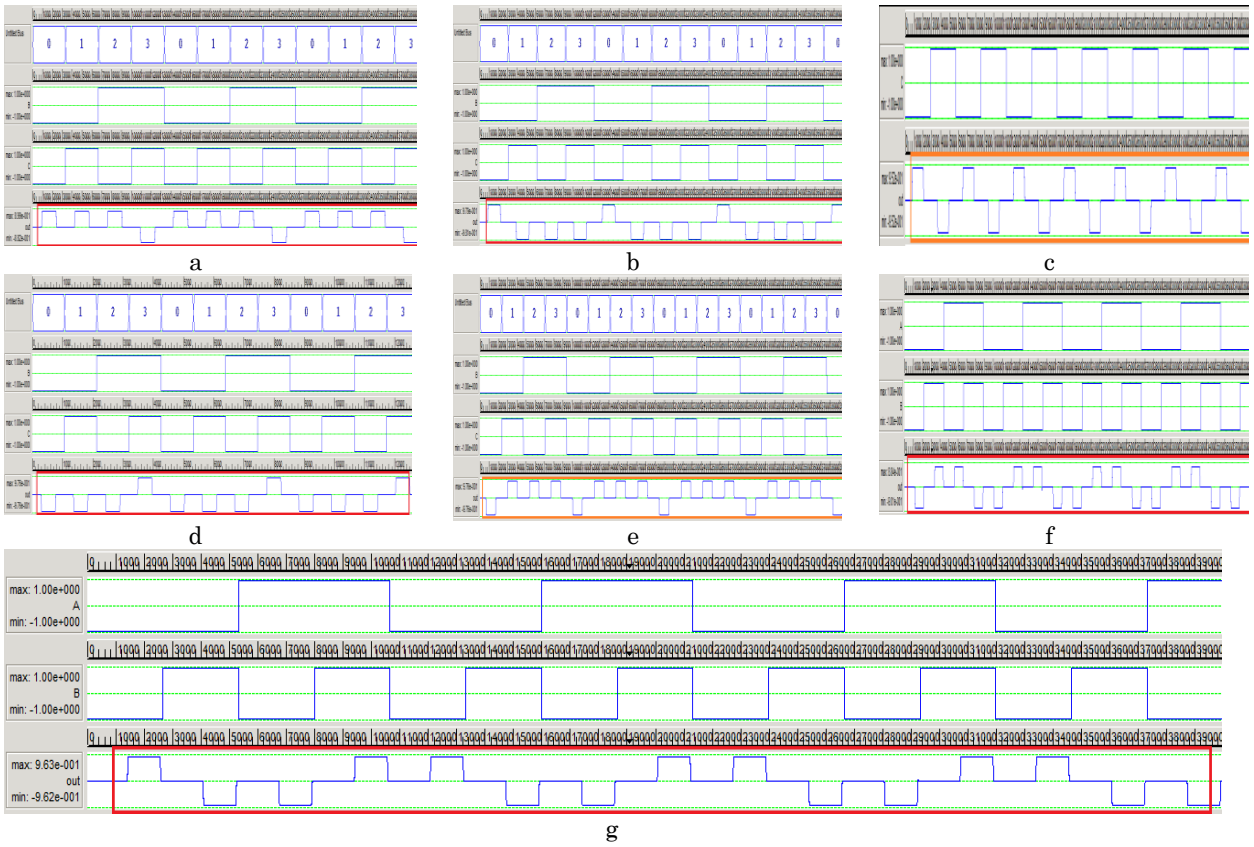


Fig. 5 – Simulation Results of the Functions Mentioned in Table 2 (a) NAND Gate (b) NOR Gate (c) NOT Gate (e) AND Gate (f) OR Gate (g) XOR Gate (h) XNOR Gate

5. QCA IMPLEMENTATION OF VARIOUS LOGIC FUNCTIONS USING THE UNIVERSAL EMV GATE

The simulation results of the logic functions listed in Table 2 are given in Fig. 5a-h. It has been evaluated that it becomes very easy to design various logic functions using novel Universal EMV gate as compared to previously reported universal gates.

Main feature of this novel universal EMV gate is that there is no translation which makes the whole design to occupy 9604 nm² (0.01 μm²) area and the number of gates required to frame all the basic logic gates is exactly one.

6. UNIVERSAL EMV GATE WITH ASSORTED SEMICONDUCTORS

QCA designs can be implemented using two interactions; electrostatic and magnetic interactions. Electrostatic interaction involves semiconductor, metal-dot and molecular interactions. Now we will discuss semiconductor interaction as this paper is concerned about the same type of interaction.

Novel Universal EMV Gate has been simulated by means of assorted semiconductors given in Table 5. This table highlights the materials, their relative permittivities or dielectric constants with output energies of each material on universal EMV Gate.

Table 5 – Verification of Universal EMV Gate with assorted Materials [28]

S. No	Semiconductor Material	Dielectric Constant/Relative Permittivity	Output Polarization	
			Max	Min
1.	Gallium Nitride (GaN)	8.9	+0.944	– 0.944
2.	Alumunium Nitride (AlN)	9.14	+0.942	– 0.941
3.	Gallium Phosphide (GaP)	11.1	+0.920	– 0.920
4.	Silicon(Si)	11.7	+0.913	– 0.913
5.	Indium Phosphide (InP)	12.5	+0.903	– 0.904
6.	Gallium Arsenide (GaAs)	12.9	+0.900	– 0.899
7.	Gallium Antimonide (GaSb)	15.7	+0.865	– 0.865
8.	Indium Arsenide (InAs)	15.15	+0.871	– 0.871
9.	Germanium (Ge)	16.2	+0.858	– 0.858
10.	Indium Antimo.nide (GaSb)	16.8	+0.851	– 0.851

By doing so, a researcher is able to generate an idea of the suitable material use.

From Table 5, it is observed that with increase in the dielectric constant or relative permittivity of various semiconductor materials, the force of interaction between the two charged particles decreases and hence the output polarization of universal EMV gate also decreases as per the coulombs law of electrostatic interaction given in Equation below.

$$F = K\frac{q_1 q_2}{r^2}$$

where $K = 1/(4\pi\varepsilon_0\varepsilon_r)$, ε_0 – absolute permittivity of free space or vacuum and ε_r is the relative permittivity or dielectric constant. Here results reveal that with increase in the value of ε, the output polarization produces noisy signals and spikes which disturbs the next levels of circuitry.

7. POWER ANALYSIS OF PROPOSED DESIGN

Besides operational evaluation of the universal EMV gate which confirmed its robustness, a comprehensive power dissipation analysis is achieved.

In evaluating the power dissipation of QCA designs, kink energy acts as an important part because it is openly connected to power dissipation. The energy necessary for the circuit design to stimulate from ground state to first excited state is known as kink energy [29]. An alternate tool used to estimate the power dissipation of QCA designs is called as QCA Pro, which produces the corresponding thermal model for every QCA cell [30]. With QCA Pro tool, the following parameters, Average leakage, switching and energy dissipation of the QCA circuit design has been evaluated as shown in Table 4 which illustrates the energy dissipation assessment of novel

Table 6 – Power Dissipation Values of Universal EMV Gate

Power Dissipation Parameters	Universal EMV Gate at Different Kinks		
Kink Energy (Ek)	0.5	1.00	1.5
Max Kink Energy	0.00148 Ek	0.00148 Ek	0.00148 Ek
Max Energy Dissipation of Circuit	0.01975	0.02129	0.02402
Max Energy Dissipation Vector	2 5	2 5	2 5
Average Energy Dissipation of Circuit	0.00983	0.01348	0.01784
Max Energy Dissipation Among All Cells	0.00462	0.00469	0.00487
Max Energy Dissipation Vector	1 6	1 6	1 6
Min Energy Dissipation of Circuit	0.00259	0.00761	0.013101
Min Energy Dissipation Vector	2 2	2 2	0 4
Average Leakage Energy Dissipation	0.00303	0.0082	0.01367
Average Switching Energy Dissipation	0.00679	0.00528	0.00416

Table 7 – Comparison of Power Analysis with some Previously Reported Designs

	Maximum Energy dissipation of Circuit			Maximum Energy dissipation among all Cell			Average Switching Energy Dissipation		
Universal Gates	0.5 Ek	1.00 Ek	1.50 Ek	0.5 Ek	1.00 Ek	1.50 Ek	0.5 Ek	1.00 Ek	1.50 Ek
FNZ Gate Design [25]	0.02423	0.02415	0.02504	0.00682	0.00669	0.00666	0.00690	0.00596	0.00507
AIN Gate Design [27]	0.02437	0.02473	0.02566	0.00610	0.00613	0.00624	0.01014	0.00886	0.00758
Proposed Design	0.01975	0.02129	0.02402	0.00462	0.00469	0.00487	0.00679	0.00528	0.00416

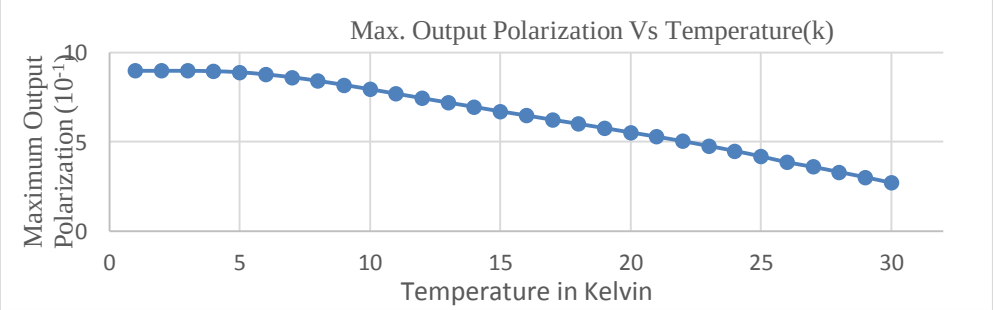


Fig. 6 – Maximum Output Polarization vs Temperature in kelvin graph of universal EMV Gate

universal EMV gate at three discrete kinks (0.5 Ek, 1.00 Ek, and 1.5 Ek) and at temperature 2 K.

With the increase in kink energy, average energy dissipation and average leakage energy dissipation gets increased and average switching energy dissipation gets decreased in universal QCA circuit design.

In addition to above calculations, comparative analysis has also been done with some previously reported universal gate designs viz., FNZ and AIN gates as shown in Table 7 below.

Table 7 reveals the maximum energy dissipation of the circuit, maximum energy dissipation among all cells and average switching energy dissipation respectively. It is observed that the proposed universal gate design has least energy dissipation in comparison to the designs presented in [25] and [27].

The graph between temperature and maximum output polarization in Fig. 6 give the realization regarding the variation in output polarization with increase in temperature. This temperature can be changed in QCA Designer tool using coherence vector engine.

8. CONCLUSION

A novel universal EMV Gate has been introduced in a highly stable manner. Various basic logic gates have been designed in order to make QCA implementation more reliable, efficient, robust and fault tolerant. The performance of Universal EMV gate has been confirmed by QCA Designer where comprehensive comparisons with the hitherto stated designs confirm the reliable presentation of the proposed designs. Further, to increase the reliability of the QCA design, various design concerns, QCA Pro tool has been used in order to find the power dissipation parameters. The proposed EMV gate is widely compared with previously reported universal gate designs (structurally as well as with Energy Dissipation) and proves amazing dominance in approximately all conditions.

REFERENCES

1. M. Wilson, K. Kannangara, J. Smith, M. Simmons, B. Raquse, *Nanotech. Basic Sci. Emerging Tech*. (2002).
2. J. Iqbal, F.A. Khanday, N.A. Shah, *Comm. Inf. Sci.Mgt. Eng.* **3** No 10, 504 (2013).
3. I. Amlani, O. Islamshah, O. Alexei, R.K. Kummamuru, G.H. Bernstein, C.S. Lent, G.L. Snider, *Appl. Phys. Lett.* **77** No 5, 738 (2000).
4. K. Walus, A. Vetteth, G.A. Jullien, V.S. Dimitrov, *Nanotech. Conf*. 2, 160 (2003).
5. A. Vetteth, K. Walus, V.S. Dimitrov, G.A. Jullien, *IEEE Emergi. Telecommunicati. Technologi. Conf*, (2002).
6. T. Lantz, E. Peskin, *IEEE Internatio. Conf. Reconfigurab. Computi. and FPGA's*, 1 (2006).
7. N.A. Shah, F.A. Khanday, Z.A. Bangi., *Comm. Inf. Sci. Mgt. Eng. CISME* **2** No 2, 11 (2012).
8. W. Wang, K. Walus, G.A. Jullien, *IEEE-Nano*. 2, 461 (2003).
9. A. Fijany, N. Toomarian, K. Modarress, M. Spotnitz, *NASA Technical Report* (2003).
10. V. Vankamamidi, M. Ottavi, F. Lombardi, *IEEE T. Comp. Aid. D.* **27** No 1 (2008).
11. K. Kim, K. Wu, R. Karri, *IEEE T. Comp. Aid. D.***1**, 176 (2007).
12. C. My, C. Mi, *J. Electron. Test*. **24**, 313 (2008).
13. I. Hanninen, J. Taka, *Workshp Embedded Comput. Syst. Archi. Modeli. and Simula. SAMOS*, 43 (2008).
14. V. Vankamamidi, M. Ottavi, F. Lombardi, *IEEE T. Comp. Aid. D* 27, 34 (2008).
15. J. Huang, M. Momenzadeh, F. Lombardi, *VLSI J.* **40**, 503 (2007).
16. M. Momenzadeh, J. Huang, F. Lombardi, *IEEE Internati. Symp. Def. and Faul. Toler. in VLSI Systs,* 199 (2005).
17. J. Huang, M. Momenzadeh, F. Lombardi, *Microelectr. J.* 38, 525 (2007).
18. V. Vankamamidi, M. Ottavi, F. Lombardi, *Proceedi. 15th ACM Grt. Lakes Symp. on VLSI.* 201 (2005).
19. V. Vankamamidi, M. Ottavi, F. Lombardi, *IEEE T. Comp.* 57, 606 (2008).
20. V. Vankamamidi, M. Ottavi, F. Lombardi, *IEEE T. Nanotech.* 4, 690 (2005).
21. M.T. Niemier, M.J. Kontz, P.M. Kogge, *Proceedi. 37th Design Automation Conf*. 227 (2000).
22. M. Crocker, X.S. Hu, M. Niemier, M. Yan, G. Bernstein, *IEEE T. Nanotech.* 7, 376 (2008).
23. M. Momenzadeh, J. Huang, M.B. Tahoori F. Lombardi., *IEEE T. Comp. Aid. D.* **24** No 12, 1881, (2005).
24. B. Sen, B.K. Sikdar, *Proceedi. 11th IEEE VLSI Design and Test Symp*. 433 (2007).
25. F.A. Khanday, Z.A. Bangi, N.A. Kant, N.A. Shah, *IEEE Internati. Conf. Multime. Signal Proces. and Communicat. Technolo* (2013).
26. S. Ghosal, B. Wiswas, *Int. J. Comp. Appl*. **74** No 15, 0975 (2013).
27. N. Gupta, C. Lal, J.K. Meena, S. ChandraJain, *IEEE Internati. Conf. Computer, Communic. and Control* (2015).
28. C. Mukherjee, S. Pramanik, D.S. Roy, S. Mondal, A. Sinha, A.G. Roy, S. Bid, S. Chakraborty, *IEEE* (2016).
29. J. Haung, F. Lombardi, Boston, *MA* (2008).
30. S. Srivastava, A. Asthana, S. Bhanja, S. Sarkar., *Proc. IEEE Int. Symp. Ckts Syst*, 2377 (2011).