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Small Signal Parameter Extraction of III-V Heterojunction Surrounding Gate Tunnel Field Effect Transistor

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This work presents simulation study and analysis of nanoscale III-V Heterojunction Gate All Around Tunnel Field Effect Transistor, along with the extraction of small signal parameters of the device. Transfer characteristics and output characteristics of the device were observed. The device is simulated for extraction of small signal parameters such as transconductance, gate-source capacitance, gate-drain capacitance, by varying doping concentration of drain region and channel length. Cut-off frequency of the device is also obtained. The results reported agree well with the data available in literature.

Keywords: Gate All Around Tunnel FET, Heterojunction, Small signal parameters, Broken-gap.

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1. INTRODUCTION

Over the past few years Tunnel field-effect transistors (TFETs) have acquired a lot of attention as compared to MOSFETs. As MOSFETs tend to scale down further, it results in various short channel effects and leakage currents. A lot of research have been carried out in past years to propose innovative device structures using different materials, to overcome the shortcomings arising from MOSFET scaling. One of the promising devices which has proved to diminish the challenges imposed by scaling is Tunnel Field Effect Transistor. TFETs offer various advantages over MOSFETs such as steeper subthreshold slope (SS), low OFF current, lower value of leakage current and negligible short channel effects. The main advantage that TFETs have over conventional MOSFET is that TFET can achieve SS below 60 mv/dec, whereas, because of thermionic emission, MOSFETs have a limitation on achieving steep subthreshold slope. Tunnel field effect transistors, on the other hand work on the phenomena of band to band tunneling of carriers. In spite of the advantages offered by TFETs, this device suffers from some limitations too. Some of them are low ON current and ambipolar behavior of the device. To improve the I_{ON} of a TFET, researchers have proposed different design architectures which include, modifications in device geometry, Band-Gap engineering, Heterojunction TFET, Carbon Nanotube TFETs etc. Researchers are striving to explore new channel materials which can aid in improving the performance of the device. Narrow band gap materials, like III–V semiconductors, have proved to be attractive channel materials that give high tunneling probability. III-V based TFETs have also been reported experimentally. In comparison to homojunction TFET, heterojunction TFETs can achieve high tunnel current [1-3].

In this paper a III-V Heterojunction Surrounding Gate Tunnel FET is simulated and analyzed in terms of its output characteristics, transfer characteristics and small signal parameters, by varying channel length and doping concentration of the drain region. The device is simulated using a TCAD device simulator.

2. DEVICE STRUCTURE

Fig. 1 shows the cross-sectional view of GaSb-InAs Heterojunction Gate All Around Tunnel FET . The surrounding gate structure provides a better electrostatic control of gate over the channel region. The device parameters taken in this paper are: Channel length (L_g) = 22 nm, Radius(R) = 10 nm, oxide thickness (T_{ox}) = 5 nm, source(GaSb) doping (N_s) = 10^{20}/cm^3, drain(InAs) doping (N_d) = 10^{18}/cm^3, intrinsic channel(InAs) region and gate work function = 5.1 eV. The gate dielectric used in the device is HFO_2. A high-k dielectric reduces the tunnel barrier width because of higher band bending. A broken gap alignment of GaSb-InAs junction at the source end has been considered in the design as it gives better performance as compared to notched gap and staggered gap alignments. [4-5] The device is simulated for two different doping concentrations of the drain region, i.e. for N_d = 10^{18}/cm^3 and 10^{19}/cm^3. Also, the cut of frequency of the device is obtained.

2.1 Simulated Model

The simulations are done using SILVACO ATLAS device simulator. The models that have been used during simulations are, Concentration dependent mobility model(CONMOB), SRH recombination, Band gap narrowing model(BGN), and Kane's model for band to band tunneling, with default parameters. [11]. AC analysis of the device is performed to obtain its electrical characteristics. Field dependent mobility model has not been considered for this device.

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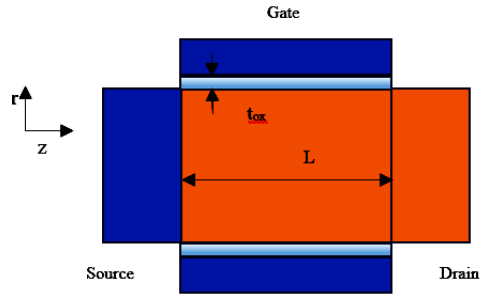

Fig. 1 – A GaSb-InAs Heterojunction Gate All Around TFET

3. RESULTS AND DISCUSSION

3.1 Drain Current

Current conduction in a TFET is based on the phenomena of Band-to-Band tunneling of electrons in which charge carriers tunnel from the valence band of the source region to the conduction band of the channel region. Hence, the tunneling generation rate (G_{btb}) becomes a crucial parameter in determining the drain current. [6] The tunneling generation rate of carriers is given by Kane's model. [10] It is expressed as:

$$G_{btb} = A\frac{|E^{\gamma}|}{\sqrt{E_g}}\exp\left[-B\frac{E_g^{3/2}}{|E|}\right] \quad (1)$$

where A and B are tunneling parameters, E_g is the band-gap of the material, $|E|$ is the magnitude of the electric field, and γ is the pre-exponential factor which is 2 for direct band-gap materials and 2.5 for indirect band-gap materials. The drain current is obtained by integrating the tunneling generation rate over the entire volume of the tunneling region. The drain current, I_d is given by:

$$I_d = q\int G_{btb}dV \quad (2)$$

where q is the electronic charge.

The transfer characteristics of the simulated device with varying drain-to-source voltage were analyzed. Significant ambipolar behavior was observed in the characteristics, which is due to high doping at the drain end. A high dopant concentration at the drain end causes band to band tunneling from the channel to the drain. A dopant concentration must be chosen to suppress ambipolarity and at the same time giving reasonable current levels. Various other methods have been mentioned in the literature to reduce ambipolarity, such as increasing gate drain distance and hence reducing the electric field on drain side, design modifications like overlapping gate on drain etc. [7-9]. Fig. 2 depicts the transfer characteristics of the device at $N_d = 10^{18}/cm^3$ and $10^{19}/cm^3$. Lower drain doping does not change current performance significantly as source and channel regions remain unaffected by the doping concentration of the drain region. However, increasing the drain doping concentration increases ambipolarity in the device. The drain doping should be chosen to keep ambipolarity to its minimum.

The device was simulated for output characteristics by varying gate to source voltage. The drain current increases with increasing V_{ds}, and the device was observed to enter the saturation region at $V_{ds} = 0.4$ V. The effect of drain doping on output characteristics was also observed and it was found that the device with higher drain doping breaks down at a smaller V_{ds} as compared to the device with a smaller drain doping.

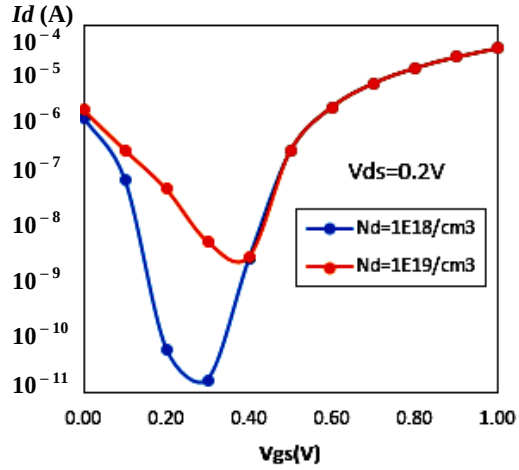

Fig. 2 – I_d-V_g characteristics at $L_g = 22$ nm, with $N_d = 10^{18}/cm^3$ and $10^{19}/cm^3$

3.2 Small Signal Parameter Extraction

In this section, small signal parameters of the device are extracted with different parameters in terms of their transconductance (g_m), and gate-drain capacitance(C_{gd}). These parameters are extracted for two different drain doping i.e. for: $N_d = 10^{18}/cm^3$ and $10^{19}/cm^3$, and three gate lengths ie for $L_g = 22$ nm, 32 nm, and 42 nm. Also, the cut-off frequency of the device is calculated for above mentioned gate lengths.

The transconductance (g_m) and output conductance (g_d) are expressed as:

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \quad (3)$$

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \quad (4)$$

where V_{gs} and V_{ds} are gate to source voltage and drain to source voltage respectively. The cut off frequency of a device is the frequency at which the current gain falls to unity, and is obtained from the following relation:

$$f_t = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \quad (5)$$

where C_{gs} and C_{gd} are gate-source capacitance, and gate-drain capacitance respectively. The variation of transconductance with respect to gate to source voltage, with V_{ds} varying from 0.1 V to 0.3 V is shown in Fig. 3. As V_{gs} is increased, the conductance rises as the number of charge carriers injected from the source increase, and because of the raise in the ON current, the transconductance is also increased. [2] A similar trend is depicted in case of MOSFETs. It was also seen that when the drain doping is changed, there was no variation in transconductance. This is because there is no

significant change in drain current by varying the doping of the drain region, as shown in the transfer characteristics in Fig. 2. [7] It was also observed that the output conductance of the device is higher for high V_{gs}, and it becomes constant with increasing V_{ds}.

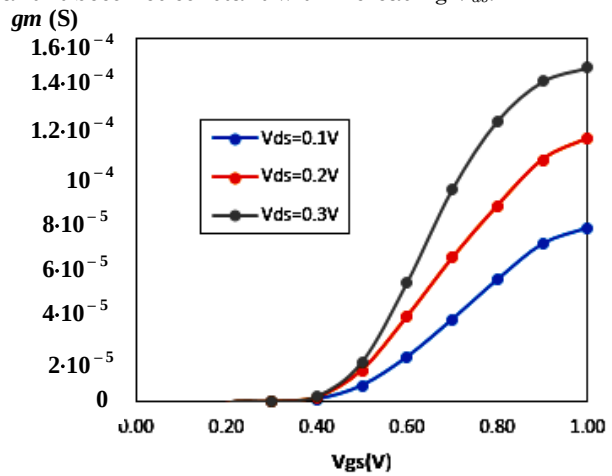

Fig. 3 – Transconductance at $L_g = 22$ nm, $N_d = 10^{18}$/cm^3

The variation of gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) with respect to V_{gs} and V_{ds} respectively was studied and it was inferred that, as the inversion layer in a Tunnel- FET is formed from the drain end toward the source end with increasing V_{gs}, the gate to drain capacitance tends to dominate the total capacitance between the gate and the inversion layer, which increases with increasing V_{gs}. Whereas, as V_{gs} increases, the gate-source capacitance was observed to decrease. [2]

Fig. 4 shows the graph of gate drain capacitance of Heterojunction GAA TFET by varying the drain doping. With increasing V_{gs}, the C_{gs} values of TFET did not show much of a variation. It is because inversion layer in TFET is formed from the drain towards the source unlike in conventional MOSFETs. On the contrary, the C_{gd} values of TFETs increase with inversion charges. With an increase in V_{gs}, the gate-drain capacitance of the device with higher doping shows a high rate of increase, as a high electron concentration, forms an additional inversion capacitance at the drain end. This is depicted in Fig. 4. [7]

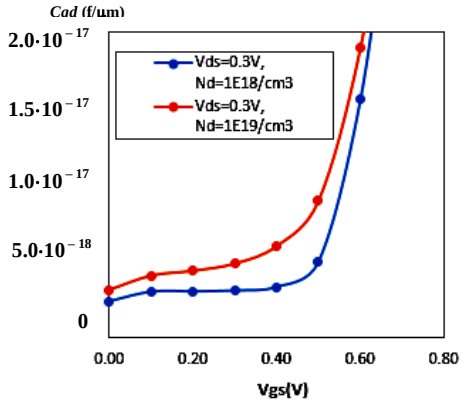

Fig. 4 – Gate-drain capacitance at $L_g = 22$ nm, with $N_d = 10^{18}$/cm^3 and 10^{19}/cm^3

The small signal parameters of the device have also been extracted by varying channel lengths as 22 nm, 32 nm and 42 nm. Fig. 5 shows the C_{gd} values of the device at different gate lengths with respect to gate-source voltage. Once again it was seen that C_{gd} dominates the total capacitance in the device and it increases with increasing V_{gs}. [2]

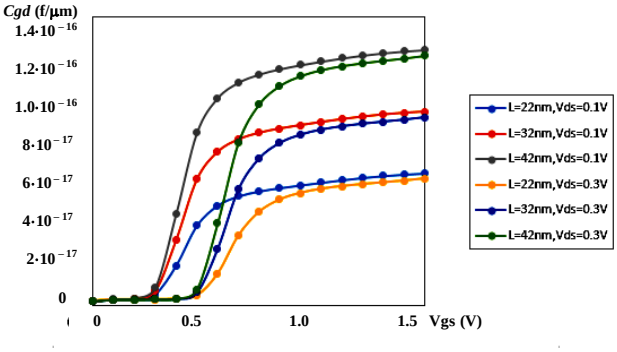

Fig. 5 – Gate-drain capacitance at $L_g = 22$ nm, 32 nm, 42 nm with $N_d = 10^{18}$/cm^3

Using the obtained values of g_m, C_{gs}, and C_{gd}, the cut-off frequency of the device can be obtained using Equation 5. The variation of f_t with respect to gate voltage is depicted in Fig. 6 and the highest cut off frequency of 402 GHz is obtained at $V_{ds} = 0.3$ V and $V_{gs} = 1$ V. By varying the doping concentration of drain, it was observed that TFET with low drain doping shows better performance than one with higher drain doping. The variation of frequency with respect to drain-source voltage at different gate to source voltages was also studied and it was found that frequency increases with increasing bias, and peak cut off frequency is obtained at $V_{gs} = 1$ V. The variation of frequency with increasing channel length was also observed keeping V_{gs} and V_{ds} constant. The cut off frequency was found to decrease with increasing channel length.

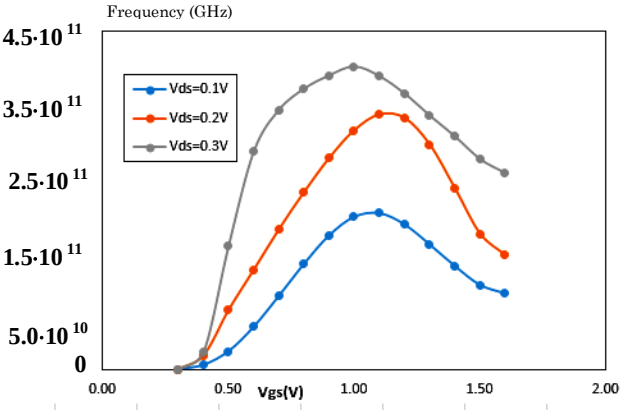

Fig. 6 – Cut-off frequency at $L_g = 22$ nm, $N_d = 10^{18}$/cm^3

4. CONCLUSION

A III-V Heterojunction Gate all around Tunnel FET is simulated using TCAD device simulator. Electrical characteristics of the device were obtained and a detailed analysis is done by varying drain doping concentration and channel length. Lower drain doping reduces ambipolarity in the device. It is observed that the de-

vice gives better performance in terms of drain current, gate drain capacitance and frequency. Transconductance was not greatly affected by varying the drain doping in the device. Gate-drain capacitance was observed to be a major component of the total capacitance of the device, and it increased with increasing gate to source voltage. The cut off frequency of the device was also obtained and it was observed that lowering the doping concentration of the drain showed an improved performance. Also, as gate length increases, the frequency of the device was observed to decrease.

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