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# Analytical Modeling & Simulation of OFF-State Leakage Current for Lightly Doped MOSFETs

Nitin Sachdeva[1], Munish Vashishath[1], P.K. Bansal[2]

[1] *YMCA University of Science & Technology, Faridabad, India*
[2] *Malout Institute of Management & Information Technology, Malout, India*

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Prior to the fabrication of Integrated circuits, the electrical parameters are analytically modeled & simulated using any computer aided design tool. The ever increasing demand of the features of the electronic appliances has forced to put more and more transistors in a small IC chip. The main target of the integrated circuit design and fabrication is to achieve more functionality at higher speed using less power, less area and low cost. Various parameters like threshold voltage, sub-threshold leakage current and sub-threshold slope etc. are analytically derived and simulated to get match with each other. In this paper, 45 nm n-channel metal-oxide- semiconductor field effect transistor (NMOS) has been designed in SILVACO tool to give low off state leakage current by increasing the work function of gate.

**Keywords:** MOSFET, SS, Threshold voltage, SCEs.

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## 1. INTRODUCTION

Actual scaling of Metal oxide semiconductor field effect transistors (MOSFETs) requires not only a size reduction of the device dimensions i.e. length and width of the device but also requires a reduction of all other dimensions including the gate/source and gate/drain alignment, the oxide thickness and the depletion layer widths. Earlier, all the devices are fabricated using heavily doped substrates, but nowadays they are replaced by lightly doped substrates. Due to the use of heavily doped substrate, there is large number of problems for designing the NMOS and other device structures. It provides Latch up problem due to low resistivity and offer the low soft error rates (SER) & it also gives the low shunt to substrate resistance. Heavily doped substrate leads to increase the MOSFET Snapback voltage which is the major cause of latch-up in CMOS circuits. As the substrate resistance is decreased, MOSFET must achieve a higher substrate current to undergo MOSFET Snapback voltage. So instead of using heavily doped substrates, consideration of lightly doped substrates to fabricate the device structures is a good idea because it provides low substrate capacitance and good noise isolation. In Lightly doped substrate, collector to substrate capacitance is less which leads to increase in unity power gain cut off frequency. As compared to heavily doped substrate Snapback voltage is lower in lightly doped. Electrostatic discharge (ESD) robustness is higher than heavily doped. ESD is the main reliability problem which is good in lightly doped. Cost of Lightly doped substrate is lower than highly doped [1, 2].

Work-function engineering is used to reduce off state leakage current in lightly doped substrate devices. Work function is an important parameter in fabrication of device structures. As lightly doped substrate devices gives higher off state leakage current but with the variation of gate work-function from 4.0 - 4.4 *e*V, gives less leakage current in off state.

In this paper, design of NMOS and its electrical characterization of low-power 45 nm channel length have been simulated using SILVACO TCAD Tools. The ATLAS tool of SILVACO software have been used to simulate transistor threshold voltage and relationships with drain current to gate and drain voltages is done and then compared with the analytical results of literature [3].

## 2. METHODOLOGY

The device is designed & simulated in SILVACO TCAD tool consists of ATHENA and ATLAS which is a process and device simulation tool respectively. The fabrication steps to design any device are written in ATHENA and simulated using ATLAS tool. Figure 1 shows the lightly doped substrate NMOS device which shows the doping of the substrate equals to 5*e*15 atoms/cm$^3$ which is a lightly doped substrate.

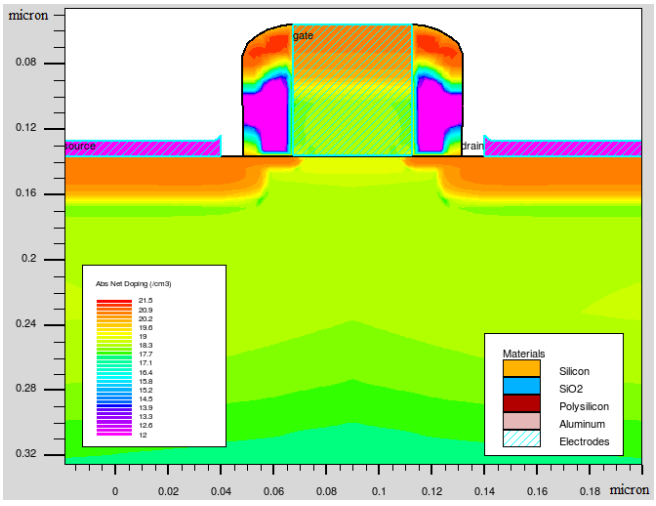


**Fig. 1** – Structure of lightly doped 45 nm NMOS

Table 1 shown above indicates the various device design specifications required for the fabrication of any device. After the device has been designed in ATHENA and by changing the doping concentration with different level of dose in the ATHENA, ATLAS can be used to simulate the I-V curves for the NMOS [3].

 

**Table 1** – Specifications of 45 nm NMOS

| Device Parameters | Value Under-taken |
|---|---|
| Physical Gate Length, Lg | 40 nm |
| Oxide thickness | 1 nm |
| Substrate doping | $5e15\ cm^{-3}$ |
| Vdd(Supply voltage_ | 1.2 V |
| Pwell implant | $1e12\ cm^{-3}$ |
| Vt adjust implant | $5e12\ cm^{-3}$ |
| S/D doping | $3.5e15\ cm^{-3}$ |

## 3. TRANSFER CHARACTERISTICS OF MOSFET

The current voltage characteristics of MOSFET have been plotted in Tony-plot as shown in Figure 2 and Figure 3. The drain current is plotted w.r.t gate voltage at different work-functions. The poly-silicon gate work function has been varied from 4.0 to 4.4 eV.

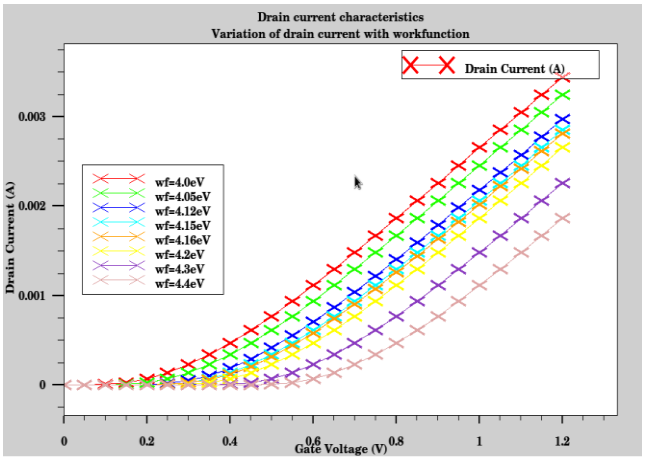


**Fig. 2** – $I_D$ versus $V_G$ Plot in linear Scale for different values of gate work-functions

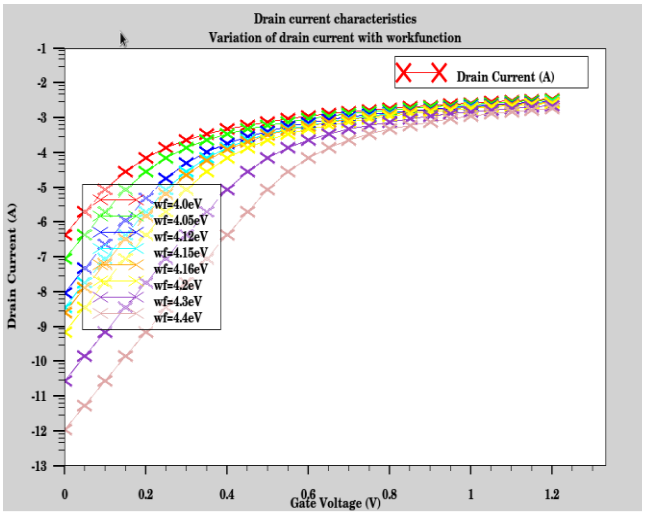


**Fig. 3** – $I_D$ versus $V_G$ Plot in Log Scale for different values of gate work-functions

To obtain the $I_D$-$V_{GS}$ curve, the drain voltage, $V_{GS}$ is varied from 0.05 V to 1.2 V at constant drain voltage. After simulation, the device parameters such as threshold voltage, sheet resistance. On current, leakage current, sub-threshold slope and DIBL can be extracted from this curve. To obtain $I_DV_{DS}$ curve, the gate voltage, $V_{GS}$ was setting to 0.1 V to 1.2 V at constant gate voltage. The output characteristics can be viewed in TONYPLOT.

The result depict that the sub threshold behavior of device improves as the poly gate work function increased to higher value. It is because of the fact that as the increase in poly gate work function increases the corresponding threshold voltage, which in turn reduces the off state leakage current and results in the improvement in the device performance. This is very enviable characteristics of the device for LSTP applications.

Figure 4 shows the variation of drain current with drain voltage at different work-functions range. As the work-function increases, drain current decreases.

Figure 5 depicts the variation of gate current with drain voltage at different gate work-functions.

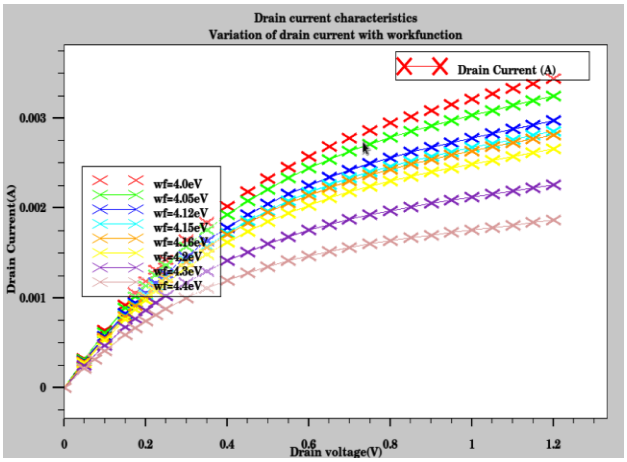


**Fig. 4** – $I_D$ versus $V_D$ Plot for different values of gate work-functions

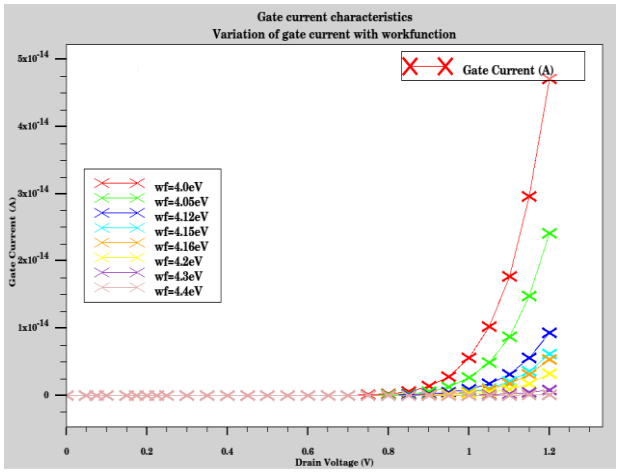


**Fig. 5** – $I_G$ versus $V_D$ Plot for different values of gate work-functions

## 4. SIMULATION RESULTS

### 4.1 Impact of Work-function on Threshold Voltage

Since the work function of the poly gate can be tuned to meet a given threshold voltage requirement, the choice of the material to be used for metal gate in such device will depend on that which of the metal pro-

vides work function suited for given threshold voltage accomplishment. Threshold voltage is the minimum amount of voltage that must be applied at the gate to establish inversion layer or virtual channel or the gate voltage which causes surface inversion is called threshold voltage [4]. The threshold voltage is the summation of the flat-band voltage, twice the bulk potential, the voltage across the oxide due to the depletion layer charge and inversely proportional to the oxide capacitance expressed as in equation 1 below:

$$V_T = V_{FB} + V_C + 2\varphi_F + \frac{q(N_a - N_d)}{C_{ox}} \sqrt{\frac{2\varepsilon_s 2\varphi_F}{q(N_a - N_d)}}, \quad (1)$$

where, the flat-band voltage, $V_{FB}$, is given by:

$$V_{FB} = \varphi_{MS} - \frac{Q_f}{C_{ox}}, \quad (2)$$

$$\varphi_{MS} = \varphi_M - \varphi_S = \varphi_M - \left( \chi + \frac{E_c - E_i}{2q} + \varphi_F \right),$$

$$\varphi_F = V_t \ln \frac{p}{n_i} = -V_t \ln \frac{n}{n_i}.$$

The work-function is the difference between potentials of metal and semiconductor as shown in equation 3 and equation 4 shows Fermi potential. Work-function is the minimum amount of energy which is required to remove an electron from surface of a conducting material to point just outside the surface with zero kinetic energy. Due to complication described in modeling, it is difficult to theoretically predict the work function with accuracy. The work function of the gate tends to be smaller for metals with an open lattice and larger for metals in which the atoms are arranged in much closed structure. The threshold voltage for gate work function ranging from 4.0 to 4.4 eV increases in the present simulation study. It has been found that by increasing the work function of MOSFET, the corresponding threshold voltage increase to a desired value.

Figure 6 depicts the threshold voltage at lower and higher drain voltage equals to 1.2 V and 0.05 V respectively, increases with the increase of work-function of gate electrode. The Poly-silicon gate work function dependence of threshold voltage comes out to be linear relation, which can be verified through the equation (1).

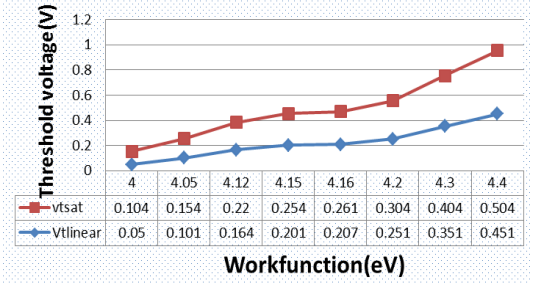


**Fig. 6** – Variation of threshold voltage at higher drain voltage with work-function

The result as depicted in this figure have been obtained for a device having $L_G = 40$ nm, $EOT = 1$ nm and $V_{dd} = 1.2$ V maintaining higher threshold voltage is a key requirement for LSTP logic technology and hence can be achieved more efficiently by increasing work function the gate material [8, 9].

### 4.2 Impact of Work-function on On Current and Off Current

The device on current behavior as a function of gate work function has been illustrated in Figure 7. It is clear that the device on current is sacrificed for decreased the on current with increase in metal gate work function of MOSFET structure.

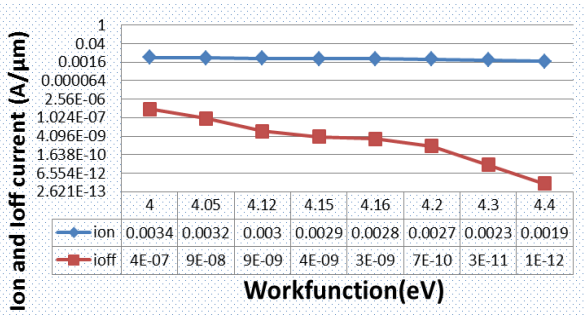


**Fig. 7** – Illustrates the on current and off current of the device

It is clear from the off state current characteristics shown in Figure 7 that a higher gate work function approximately 4.4 eV can fulfill this tolerable off current projection of the MOSFET structure [5].Off current is decreased with increasing the work function [7].

### 4.3 Impact of Work-function on On/Off Ratio

The on/off current obtained from the device simulation has been found to improve significantly with increase in metal gate work function of MOSFET [6]. The on current of the device can be reduced to some extent with an increased gate work function, but an increase in on/off current ratio is a clear indication of overall improvement in drive current with a required low off state leakage current for LSTP technology. Figure 8 shows On/Off ratio increases with the increase of work-function.

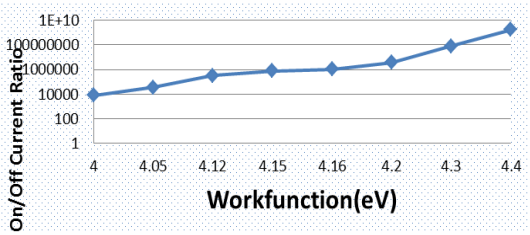


**Fig. 8** – Variation of On/Off current with work-function

### 4.4 Impact of Work-function on Sub-threshold Slope

In long channel devices, the sub-threshold current is independent of the drain voltage for $V_{DS}$ larger than a few $V_T$. The dependent of gate voltage is exponentially the inverse of slope of the $\mathrm{Log}_{10}$ ($I_{DS}$) versus $V_{GS}$ characteristics which is called the Sub Threshold Slope ($S_t$).

$$I_{ds} = \mu_0 C_{ox} \frac{W}{L} (m-1)(V_T)^2 e^{(V_g - V_{th})/mv_T} (1 - e^{-V_{DS}/v_T})$$

$$\text{where } m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{w_{dm}},$$

$$S_t = \left( \frac{d(\log_{10} I_{ds})}{dV_{gs}} \right)^{-1} = 2.3 \frac{mkT}{q} = 2.3 \frac{kT}{q} \left( 1 + \frac{C_{dm}}{C_{ox}} \right).$$

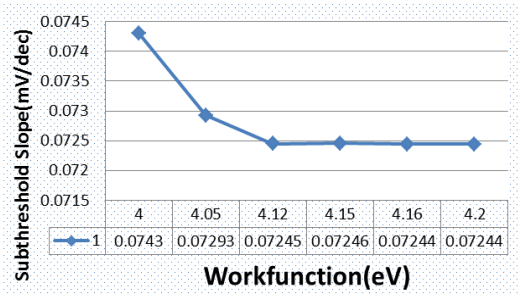


**Fig. 9** – Variation of SSlinear with work-function

Sub-threshold Slope shows how fast the transistor can be turned off (rate of decrease of $I_{OFF}$) when $V_{GS}$ *is* decreased below threshold voltage. For bulk CMOS process can range from 70 to 120 mV/decade. Figure 9 depicts the decrease of sub-threshold current with the increase of work-function as desired for low power devices [10, 11].

## 5. CONCLUSION

The analysis of variation of various parameters with work-function shows that with the increase of work-function of gate electrode, off state leakage current of the device for lightly doped substrate decreaseswhich is desirable factor for low power applications. Moreover, the DIBL and sub-threshold slope also improves but the drain current of the device decreases. So there is a trade-off between on current and off current. After the simulation study, it has been observed that by increasing the threshold voltage, short channel effects decreases and performance of the device increases.

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## REFERENCES

1. *International Technology Roadmap for Semiconductors* (2011).
2. G. James, S. Joseph, V. Mathew, *J. Electron Devices* **8**, 310 (2010).
3. ATLAS Device simulator, SILVACO TCAD software.
4. M.-H. Chiang, C.-N. Lin, G.-S. Lin, *Semicond. Sci. Technol.* **21**, 190 (2006).
5. S. Xiong, J. Bokor, *IEEE T. Electron Dev.* **50** No 11, 2255 (2003).
6. K.-R. Han, B.-K. Choi, H.-I. Kwoni, J.-H. Lee, *Jpn. J. Appl. Phys.*, **47** No6, 4385 (2008).
7. K. Roy, S. Mukhopadhyay, H. Mahmoodi, *Proc. IEEE,* **91**, 305 (2003).
8. C.J. Choi, M.Y. Jang, Y.Y. Kim, M.S. Jun, *Jpn. J. Appl. Phys.* **46** No1, 125 (2007).
9. Farkhanda Ana, Najeeb-ud-din, *JECT* **2**, 4 (2011).
10. L.-Y. Na, K.-J. Baek, Y.-S. Kim, *IEEE T. Electron Dev.* **59** No12, 3273 (2012).
11. Neha Goel, Manoj Kumar Pandey, *J. Nano- Electron. Phys.* **9** No 1, 01022 (2017).