JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. 9 No 5, 05002(4pp) (2017)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том 9 № 5, 05002(4cc) (2017)

Numerical Simulation and Mathematical Modeling of 3D DG SOI MOSFET with the Influence of Biasing with Back Gate

Neha Goel[1], Manoj Kumar Pandey[2]

[1] *Research Scholar, SRM University, NCR Campus Ghaziabad, India*
[2] *Department of ECE, SRM University NCR Campus Ghaziabad, India*

(Received 20 June 2017; revised manuscript received 20 June 2017; published online 16 October 2017)

Design consideration of a fully depleted SOI (Silicon-On-Insulator) MOSFET device by three dimensional mathematical modeling is presented in this paper. To the best of our knowledge, when our device is fabricated in nanometer regime, the threshold voltage changes due to various effects. Back gate voltage plays a significant role on the controlling of threshold voltage. Separation of variable is used to solve the Poisson's three dimensional equation, analytically with suitable boundary conditions for the threshold voltage of double gate SOI MOSFET with the influence of biasing with back gate. In this work, changes in threshold voltage has been calculated and demonstrated that how short channel effects and DIBL can be suppressed with application of Back Gate bias voltage

Keywords: Fully Depleted Silicon on insulator (FDSOI), 3D analytical model, Short channel effects (SCE), Bulk CMOS, Surface potential, Threshold voltage, Drain induced barrier lowering (DIBL)

DOI: 10.21272/jnep.9(5).05002 PACS number: 85.30.tv

1. INTRODUCTION

As the size of device move into deep sub-micrometer regime for realizing good device speed performance and higher integration densities, the characteristics of a MOSFET degrade. However, the main technology, Bulk CMOS will remain for submicron gate ULSI systems. The Double Gate silicon on insulators (SOI) MOSFETs with thin film have superior electrical performances because of the better control of SC (short channel) effects, excellent Latch-up immunity, reduced parasitic capacitances and improved isolation compared to bulk silicon technology [1].

A progress of scaling to improve performance, the short-channel effects (SCE) is required to suppress to improve the reliability of the device. As the channel length shrinks, gate controllability over the channel depletion region reduces, causes to increase charge sharing from source/drain. Due to SCE many reliability issues including the dependence of device characteristics, such as threshold voltage, upon channel length occurs. Channel pinch off and shift in threshold voltage with decreasing length of the channel are remarkable reliability problem which occur due to SCE. Double gate controllability and thinner gate oxides are suppose to be the effective ways to minimize short channel effects.

For instance, gate overdrive increases due to a lower threshold voltage while the leakage current increases exponentially. Dielectric constant, channel doping concentration and band gap are the material parameters and the geometrical dimensions on which the threshold voltage depends are length of channel, thickness of the oxide and thickness of channel. Thus, the threshold voltage also depends on the gate bias (back) voltage of the device with the dependence on geometrical dimensions and material parameters. Therefore, by controlling the bias, specific value voltage has been achieved. Later several author's [2-4] proposed the dependence of threshold voltage for DG-MOSFET with length of the channel, oxide thickness, thickness of the channel and channel doping concentration was investigated.

In the present work, a new model based on threshold voltage is developed for fully (FD) depleted double gate SOI MOSFET based on the solution of the three dimensional Poisson's equation is solved by separation of variables method, hence an investigation is made to calculate the effect of front gate bias and gate bias (back) on the threshold voltage in double gate MOSFET. The influence of gate bias (back) and drain voltage have also been included.

2. SILICON ON INSULATOR (SOI) MOSFET

There are various characteristics of SOI MOSFET due to which it would be beneficial to switch to SOI MOSFET technology. The SOI technology have high speed of operation, elimination of latch up ,high device density ,very less leakage current, power dissipation is small, easier device isolation structure [5] etc.

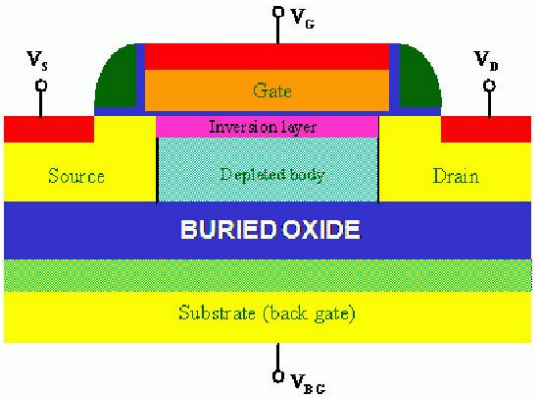

Fig. 1 – Double gate SOI MOSFET with back gate bias

Now, to analyze the structure shown in Fig. 1, The front Si-SiO_2 interfaces are located at $x = 0$ and back Si-SiO_2 interfaces are located at $x = t_{si}$, where t_{si} = SOI film thickness. t_{oxf} = gate oxide thickness (front), and t_{oxb}= gate oxide thickness (back), V_{gf} = Applied potential at front

gate, V_{gb} = Applied potential at back gate. The source-SOI film and drain-SOI film junctions are located at $y = 0$ and $y = L_{eff}$, respectively, where, L_{eff} is the effective channel length. The vertical direction is defined by x and the lateral direction is defined by y. The sidewall of Si-SiO_2 interfaces are located at $z = 0$ and $z = W$, where, the direction along the width of the transistor is defined as z.

3D Poisson's equation for fully depleted SOI film is:

$$\frac{d^2}{dx^2}\Psi(x,y,z)+\frac{d^2}{dy^2}\Psi(x,y,z)+\frac{d^2}{dz^2}\Psi(x,y,z):=\frac{qNa}{\varepsilon si}, \quad (1)$$

where, $\psi(x,y,z)$ is the potential at a particular point (x,y,z) in the SOI film and Na is the channel doping concentration. For solving equation (1), the above equation is separated into 1D Poisson's equation, 2D and 3D Laplace equation as :

$$\frac{d^2}{dx^2}\Psi1(x):=\frac{qNa(x)}{\varepsilon si}, \quad (2)$$

$$\frac{d^2}{dx^2}\Psi2(x,y)+\frac{d^2}{dy^2}\Psi2(x,y):=0, \quad (3)$$

$$\frac{d^2}{dx^2}\Psi3(x,y,z)+\frac{d^2}{dy^2}\Psi3(x,y,z)+\frac{d^2}{dz^2}\Psi3(x,y,z):=0, \quad (4)$$

where, $\psi i = \psi 1(x) + \psi 2(x,y) + \psi 3(x,y,z)$. (A)

A: Solution of $\psi 1(x)$

$$\Psi1:=\left[\Psi sb+Esb(ts-x)+\frac{q}{2\varepsilon si}Na(ts-x)^2\right]\frac{qNa(x)}{\varepsilon si}. \quad (5)$$

B: Solution of $\psi 2(x,y)$

$$\Psi2:=\frac{1}{\sinh(\gamma\cdot Leff)}\left[Vs\cdot\sinh(x\cdot y)+Vr\cdot(\gamma(Leff-y))\right]\left[\sin(\gamma\cdot x)+\frac{\varepsilon si}{\varepsilon ox}toxf\cdot\gamma\cos(\gamma\cdot x)\right]. \quad (6)$$

C: Solution of $\psi 3(x,y,z)$

$$\Psi3:=\mathrm{Psr}\left[\sinh(\chi sr(W-Z))+\sinh(\chi srZ)\right]\frac{\sin(\alpha s(y-Leff))}{\cos(\alpha s\cdot Leff)}\left[\sin(\beta r\cdot x)+\frac{\varepsilon si}{\varepsilon ox}toxf\cdot\beta r\cos(\beta r\cdot x)\right]. \quad (7)$$

Main Equation of Surface Potential (ψi) can be calculated by putting values of $\psi 1$, $\psi 2$ and $\psi 3$ in Equation A.

3. RESULTS AND DISCUSSIONS

The Device parameters used for mathematical modeling are given in the table below:

Table 1 – Device Parameters

Parameters	Value
Gate length, L	70 nm
Device Width, W	50nm
SOI Film Thickness, tsi	15nm
Front gate oxide thickness	2nm
Back gate oxide thickness	300nm
Side wall oxide thickness	15nm

3.1 Surface Potential

The method, separation of variable is used to solve basic 3D Poisson's equation, this is to determine the behavior of surface potential, when Front gate voltage is fixed and gate voltage (back) is assumed. The variation of front surface potential at the front Si-SiO_2 interface (i.e., $x = 0$) at different channel lengths, along with back gate voltage can be shown as in Fig. 2 (uniformly doped SOI.

Here in figure, we determine the variation of front surface potential for n-channel silicon on insulator MOSFETs along with length of the channel at the different values of gate voltage (back), at front Si-SiO_2 interface [6, 7].

It has been seen from the graph that minimum of surface voltage shift towards the source end, remains in the middle of channel for low drain voltage. For a higher drain bias, profile start shifting upward and approaches to drain side.

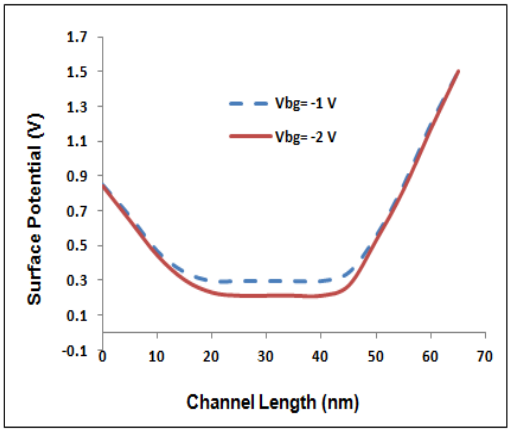

Fig. 2 – Front Surface Potential varies with channel Length at Different Back Gate Voltages

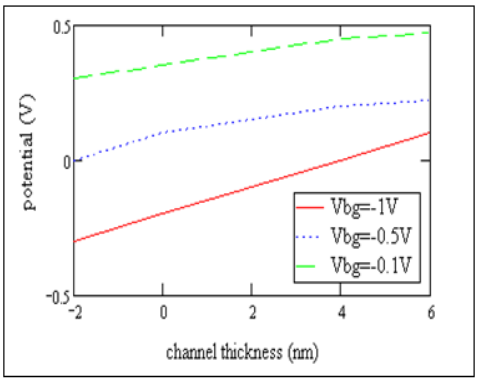

Fig. 3 – Front Surface Potential with thickness of channel at Different back to gate voltages

In Fig. 3 the front surface potential is plotted versus distance along the channel thickness with three differ-

ent values of back gate bias. There is a linear increase of potential from the front gate to the potential of back gate has been observed. For the smaller back gate bias, the curve for potential rises at higher rate. That means, the potential higher at smaller back gate voltage. It has been seen from the graph that surface voltage decreases in the middle range of channel length and remains unchanged. Also surface potential shifts upwards for higher value of channel thickness.

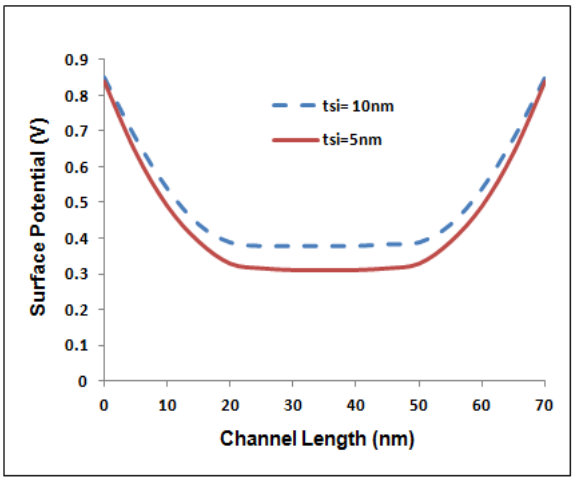

Fig. 4 – Shows Change in front surface potential along channel length at different values of *tsi*

3.2 Threshold Voltage

The threshold voltage [8, 9] is defined as the minimum gate-to-source voltage differential that is needed to create a conducting path between the source and drain terminals. Figs. 5 and 6 shows change in threshold voltage with channel length and thickness at different back gate voltages. From the Fig. 5 it is shown that as the Channel length reduces the threshold voltage decreases and hence curve shifts downward for a low value of gate voltage (Back).

Some Significant features of Fig 6 which shows variation in threshold voltage with respect to thickness of channel at different values of back gate voltages are as below. As the Channel thickness reduces the threshold voltage increases and hence curve shifts upward for a low

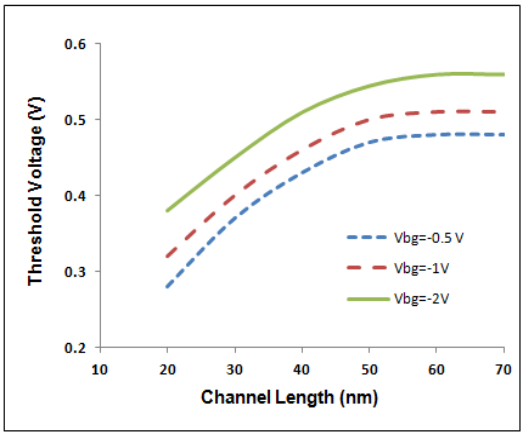

Fig. 5 – Change in Threshold voltage with Length of the channel for different values of back gate voltages.

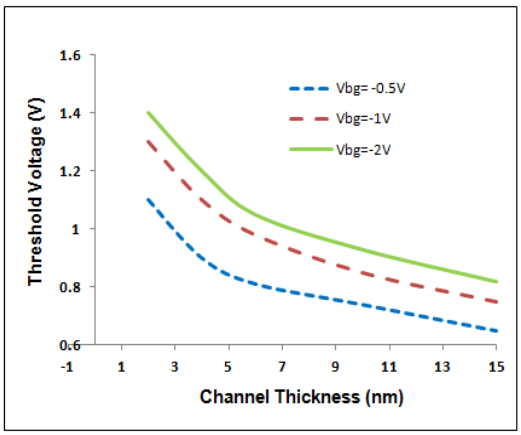

Fig. 6 – Change in threshold voltage with thickness of the channel for different values of back gate voltages

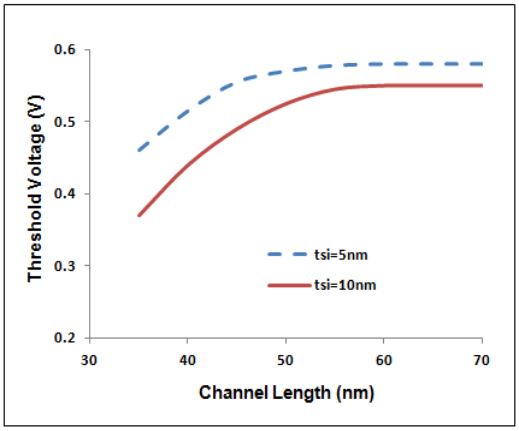

Fig. 7 – Change in Threshold voltage with length of the channel for different values of silicon film thickness

lvalue of gate voltage (Back). The Increments of V_t with decreasing *tsi* accounts for shift in V_t due to short channel effects.

From Fig. 7 it is evident that slope is less sensitive to t_{si} greater for than 5 nm but increases rapidly as *tsi* reduces below 5 nm. The value of slope give us a measurement of the short channel effect. A large back gate bias can be used to suppress the SCE (short channel effects) for a value of *tsi*.

3.3 Drain induced barrier lowering (DIBL)

The punch-through originates from the lowering of barrier close to the source, commonly called as DIBL (Drain induced barrier lowering) [10, 11]. When drain is near the source, the drain bias is capable of influencing the barrier at the source end, such that channel carrier concentration at that location does not remain fixed. When the source barrier is lowered, it causes an injection of extra carriers that increases the current significantly. This results in lowering of the threshold voltage of the transistor. Fig. 8 shows behavior of DIBL with respect to channel length at two different back gate biases. It is evident from the figure that for higher channel length, DIBL is almost independent of the back gate bias but it drops as the back gate biases reduces for short channel lengths.

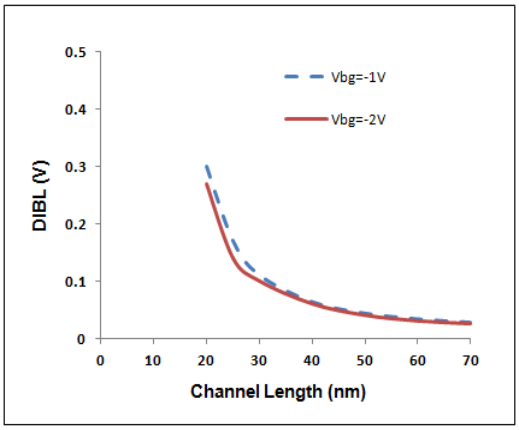

Fig. 8 – Measured DIBL of fully depleted DG MOSFET with length of the channel for different back gate voltages

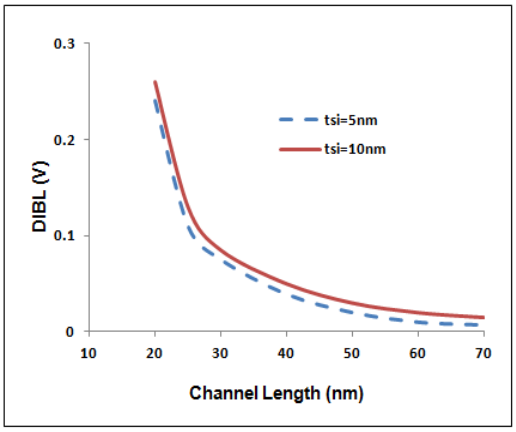

Fig. 9 – Measured DIBL of fully depleted DG MOSFET with length of the channel for silicon film thickness

It is shown from Fig. 9 that DIBL effect is prominent for channel length below 30 nm, less prominent for thinner silicon films due to the better gate control of the channel.

4. CONCLUSION

A 3*D* Double gate fully depleted SOI MOSFET model is discussed, based on solution of Poisson's equations at different gate back gate bias. Here short channel effects and DIBL which causes to shift threshold voltages are considered. Threshold voltage results with variation in channel length and thickness at different bias conditions are presented. Threshold voltage increases with more negative bias, this is because of good control of gate voltage over the channel. As per our investigation threshold voltage shift is more significant for the channel thickness below 5 nm. This model maintains high accuracy and can be applied for wide range of devices with many silicon body thickness and bias conditions. This model accounts the back gate bias, showing their superior effect to reduce short channel effect in double gate SOI MOSFET.

AKNOWLEDGEMENTS

This Research Work is recognized by SRM University, Chennai.

REFERENCES

1. C. Fiegna, H. Iwai, T. Wada, T. Saito, E. Sangiorgi, B. Ricco, *Symp. VLSI Technol. Dig. Tech. Papers*, 33 (1993).
2. Q. Chen, E.M. Harrel, J.D. Meindl, *IEEE Transact. Electron Dev.* **50** No 7, 1631 (2003).
3. X. Liang, Y. Taur, *IEEE Transact. Electron Dev.* **51** No 9, 1385 (2004).
4. M.J. Kumar, A.A. Orouji, *IEEE Trans. Electron Dev.* **52**, 1568 (2005).
5. G. Katti, N. DasGupta, A. DasGupta, *IEEE Transact. Electron Dev.* 51 No 7, 1169 (2004).
6. H.V. Meer, K.D. Meyer, *IEEE Transact. Electron Dev.* **ED-48**, 2292 (2001).
7. R. Rao, G. Katti, D.S. Hvaldar, N. DasGupta, A. DasGupta, *Solid State Electron.* **53**, 256 (2009).
8. Q. Chen, E.M. Harrel, J.D. Meindl, *IEEE Transact. Electron Dev.* **50** No 7, 1631 (2003).
9. F. Balestra, M Benachir, J. Brini, G. Ghibaudo, *IEEE Transact. Electron Dev.* **37**. No 2 (1990).
10. C. Mallikarjun, K.N. Bhat, *IEEE Transact. Electron Dev.* **37** No 9, (1990).
11. D. Esseni, A. Abramo, L. Selmi, E. Sangiorgi, *IEEE Transact. Electron Dev.* **50** No 12, 2445 (2003).