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# A New Electro-Thermal Modeling of Low Voltage Power MOSFET with Junction Temperature Dependent Foster (RC) Thermal Network

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Thermal loading of MOSFET (Metal-Oxide-Semiconductor- Field-Effect-Transistor) model is a very important factor for the reliability of power electronics systems. Thus, the junction temperature must be accurately estimated. This paper presents a new electro-thermal (ET) model for low voltage Power MOSFET rated at (30 V/13 A) by *PSpice* simulator to estimate junction temperature (*Tj*) and power loss. The (ET) model is composed of electrical network model and (RC) thermal network model. The parameters of the (RC) thermal network model are extracted from datasheet using genetic algorithms (GA) method for computation of the transient thermal impedance ($Zth(j-c)$). The propose model reflects superior performance in terms of flexibility and accuracy. The results obtained indicate a good matching between proposed model and manufacturer's data.

**Keywords:** Electro-thermal (ET) model, Junction temperature (*Tj*), Reliability, MOSFET, Genetic Algorithm (GA), PSpice.

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## 1. INTRODUCTION

The development of semiconductor manufacturing technology has resulted in miniaturized power electronic chips with higher voltage and power, this causes large heat dissipation in a reduced size chip, which may affect the device operation. Hence, the junction temperature (*Tj*) of the chip has become a key variable. A fast and accurate transient thermal model based on the junction temperature (*Tj*) dependency upon power losses is crucial to provide proper thermal management of power electronics model. In the literature, the thermal characteristics of power model are characterized using three methods. The Finite Element Method (*FEM*), the thermal resistance-capacitance (RC) networks method and the analytical method [1, 2]. The FEM is a numerical method for simulating the relationship between thermal responses and heat resource (power loss) by a large number of finite elements [3, 4]. The (RC) model characterizes this relationship using a thermal resistance and a thermal capacitance. In the analytical method, a 1*D* or 2*D* heat conduction diffusion equation is solved analytically to find the thermal response of the device. In this method, the heat spreading effect in the material might not be accurately estimated and, usually, a typical heat spreading angle of 45° is assumed [5]. The FEM is more accurate than (RC) model but needs much more time [6]. The (RC) model is widely used due to its simplicity and easy implementation in general circuit simulation software [7]. In this paper, a simple behavioral electro-thermal model for low voltage power MOSFET in the PSpice simulation is provided. The extraction of thermal model parameter values from data sheet using Genetic Algorithm (GA) optimization method for the computation of the transient thermal impedance (*Zth*). In addition, the static and dynamic behavior of the electro-thermal model is simulated and compared with those provided by the manufacturer's datasheet to validate the results obtained by the PSpice model. Finally, to better illustrate the capability and attractiveness of the electro-thermal model in estimating the junction temperature (*Tj*), a dc/dc Boost converter is used as the point of reference.

## 2. ELECTRO-THERMAL MODEL

Generally, an electro-thermal model consists of an electrical model of the device coupled with a thermal resistance-capacitance (RC) network [8]. Fig. 1 shows a diagram of an electro-thermal (ET) simulation of power MOSFET model. In Fig. 1, an thermal model is coupling with a electrical model. The value of the total power loss is injected to the thermal model, in which the thermal characteristics of the model are defined. Then, the junction temperature (*Tj*) is generated by the thermal model, and the temperature dependent device model parameters are determined by this junction temperature (*Tj*).

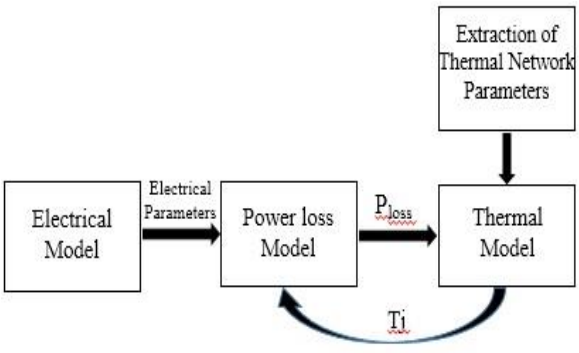


**Fig. 1** – The diagram of the electro-thermal (ET) simulation

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### 2.1 Electrical MOSFET Model

The equivalent circuit of an electrical MOSFET used in this paper is depicted in Fig. 2. It includes a MOSFET level-3, reverse body diode. Beside, $R_G$ is the internal series gate resistance, $R_S$ is the source lead and bond wire resistance, $R_1$ is the epitaxial layer bulk resistance, this resistance is a temperature dependent used to describe the effect of the temperature on the model. $L_S$, $L_G$ and $L_D$ are respectively, the source, gate, and drain bond wire inductances. The MOSFET level-3 is modelled as a voltage controlled current source which can be used to describe the *DC* characterization (static *I-V* output and transfer characteristics) of the device. The drain-source current (IDS) is determined as a function of the drain-source voltage (VDS) and the applied gate-source voltage (VGS) by equations:

$$I_{DS} = 0 \text{ for } V_{GS} < V_{th} \quad (1)$$

$$I_{DS} = \beta\left(V_{GS} - V_{th} - \frac{1+f_b}{2}V_{DS}\right)V_{DS} \text{ for } V_{GS} > V_{th} \quad (2)$$

where

$$\beta = Kp\frac{W_{eff}}{L_{eff}} \quad (3)$$

$$Kp = \mu_{eff}C_{ox} \quad (4)$$

else

$$\mu_{eff} = \mu_s \quad (5)$$

$$\mu_s = \frac{\mu_0}{1+\theta\left(V_{GS} - V_{th}\right)} \quad (6)$$

$$f_b = \frac{\gamma f_s}{4\sqrt{\phi + V_{sb}}} + f_n \quad (7)$$

The key model parameters of MOSFET Level-3 and body diode that could be used for circuit simulations are summarized in Table 1.

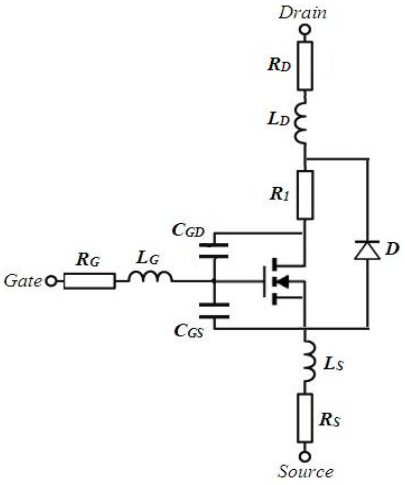


**Fig. 2** – Electrical model

**Table 1** – Model parameters of MOSFET Level-3 and body diode

| **Static characteristic** | |
|---|---|
| Parameter | Value/Unit |
| *VT* | 2.6 V |
| $K_P$ | $8.98.10^{-6}$ A/V² |
| $\theta$ | $6.556.10^{-4}$ |
| $\mu_0$ | 650 cm²/Vs |
| **Body diode model** | |
| Parameter | Value/Unit |
| $I_S$ | 1 µA |
| $Cj_0$ | 1.52 PF |
| *Rs* | 0.1 Ω |
| *TT* | 50 ns |
| *M* | 0.32 |
| *Vj* | 0.38 V |
| **Package** | |
| Parameter | Value/Unit |
| $R_S$ | 600 µΩ |
| $R_D$ | 100 µΩ |
| $R_G$ | 6 Ω |
| $L_S$ | 3 nH |
| $L_D$ | 6 nH |
| $L_G$ | 8 nH |
| **Capacitances** | |
| Parameter | Value/Unit |
| *Coxd* | 5 nF |
| *CGS* | 1.1 nF |

### 2.2 Thermal Impedance Model and Extraction Parameters

The transient thermal behavior of an MOSFET model is characterized by a transient thermal impedance $Zth - jc(t)$ between the junction and case temperature. It can be expressed by the following equations [9, 10]:

$$Z_{th-jc}(t) = \frac{T_j(t) - T_c(t)}{P_d} \quad (8)$$

where $T_j(t)$ is the junction temperature, $T_c(t)$ the case temperature, and Pd is the average dissipated power Fig. 3 shows the transistor power losses flow and the schematic structure of the MOSFET model which consists of four principle materials.

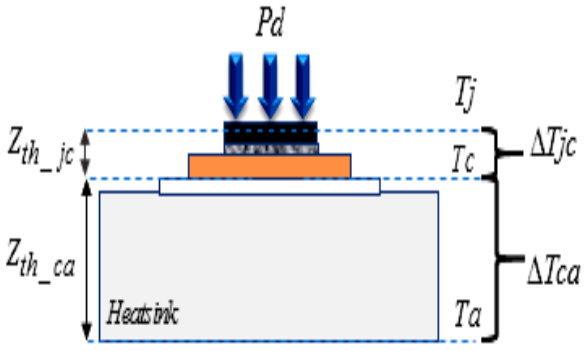


**Fig. 3** – Physically internal structure of the device

In order to describe the thermal transient impedance with the required precision, there are two common types of *RC* network models namely, the Foster and Cauer models [11]. These models provide excellent accuracy over a wide dynamic range, without simulation times or model complexity. A Foster network is constructed using thermal resistance and thermal capacitance parameters from the device datasheet and the parameters do not have physical meanings. In thermal modeling, the Foster (*RC*) network is preferred even though it is purely mathematical. The Foster (*RC*) network can only predict the junction temperature instead of the temperature distribution. In order to improve the Foster thermal networks based models, algorithms are developed for the conversion of Foster networks to an equivalent Cauer type thermal network with the same pair number of (*RC*) lumps [12]. The Cauer network relates better to the real physical thermal system because each node represents a real temperature and can be used to describe the temperature distribution inside the packaging [13-16]. When using the Foster network, the transient thermal impedance curve can be fitted into a series consisting of a finite number of exponential terms as given in (9).

$$Z_{th-jc}(t) = \sum_{i=1}^{n} R_i \left(1 - \exp\left(-\frac{t}{\tau_i}\right)\right) \tag{9}$$

with

$$\tau_i = R_i C_i \tag{10}$$

In the present work, the 4th order thermal equivalent resistance-capacitance (*RC*) Foster model pair parameters are extracted by fitting the step response equation given in (9) to the *Zth* curves. The Genetic Algorithm (GA) optimization method is used for this purpose. To estimate the thermal impedance of the device, first order transfer functions are used. The $R_i$ and $\tau_i$ parameters are determined (9) using Genetic Algorithm (GA) optimization method, in order to estimate the thermal impedance curve provided in the device datasheet according to Fig. 5. It is worth noticing that four parameters are sufficiently enough for a good estimation of the Foster Network. The parameters of the Foster equivalent circuits are extracted. They are listed in Table 2. An excellent correlation can be observed between the *Zthjc* estimated model and the datasheet. The curve clearly shows that the relative error between the model's data and the manufacturer's data does not exceed 5 % which means that the model is accurate.

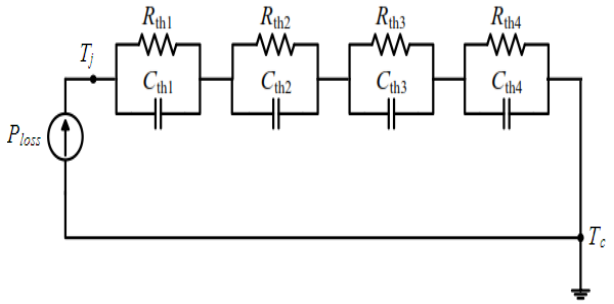


**Fig. 4** – Thermal model

The extracted parameters of the Foster model are listed in Table 2.

**Table 2** – Device Thermal impedance parameters estimation

| No | *Ri*(*C*/*W*) | *τi*(*s*) |
|---|---|---|
| 1 | 0.7612 | 0.0006 |
| 2 | 1.5105 | 0.0140 |
| 3 | 0.7956 | 0.0107 |
| 4 | 0.1326 | 0.0253 |

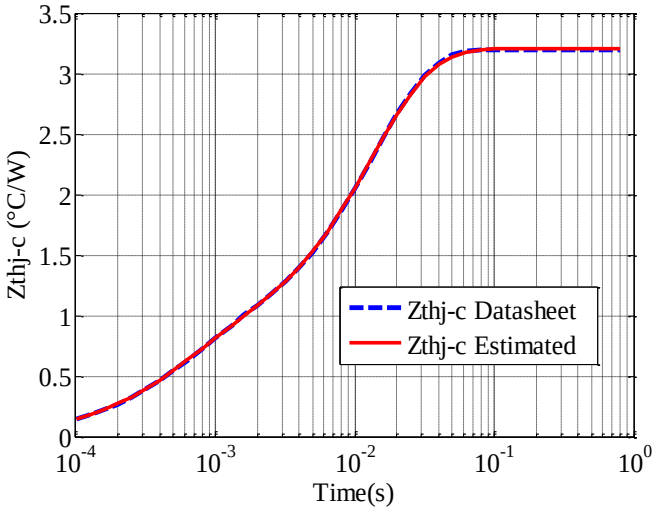


**Fig. 5** – Comparison of the transient thermal impedances from junction to case obtained from the estimated and datasheet model

### 2.3 Validation of the Electrical Model of the ET Compact Models

The validation of the model is carried out by comparing PSpice simulations with the datasheet of the SI MOSFET (SI7390DP) [17].

### 2.4 Static Characteristics Verification

The curves in Fig. 6 and Fig. 7 show respectively the output characteristics *Ids*(*Vds*) and transfer characteristics *Ids*(*Vgs*).

### 2.5 Dynamic Model

The dynamic response of MOSFET device is determined by three junction capacitors, namely, the gate-to-source capacitance (CGS), the drain-to-source capacitance (CDS) and the gate-to-drain Miller capacitance (CGD). As it turns out, the capacitances reported in the datasheet are input capacitance (*Ciss*), the output capacitance (*Coss*) and the reverse transfer capacitance (*Crss*). The needed CGS, CDS, and CDS capacitance values can be deduced from the following equations:

$$C_{GS} = C_{iss} - C_{rss} \tag{11}$$

$$C_{DS} = C_{oss} - C_{rss} \tag{12}$$

$$C_{GD} = C_{rss} \tag{13}$$

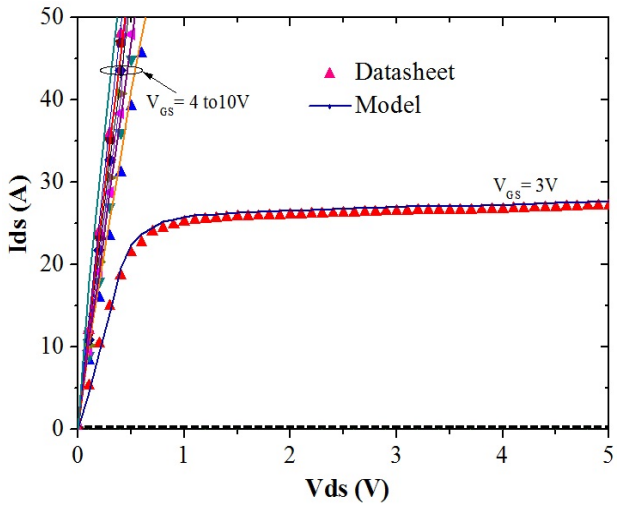


**Fig. 6** – *I-V* output characteristics comparison between the simulation results and datasheet for various *Vgs* values at $T = 25$ °C

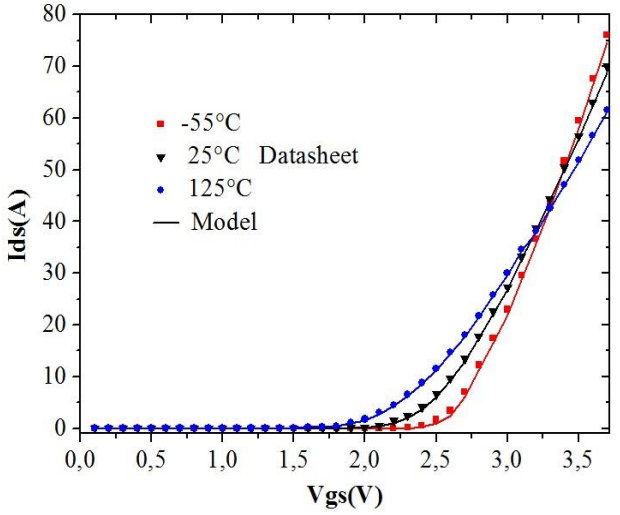


**Fig. 7** – Transfer characteristics comparison between the simulation results and datasheet at different temperatures

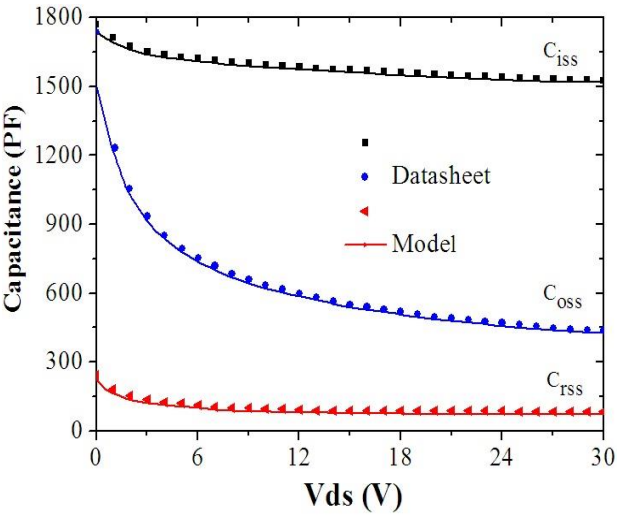


**Fig. 8** – *C-V* curve comparison between the simulation results and datasheet under $f = 1$ MHZ

Fitting *Crss* by tuning zero-bias junction capacitance ($C_{j0}$) and grading coefficient (*M*) parameters of junction capacitance of CGD in fact that it is independent from other capacitance components. To fit *Coss*, the same parameters for CDS can be used taking into consideration the known profile for CGD. At the end, the *C-V* curve tuning process is achieved by fitting *Ciss* and finding the proper value of the linear capacitance CGS.

## 3. ELECTRO-THERMAL MODEL OF A DC/DC BOOST CONVERTER

To provide a realistic for junction temperature evaluation, a DC/DC Boost converter is constructed in the PSpice software environment, using the electro-thermal model, as shown in Fig. 9. The boost converter circuit, used during the simulation, has been designed to operate at the Switching frequency of 10 kHz with 15 V input voltage, 30 V Output voltage, the duty ratio $D = 50$ %, the inductance $L = 500$ µH, the output capacitance $C = 25$ µF, and the electrical resistance $R = 50$ Ohm. The power loss profile and the corresponding junction temperature variations during the first 20 ms of simulation time are shown in Fig. 10.

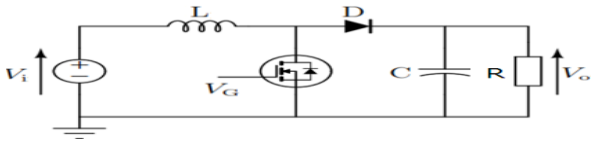


**Fig. 9** – Coupled Electro-thermal model circuit for a DC-DC boost converter

As shown in Fig. 10, the electro-thermal (ET) model is capable of dynamically estimating the junction temperature (*Tj*) during switching cycles.

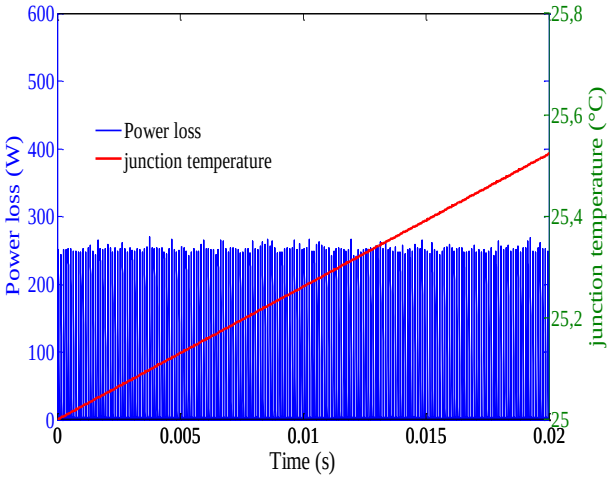


**Fig. 10** – Simulation results of the junction temperature in the electro-thermal model

## 4. COCLUSION

In this paper, a new behavioral electro-thermal (*ET*) model for low voltage power MOSFET which accounts for the thermal effects on the device characteristics has been improved. This model is validated under both static characteristics, dynamic characteristics and compared with data provided by the standard

datasheet. The important advantage of the proposed model is simpler with fewer parameters to be estimated compared with existing models. A MATLAB environment based Genetic Algorithm (GA) optimization method has been used to evaluate the (RC) thermal network parameters. To show the capability of the electro-thermal model in estimating the junction temperature transients, a practical situation is considered where a DC/DC boost converter is considered as a point of reference. Finally, form the simulation results it can be concluded that this model is capable to estimate the junction temperatures (*Tj*) of the device in awide range of operating conditions.

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