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A Graphical Method to Study Electrostatic Potentials of 25 nm Channel Length DG SOI MOSFETs

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To determine electrostatic potentials in silicon channel of undoped DG SOI MOSFET devices, a graphical approach is proposed. The method keeps close to experimental reality by taking into account flat band potential at reduced channel lengths up to 25 nm. This graphical method solves a transcendental equation of Poisson's equation to obtain electrostatic potentials at center and surface of device as a function gate and drain bias voltages.

Keywords: Symmetrical DG SOI MOSFET, Poisson's equation, Electrostatic potential, Numerical method.

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1. INTRODUCTION

In recent years, multi-grid devices have been intensively studied to obtain new MOSFET structures that reduce transistors size while maintaining high performance [1]. Double grille field effect transistors (DGMOSFET) are such promising structures [2]. They make it possible to dimension future MOSFET devices down to few tens of nanometers in size. Symmetrical double grill MOSFETs appear to be attractive alternatives as they can effectively reduce short channels effects and work under higher currents [3].

In this regard, silicon on insulator (SOI) technology has been adopted as the best alternative to previous technologies on a large scale due to its advantages over other technologies [4-5]; therefore, recent studies have focused on studying the electronic properties of DG-SOI-MOSFET in Sub-100 nm scale [6-8].

Zero doping hypotheses in devices have been questioned in recent years due to residual impurities in concentrations that can reach 10^{14} cm^{-3} [9]. Absence of doping atoms in the channel reduces mobility degradation by eliminating the diffusion of impurities. It also avoids undesirable dispersion of features that result from inevitable random microscopic dopant variations in ultra-submicron-sized devices [10].

Existing surface-potential based models rely on numerical iteration to solve their fundamental equations. Several numerical methods have been used previously in the literature. Widely used methods are bisection method [11], Newton-Raphson method [12] and finite difference method [13].

Advantages of plane structure are a better silicon channel thickness uniformity and use of existing manufacturing processes. Disadvantages are difficulty in back gate and under-channel gate dielectric manufacturing and lower gate device wiring is expensive [14].

In this work, we shall use a plane structure and we shall develop a graphic approach used previously by Oana Cobianu and al [15].

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As a first step, Poisson equation and associated boundary conditions lead to a transcendental equation that will allow solving derive the electrostatic potential at center of silicon film. Knowing this electrostatic potential, potentials at surface and volume are easily calculated and channel electrical charge carriers density will be obtained.

To validate developed model which be applied to 25 nm DGSOIMOSFET transistors, electrostatic potentials will be determined for various grid polarizations, oxide thicknesses and silicon film thicknesses.

2. POISSON'S EQUATION SOLUTION

Fig. 1a shows schematic structure of symmetric DG SOI MOSFET, where x is direction along channel thickness and y is direction along channel length. L is channel length, t_{Si} is silicon film thickness and t_{OX} is gate oxide thickness.

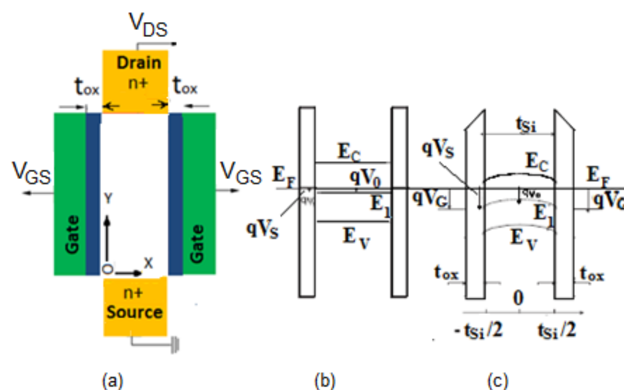

Fig. 1 – Schematic cross-section of DG SOI MOSFET structure (a), and Energy bands diagram (b, c)

Same VGS voltage is applied to both gates that have same flat-band voltage. Since current flows only in y direction, quasi-Fermi level is assumed constant along x direction. Absence of contact with silicon channel means that energy levels are referenced at electrons quasi-Fermi of $n+$ source as shown in Figures 1b, c.

Maxwell-Boltzmann distributions [10] are assumed, and to ignore energy quantization channel is taken un-

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doped and of thickness greater than 5 nm [16].

For mobile electrons through the vertical section perpendicular to silicon film of undoped symmetric DG SOI MOSFET transistor, Poisson equation is written as [11, 17, 18]:

$$\frac{d^2\varphi}{dt^2} = \frac{qn_i}{\varepsilon_{Si}} e^{\frac{\varphi - V}{U_T}} \quad (1)$$

With two following boundary conditions: Maximum potential at center of channel is given by equation (2) and potential at SiO_2/Si interface is given by equation (3).

$$\left.\frac{d\varphi}{dx}\right|_{x=0} = 0 \quad (2)$$

$$V_{GS} - V_{FB} = \varphi\Big|_{x=\frac{t_{Si}}{2}} + \frac{\varepsilon_{Si} t_{ox}}{\varepsilon_{ox}} \cdot \left.\frac{d\varphi}{dx}\right|_{x=\frac{t_{Si}}{2}}. \quad (3)$$

Where φ is electrostatic potential in silicon body, V_{FB} is flat-band voltage, V_{GS} is gate-source voltage, V is channel potential that takes values 0 on source side and V_{DS} on drain side, and n_i is intrinsic concentration of carriers in silicon, ε_{ox} and ε_{si} are dielectric permittivity of oxide and silicon, respectively.

Electric field in silicon is obtained from Poisson's equation first integration as

$$\left.\frac{d\varphi}{dt}\right|_{x=0} = \sqrt{\frac{2KTn_i}{\varepsilon_{Si}} e^{-\frac{qV}{KT}} \left(e^{\frac{q\varphi}{KT}} - e^{\frac{q\varphi_0}{KT}}\right)} \quad (4)$$

Then second integration gives electric potential as

$$\varphi(x) = \varphi_0 - \frac{2KT}{q} \cdot \ln\left[\cos\left(b \cdot e^{\frac{q(\varphi_0 - V)}{2KT}} \cdot x\right)\right] \quad (5)$$

Where $b = \sqrt{\frac{q^2 n_i}{2\varepsilon_{Si} KT}}$

By setting $x = t_{Si}/2$ in equation (5), electrostatic potential at silicon dioxide interface is determined from:

$$\varphi_S = \varphi_0 - \frac{2KT}{q} \cdot \ln\left[\cos\left(b \cdot e^{\frac{q(\varphi_0 - V)}{2KT}} \cdot \frac{t_{Si}}{2}\right)\right] \quad (6)$$

Injecting equation (4) into equation (3), a transcendental equation is obtained with two electrostatic potentials as:

$$V_{GS} - V_{FB} = \varphi_S + \frac{\varepsilon_{Si} t_{ox}}{\varepsilon_{ox}} \sqrt{\frac{2KTn_i}{\varepsilon_{Si}} e^{-\frac{qV}{KT}} \left(e^{\frac{q\varphi_S}{KT}} - e^{\frac{q\varphi_0}{KT}}\right)} \quad (7)$$

Where, φ_S and φ_0 are electrostatic potentials at surface and in body of silicon layer (channel), respectively.

3. GRAPHICAL METHOD

Introducing potential φ_S from equation (6) into equation (7), a new transcendental equation is obtained that relates applied gate-source voltage, drain-source voltage and electrostatic potential in middle of silicon film as:

$$V_{GS} - V_{FB} - \varphi_0 = \beta \cdot e^{\frac{q(\varphi_0 - V)}{2KT}} \cdot |\tan(Z)| - \frac{2KT}{q} \ln\{\cos(Z)\} \quad (8)$$

Where parameters Z and β are given by:

$$\begin{cases} \beta = \frac{t_{ox}\sqrt{2\varepsilon_{Si} KTn_i}}{\varepsilon_{ox}} \\ Z = b \cdot e^{\frac{q(\varphi_0 - V)}{2KT}} \cdot \frac{t_{Si}}{2} \end{cases} \quad (9)$$

Logarithm and cosine functions in transcendental equation lead to an electrostatic potential interval φ_S at center of channel that obey:

$$\left.\begin{matrix} \cos(Z) \rangle 0 \\ \tan(Z) \rangle 0 \end{matrix}\right\} \rightarrow Z \in \left[0 \quad \frac{\pi}{2}\right] \quad (10)$$

And

$$\varphi_0 \in [0 \quad \varphi_{0m}] \quad (11)$$

Where

$$\varphi_{0m} = V + \frac{2KT}{q} \cdot \ln\left(\frac{\pi}{t_{Si} \cdot b}\right) \quad (12)$$

Thus, φ_{0m} changes with V and t_{Si}. For $T = 300$ K and $V = 0$, potential φ_{0m} as a function of silicon layer thickness is shown in Table 1.

Table 1 – φ_{0m} values for different thicknesses t_{si} of silicon layer

t_{si} (nm)	5	10	15	20	25
φ_{0m} (V)	0.5334	0.4975	0.4765	0.4616	0.4500

Since φ_0 is a function of voltages applied across drain and gate, transcendental equation (8) is solved graphically by writing:

$$f = V_{GS} - V_{FB} - \varphi_0 \quad (13)$$

$$g = \beta \cdot e^{\frac{q(\varphi_0 - V)}{2KT}} \cdot |\tan(Z)| - \frac{2KT}{q} \ln\{\cos(Z)\} \quad (14)$$

$$h = f - g \quad (15)$$

φ_0 is obtained when h is equal to zero for a set of V_{GS} and V values as input quantities. For each calculated $\varphi_0$value, electrostatic surface potentials ($x = \pm\, t_{Si}/2$) are calculated from equation (5).

Figure 2 shows f and g functions evolution with φ_0 for $V_{GS} = 0{,}5$ V, $V_{FB} = 0.269$ V, and $V_{DS} = 0$ V.

For a gate-source voltage $V_{GS} = 0.5$ V, a body electrostatic potential of 0.514 V is obtained, in good agreement with Biswajit et al. [16] result.

4. INVERSION CHARGE

Applying Gaussian law at interface and taking into account geometric symmetry, charge inversion is given by:

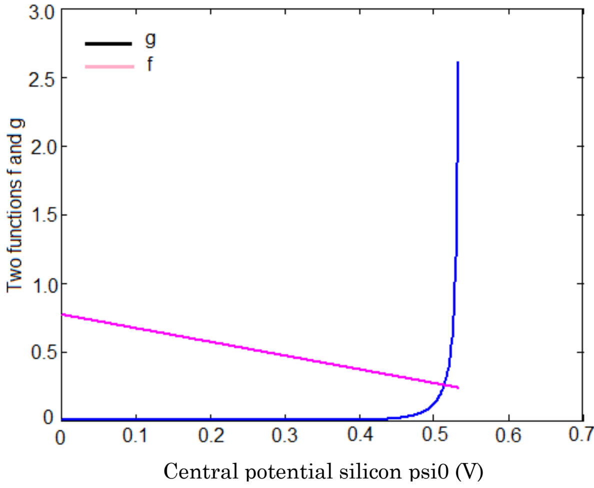

Fig. 2 – Graphical transcendental equation solving

$$Q_{inv} = 2 \cdot \varepsilon_{Si} \cdot \left.\frac{d\varphi}{dx}\right|_{x=\frac{t_{Si}}{2}} \tag{16}$$

Replacing electric field $d\varphi/dx$ by equation (4), charge inversion is:

$$Q_{inv} = \sqrt{8\varepsilon_{Si} n_i KT} \cdot e^{\frac{q(\varphi_0 - V)}{2KT}} \cdot \left| \tan(b.e^{\frac{q(\varphi_0 - V)}{2KT}} \cdot \frac{t_{Si}}{2} \right| \tag{17}$$

5. RESULTS AND DISCUSSION

Using graphical approach and varying gate and drain voltages, electrostatic potentials in middle (body) of silicon layer are obtained. Then, electrostatic potential at surface of silicon film is deduced from equation (6).

Figure 3 shows potentials φ_0 and φ_S for symmetric DG-SOI-MOS transistors with dioxide thickness of 2 nm and silicon thickness t_{Si} taking 10 nm, 20 nm values, respectively. An electric potential created by a point charge in a volume is inversely proportional to distance as:

$$V = \frac{1}{4\pi \cdot \varepsilon_0 \varepsilon_r} \int \frac{\rho}{r} dr$$

Thus, surface potential is independent of silicon layer thickness as shown in Figure 3. Furthermore, electrostatic potential in body decreases as t_{Si} increases. Such results are consistent with those found in literature [15, 16, 19].

Figure 4 show electrostatics potentials φ_0 and φ_S as a function of gate bias for 2 nm and 3 nm oxide thicknesses.

Both figures show that electrostatic potentials increase as oxide thickness decreases. Figures also show that oxide thickness has little influence on surface potential φ_S, but acts strongly on body potential φ_0.

As gate voltage increases towards threshold, electronic density becomes greater and greater. For higher gate voltages than threshold, φ_S continues to increase while φ_0 deviates rapidly from φ_S to a maximum value φ_{0max} corresponding to saturation [21].

Figure 4 shows electrostatic potentials φ_0 and φ_S in silicon channel of MOSFET transistors as a function of drain voltage V_{DS} for 0.5 V, 0.8 V and 0.9 V gate voltages, with t_{Si} = 10 nm and tox = 2 nm. Notice that inversion corresponding to $\varphi_0 = \varphi_S$ occurs for $V_{GS} > 0.4$ V. Potentials φ_S and φ_0 are directly proportional to gate voltage V_{GS} up to $V_{GS} \approx 0.3$ V. Beyond, saturation happens [20].

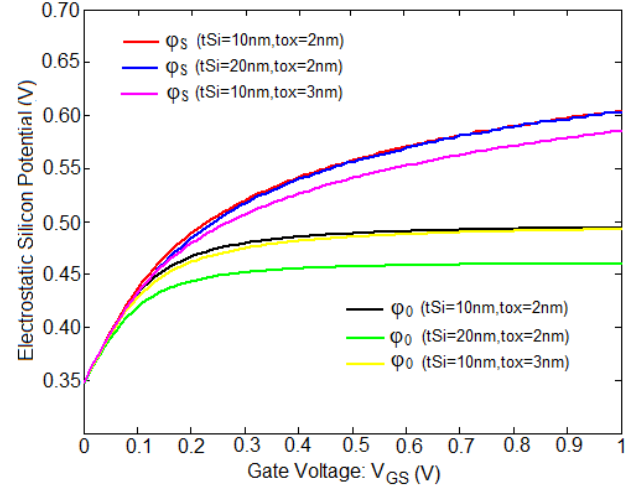

Fig. 3 – Evolution of electrostatic potentials φ_S and φ_0 with gate voltage for several silicon thickness and gate oxide thicknesses values

Figure 5 shows charge inversion versus gate bias V_{GS} for four V_{DS} drain voltages, with t_{Si} = 10 nm and t_{ox} = 2 nm.

Figure 6 show the dependence of induced mobile charge carriers (electrons) in channel, as a function of gate-source voltage V_{GS} and drain-source voltage V_{DS}, for several oxide and silicon thicknesses. Notice that φ_S depend strongly on t_{ox}. It increases when tox increases.

The different graphical results shows that for device surface potential depends little on channel thickness, whereas it strongly depends on oxide thickness. From the results of our analytical study of DG-SOI-MOSFT good agreement was found with results in the literature [9-21].

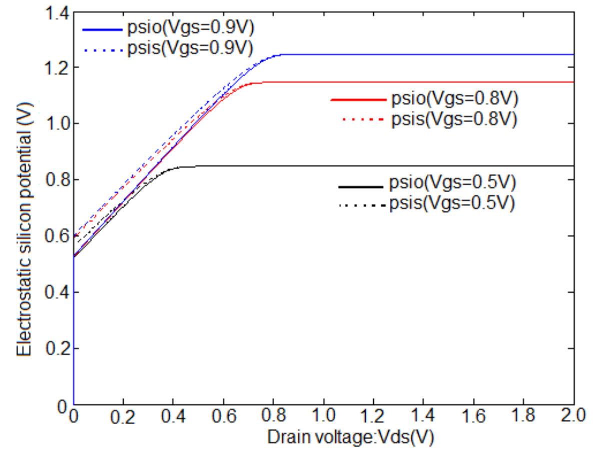

Fig. 4 – Silicon electrostatic potential for t_{Si} = 10 nm and several gate voltages

6. CONCLUSION

A numerical graphical solution of Poisson equation for un-doped symmetric DG-SOI-MOSFETs has been developed in with a Sub-100 nm channel length of 25 nm and an undisturbed flat-band voltage ($V_{FB} \neq 0$).

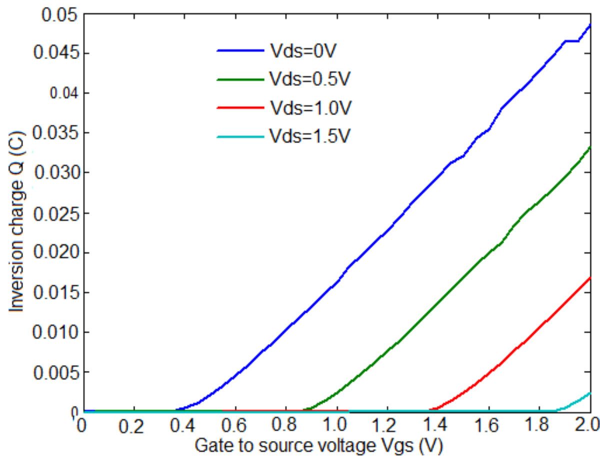

Fig. 5 – Inversion charge (Qin) versus gate voltage (V_{GS}) for several applied drain voltage (V_{DS})

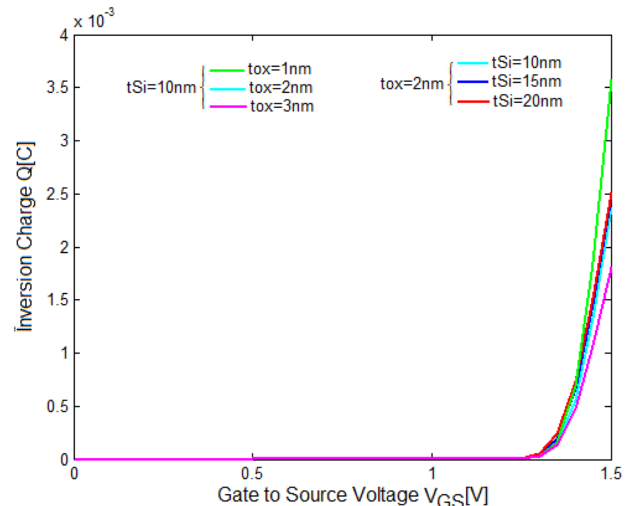

Fig. 6 – Inversion charge (Qin) versus gate voltage (V_{GS}) for several silicon film and gate oxide thicknesses at V_{DS} = 1.5 V

We have shown that the electrostatic potentials are the depend on the basic dimensions (channel thickness and oxide thickness) of this technology, this allows to calculate drain current, trans-conductance, output conductance, transfer characteristics and output characteristics as a function of drain voltage and gate voltage. The compatibility between our results and what is stated in the literature also shows the efficient and physically meaningful of this method of study the DG-SOI-MOSFETs structures.

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