# Charge Based Quantization Model for Triple-Gate FINFETS

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In this article we have developed an analytical model for Tri gate Metal oxide semiconductor field effect transistor (MOSFET) by including quantum effects. The coupled Schrödinger and Poisson's equation is solved using variational approach to develop an analytical quantum model. An analytical model for charge centroid is obtained and then inversion charge model is developed with quantum effects by means of oxide capacitance for different channel thickness and gate oxide thickness. The compact model is shown to reproduce transfer characteristics, transconductance and C-V curve of tri gate MOSFET using the model. The modeled results are then compared to the simulated results. The comparison shows the accuracy of the proposed model.

**Keywords:** Analytical Model, Tri-Gate MOSFET, Poisson's equation, Drain current model, Transconductance, C-V curve.

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## 1 INTRODUCTION

As the dimensions of the conventional MOSFETs are being scaled towards Nano scale dimensions, due to short channel effects it is been difficult to improve performance of the device. Therefore Multigate MOSFET structures like double gate (DG), tri gate (TG) and gate all around (GAA). [1-3] The double gate MOSFET is one of the most promising structures for complementary metal oxide semiconductor (CMOS) scaling to nanometer size due to its ability to suppress short channel effects such as drain induced barrier lowering, sub threshold slope , threshold voltage roll off. Thus an analytical model is required to design future integrated circuits.

In order to obtain devices with upgraded performance like improved device speed, device miniaturization, improved power efficiency, devices have been subjected to aggressive down scaling which results in severe Short channel effects (SCEs) which degrade the device performance. To overcome several SCEs, different silicon MOS structures like Silicon-on insulator have been developed which is high immune to SCEs and various multi gate structures are introduced. Introduction of double gate in MOSFET has added an advantage by allowing higher electrostatic control over the channel on 2D planner MOSFET.[4-6] By introduction of a tri-gate allows better electrostatic control over the channel by the gate and improves conductivity with increase in surface area by increasing the speed and performance thus by reducing the power consumption in the device. Tri gate transistors on Silicon on insulator (SOI) substrate combine good sub threshold characteristics with high on current. [7]

## 2 QUANTUM MODEL

The below Fig. 1 shows cross sectional view of tri gate SOI MOSFET, $H$ is the Si film thickness or channel thickness, tox is the $SiO_2$ dielectric thickness or oxide thickness and $W$ is the width of the channel, $L$ is the channel length which is also called as gate length; the surface potential is defined as the Fermi potential at the point $(x, y)$ along the channel to its source end. It is assumed to be the flow of current is only in the $y$ direction and quasi Fermi level remains constant over the channel in $x$ direction [8]. In case of tri gate MOSFET the quantum confinement arises by the surface potential, quantum effect arises due to confinement of moving electrons in the thin Si film.

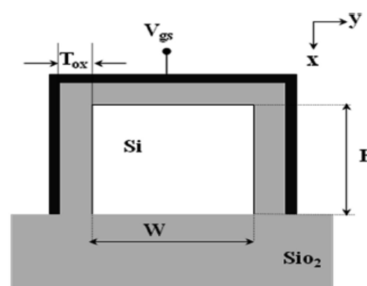


**Fig.1** – Cross sectional view of tri gate MOSFET

The quantum confinement which is usually observed when the particle size is very small compared to the wavelength of the electron. Confinement refers to the motion of electrons moving randomly restricted in specific energy levels in the quantum wells. The inversion charge carriers are confined into the well and are depending on the body thickness. More than 90 % of the electrons are confined in the ground state of lower sub band for lower *Si* thickness. So, by considering lower sub band and all the higher sub bands are neglected Relationship between wave function and electron density are studied by solving the coupled system of Schrodinger and Poisson's equation [9]. The electrostatic potential is determined by the nonlinear Poisson equation is given by

$$\frac{d^2\varphi(x)}{dx^2} = \frac{q}{\varepsilon_{Si}}\left(N_A + N_{inv}\left|\psi_i(x)\right|^2\right). \tag{1}$$

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Due to the confinement of electron motion which is normal to the Dielectric/Semiconductor interface, over the channel of the transistor conduction band is split into several specific sub-bands. The Eigen function $\psi_i(x)$ is calculated for the lower energy sub band. Using surface potential $\phi(x)$ the Schrodinger equation is solved for lower energy sub band $E_i$ using Variational approach.
The Schrodinger equation is written as

$$\frac{-h^2}{8\pi^2 m_x}\frac{d^2\psi(x)}{dx^2}+\left(-q\varphi(x)\psi_i(x)\right)=E_i\Psi_i(x), \qquad (2)$$

where $\phi(x)$ is the electric potential, $\psi_i(x)$ is the Eigen function, $h$ is the Plank's constant, $E_i$ is the lower sub-band energy and $m_x$ is the effective mass of electrons in the x-direction. For silicon channel, $m_x$ can be written as 0.916 $m_0$.

The Eigen wave function can be written as,

$$\Psi_i(x)=a_0\sqrt{\frac{2}{t_{Si}}}\sin\left(\frac{\pi x}{t_{Si}}\right)\left[e^{\frac{-b_0 x}{t_{Si}}}+e^{\frac{-b_0(t_{Si}-x)}{t_{Si}}}\right]. \qquad (3)$$

### 2.1 Inversion Charge

In this section we are modeling an Inversion charge centroid model and inversion charge by considering Quantum effects [10]. The inversion layer centroid can be calculated integrating the square of $\psi_i(x)$ over $x=0$ to $x=t_{Si}/2$.

$$x_i=-4a_0^2e^{-2b_0}\pi H^2W^2\left(4b_0^2+\pi^2+\pi^2\cosh(b_0)\right)+x_1, \qquad (4)$$

where, $a_0$ is the normalization constant and $b_0$ is the variational parameter and is given below.

$$x_1=\left(\frac{[b_0(b_0^2+\pi^2)\cosh(b_0)-(b_0^2(3+b_0)+(1+b_0)\pi^2\sinh(b_0))]}{b_0^2HW(b_0^2+\pi^2)^2(4b_0^2+\pi^2)}\right),$$

$$a_0=\sqrt{\frac{b_0HW\left(4b_0^4+5b_0^2\pi^2+\pi^4\right)}{8\pi HW\sinh(b_0)[\cosh(2b_0)-\sinh(2b_0)](4b_0^2+\pi^2+\pi^2\cosh(b_0))}}, b_0=(W+H)\pi^2\left(\frac{5}{12}\frac{q^2\left(m_x+m_y\right)Q_{inv}}{\varepsilon_{Si}h^2}\right),$$

$$Q(V)=3C_{ox}\left\{\left(\frac{-2C_{ox}{v_t}^2}{Q_0}\right)+\sqrt{\left(\frac{2C_{ox}{v_t}^2}{Q_0}\right)^2+4{v_t}^2\ln^2\left[1+\exp\left(\frac{V_{gs}-V_{th}+\Delta V_{th}-V}{2v_t}\right)\right]}\right\}, \qquad (5)$$

$$I_d=\mu\frac{W}{L}\left[-2C_{ox}A+\frac{2C_{ox}(1+e_{vx})}{e_{vx}}\left(\frac{U}{2}\sqrt{A^2+U^2}+\frac{A^2}{2}\ln\left(U+\sqrt{A^2+U^2}\right)\right)\right]. \qquad (7)$$

Inversion Charge is calculated by direct calculation without using iterative algorithms [10]. We have used the following expression to calculate the inversion charge represented by $Q(V)$ *in* equation (5), where,

$$Q_0=4\left(\frac{kT}{q}\right)C_{Si}, \qquad V_0=\Delta\phi-v_t\ln\left(\frac{qt_{Si}n_i}{2Q_0}\right),$$

$$V_{th}=V_0+2v_t\ln\left(1+\frac{Q_{inv}}{2Q_0}\right), \Delta V_{th}=\frac{\left(\frac{2C_{ox}{v_t}^2}{Q_0}\right)Q_{inv}}{\frac{Q_{inv}}{2}+Q_0}.$$

and $v_t = kT/q$ *(0.0259)* at room temperature, q is charge of electron $1.602\times10^{-19}$ C, $T = 300$ K, $k$ is Boltzmann constant. $Q_{inv} = qN_{inv}$.

$$C_{ox}=\frac{\left(\varepsilon_{ox}/t_{ox}\right)}{1+\left((x_i/t_{Si})(\varepsilon_{ox}/t_{ox})\right)},$$

where $C_{ox}$ the term that introduces the centroid derivative which has been included to represent the device capacitance by equating it in (equation 5) with the account of Quantum Effect.

### 2.2 Drain Current

In this section a continuous analytical drain current expression with respect to the previously modeled inversion charge model for the DG MOSFET is obtained which is given by the equation as follows,

$$I_d=\mu\frac{W}{L}\int_0^{V_{ds}}Q(V)dV \qquad (6)$$

and the expression is given in equation (7), where

$$A=\frac{2C_{ox}v_t^2}{Q_0}, e_{vx}=e^{\frac{V_{gs}-V_{th}+\Delta V_{th}-V}{2v_t}}, U=2v_t\ln\left(1+e_{vx}\right).$$

### 2.3 Transconductance

The variational parameter of Drain current called transconductance, which quantifies the Drain current variation with respect to the gate source voltage variation keeping drain to source voltage as constant and is given by

$$G_m=\frac{dI_d}{dV_{gs}}. \qquad (8)$$

### 2.4 C-V Curve

Where $Q(V)$ is obtained from the previous section

2.1 modeled by considering quantum effects [11]. C-V analysis is useful for obtaining information about MOS gate stacks such as parameters like oxide thickness, doping density of the substrate, flat band voltage and gate work function.

$$C_v = \frac{dQ(V)}{dV_{gs}}. \quad (9)$$

## 3 RESULTS AND DISCUSSION

Silvaco ATLAS provides general capabilities for physically based 2 dimensional simulations of semiconductor devices including DC and AC small signal analysis, Energy band models, band to band tunneling models etc., and electrical characterization of the semiconductor devices. In this section our obtained results using MATLAB are compared with 2-D numerical simulation which is obtained by Silvaco ATLAS software.

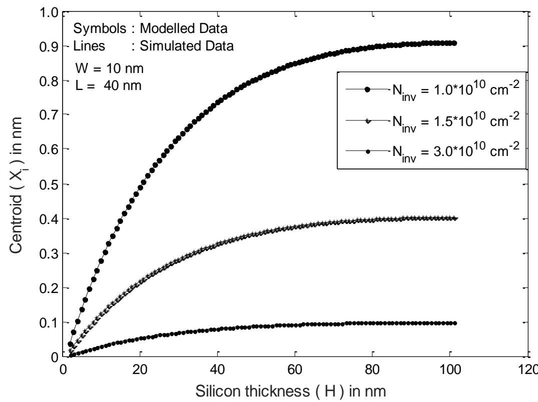


**Fig.2** – Inversion charge Centroid as a function Silicon thickness for different inversion charge density ($N_{inv}$). $W$ = 10 nm, $H$ = 10 nm

Fig. 2. shows the plot of inversion charge centroid ($x_i$) along the silicon channel thickness ($H$) in variation with inversion charge density ($N_{inv}$) represented by the equation 4. For the smaller thickness of the channel the charge centroid depth increases linearly with respect to the silicon thickness in accordance with the $N_{inv}$. For larger thickness due to the high electric field at the channel oxide interface with the effect of quantum effects charge centroid decreases with the increase in the $N_{inv}$.

Fig. 3. represents the plot of inversion charge with the input gate voltage for the different values of device dimensions represented by the analytical expression in equation 5. From the plot we can conclude that the inversion charge increases linearly above the threshold voltage for all the device dimensions, for the smaller device dimensions $H = 5$ *nm* and $t_{ox} = 1$ *nm* yields an increased inversion charge value.

Fig. 4. to Fig. 7. show the transfer characteristics ($I_d$-$V_{gs}$) of the tri gate device in variation with all the device parameters, these plots are represented by the analytical expression ($I_d$) represented by equation 7.

Fig. 4. shows the behavior of drain current with different drain to source voltage ($V_{ds}$) for $V_{ds}$ = 0.1 V, 0.3 V & 0.5 V respectively. It is observed that the threshold

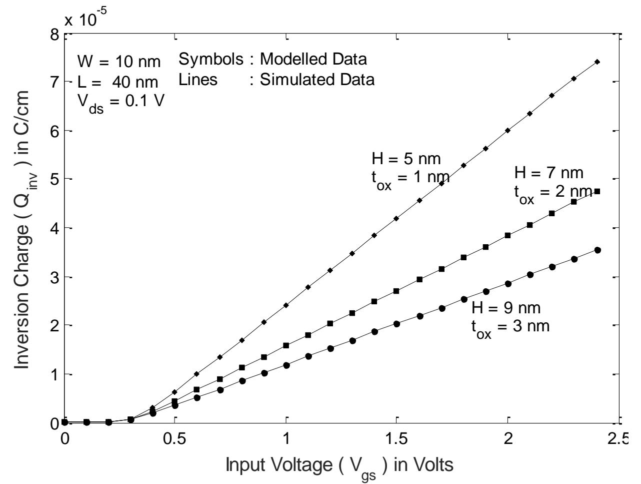


**Fig.3** – Inversion charge as a function of Gate voltage for different device dimensions. $W$ = 10 nm $L$ = 40 nm, $V_{ds}$ = 0.1 V

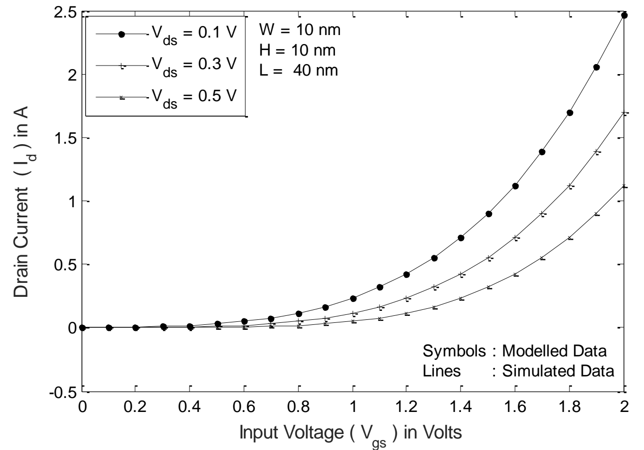


**Fig.4** – Drain current as a function of gate voltage variation in drain to source voltage. $W$ = 10 nm, $L$ = 40 nm, $H$ = 10 nm

voltage and drain current is totally dependent on $V_{ds}$. For lower $V_{ds}$ (0.1 V) we get a higher drain current (2.4 A) with less threshold voltage $V_{th}$ = 0.3 V. thus due to the smaller threshold voltage & larger current of the device, there will be increase in the performance and reduction in the power consumption of the device.

Fig. 5. shows the $I_d$-$V_{gs}$ curve for the channel lengths $L$ = 20 nm, 30 nm & 50 nm respectively. Thus it shows for the channel length of 20 nm gives a better output current.

Fig.6. shows the $I_d$-$V_{gs}$ curve for the different channel width and channel thickness, $W = H$ = 5 nm, 7 nm & 10 nm respectively and shows a higher output current for the device dimensions $W = H$ = 10 nm. Fig. 7. shows the $I_d$-$V_{gs}$ curve for the temperatures 300 K, 400 K & 500 K respectively; it is observed that for room temperature MOS devices will operate with better performance than for higher temperatures.

Fig. 8. shows the plot of transconductance over input gate voltage represented by the equation 8, it shows a change in the input voltage form 0.2 V to 0.4 V there is a larger change in the output current. Thus

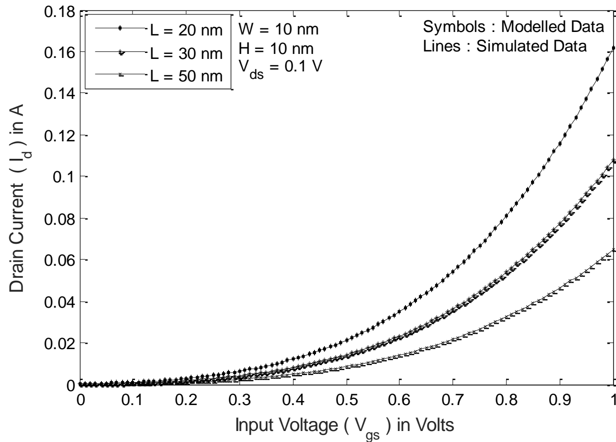


**Fig.5** – Drain current as a function of gate voltage variation in channel length. $W$ = 10 nm, $H$ = 10 nm, $V_{ds}$ = 0.1 V

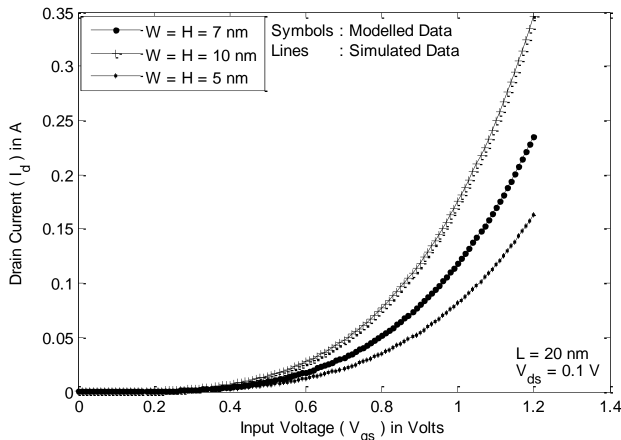


**Fig.6** – Drain current as a function of gate voltage variation in channel width & Height. $L$ = 40 nm, $V_{ds} = 0.1$ *V*

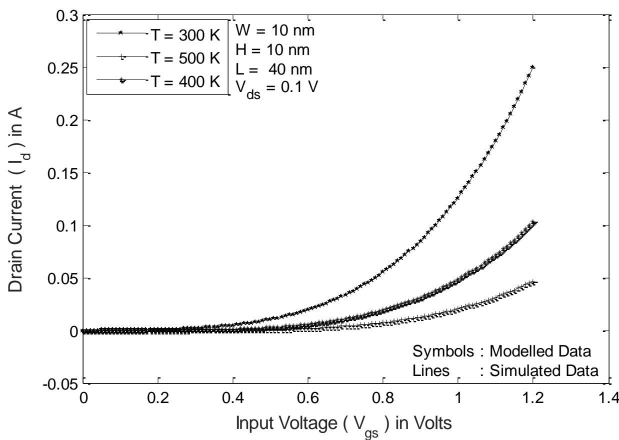


**Fig.7** – Drain current as a function of gate voltage variation in Temperature. $W$ = 10 nm, $H$ = 10 nm, $L$ = 40 nm, $V_{ds}$ = 0.1 V

shows a better sensitivity of the device. Fig. 9. shows the plot of gate capacitance along the input gate voltage for the device dimensions $W$ = 10 nm, $H$ = 10 nm and $L$ = 20 nm obtained by the equation 9.

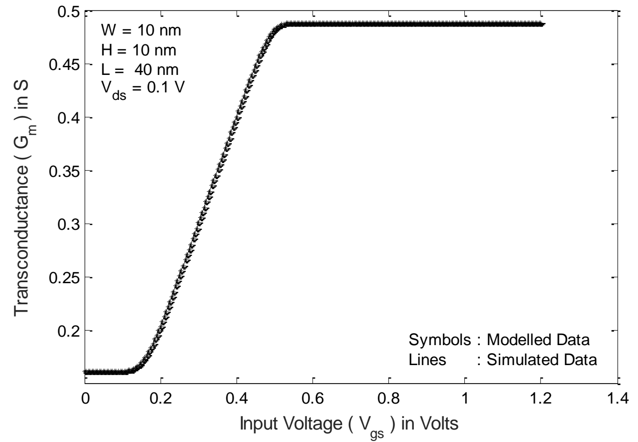


**Fig.8** – Transconductance versus gate voltage of trigate Fin-FET structure

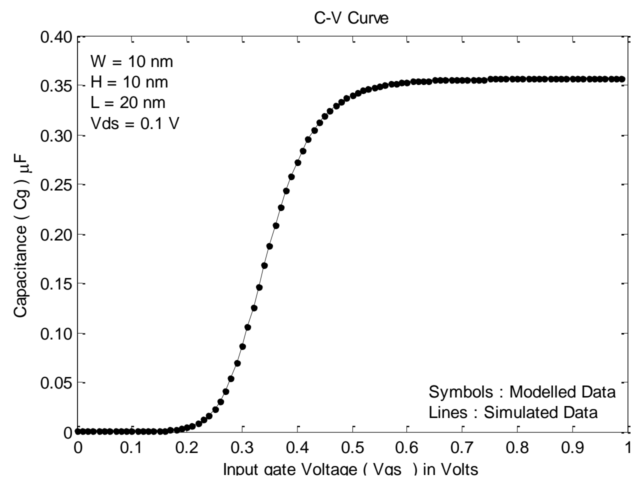


**Fig.9** – Gate capacitance versus gate voltage of trigate Fin-FET structure

## 4 CONCLUSION

An analytical model for tri gate MOSFET of Si film thickness has been developed by Quantization. Due to the quantum effect, the channel charge carrier density is lower than the classical one. We have characterized and modeled the inversion charge and its spatial distributions of tri gate MOSFET, including quantum effects. The model is based on the quantum mechanical variational approach, accounts for the Si film thickness which is depending on electric potential solved by couple Poisson and Schrödinger equation. A design criterion is defined for achieving beneficial strong volume-inversion operation. The comparison of I-V characteristics, transconductance, centroid and C-V curves are generated by compact model with quantum effects. The model predictions are an excellent approximation for all regions of device operation. Therefore, the model of this study provides a helpful method to review Quantum effects on *TG-MOSFETs*.

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