JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. **11** No 4, 04014(6pp) (2019)

ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том **11** № 4, 04014(6cc) (2019)

Investigation of Localized Charges on Linearity and Distortion Performance of Ferroelectric Dual Material Gate All Around TFETs

Varun Mishra*, Yogesh Kumar Verma†, Santosh Kumar Gupta#

Electronics and Communication Engineering Department, Motilal Nehru National Institute of Technology, Allahabad, India

(Received 28 March 2019; revised manuscript received 02 August 2019; published online 22 August 2019)

Scaling down the MOSFETs below 20 nm implies several complications such as high OFF-state current due to thinning of gate oxide, drain induced barrier lowering, and other short channel effects (SCEs). In this aspect, tunnel-field-effect transistor (TFET) has emanated as the suitable contender to outshine the MOSFETs in nanoscale regime. Negative capacitance property of ferroelectric material is combined with the band-to-band tunneling mechanism of tunnel FET in order to enhance ON-state current of the device. Silicon doped hafnium oxide (Si:HfO_2) is used as a ferroelectric layer (gate insulator). Lower permittivity and compatibility with the fabrication process flow of Si:HfO_2, makes it a suitable ferroelectric material in contrary with perovskite materials. This work examines the impact of localized charges on electrical performance, linearity, and distortion parameters of ferroelectric-dual material-gate all around-tunnel field effect transistor (FE-DMGAA-TFET). The presence of oxide charges modifies the bias point of the device; therefore, its effect needs to be investigated in terms of figures of merit (FOM) of linearity and distortion. Localized oxide charge may be positive or negative depending on the trap energy level with respect to Fermi level. It is observed that OFF-state current deteriorates considerably for donor-localized charge from an order of 10^{-19} to 10^{-12} A. The non-linearity and distortion of the device decrease in the presence of negative localized charge. It has been analyzed through numerical calculations that due to donor-localized charges the subthreshold regime deteriorates significantly highlighting the requirement of an intensive analysis in this region for future niche market of electronics. However, the effect of acceptor-localized charges is marginal on the performance of the device, thus offering great potential to maintain its reliability.

Keywords: Ferroelectric, Localized charges, Negative capacitance, Third order intermodulation distortion, Zero crossover point.

DOI: 10.21272/jnep.11(4).04014 PACS numbers: 85.30.Mn, 73.43.Jn, 85.50. – n

1. INTRODUCTION

Scaling of the MOSFETs below 20 nm involves several problems related to fabrication, leakage current dominating the off-state power, drain-induced barrier lowering (DIBL), subthreshold swing (SS) and various distinct short channel effects (SCE) [1, 2]. The distinguished properties of tunnel-field-effect transistor (TFET) make it a promising contender to outperform the conventional MOSFETs [3-5] in nanoscale regime. TFETs use interband tunneling at source-channel junction and the large tunneling path at a lower gate voltage prevents the tunneling of electrons, thus provides low leakage current. However, TFETs exhibit low drive current, high ambipolar current and threshold voltage [6]. In order to overcome these characteristics, gate all around (GAA) structure was proposed [7] which has an enhanced control over the channel. However, the problem of low drive current and delayed saturation still exists in GAA structure. To mitigate such problems, the incorporation of ferroelectric (FE) material as gate insulator was suggested by M.H. Lee *et al.* [8] to increase the drive current because of its negative capacitance (NC) providing a positive feedback at gate terminal which enhances the band bending at source-channel junction thereby shortening the tunneling path and increasing the drive current. NC-FET is one of the contenders of TFETs that can provide the SS below 60 mV/dec. Generally, SS is expressed as

$$SS = \left(\frac{\partial \psi_S}{\partial \log_{10} I_D}\right) \cdot \left(1 + \frac{C_S}{C_{ins}}\right), \qquad (1.1)$$

where ψ_S denotes the surface potential; I_D stands for drain current; C_S and C_{ins} are the capacitances of semiconductor and insulator respectively. The fundamental concept of NC is that the term C_S/C_{ins} becomes negative which reduces the body factor below one [9]; thus, the amplified surface potential created by an internal positive feedback on the gate voltage leads to increase in band bending and tunneling of electrons at the source-channel junction. This process enhances the drive current and reduces the SS. Chunsheng Jiang *et al.* investigated the NC in GAA-TFET by using perovskite FE materials [10], the main difficulty in using these materials is their incompatibility with the CMOS process and scaling. U. Schroeder *et al.* [11] reported the discovery of ferroelectric properties in silicon doped hafnium oxide (Si:HfO_2). The main interest in utilizing Si:HfO_2 is its full compatibility with the CMOS process and enhanced scaling. The lower permittivity of Si:HfO_2 contrasts with other FE materials such as Lead Zirconium Titanate (PZT) and Strontium Bismuth Tantalate (SBT), permits to utilize thinner films which reduces the fringing field effects.

The exponential rise in the communication technol-

* rel1605@mnnit.ac.in
† rel1607@mnnit.ac.in
# skg@mnnit.ac.in

ogy has attracted a huge number of customers in the field of radio frequency (RF) electronics. Hence, it has increased the market for RF semiconductor devices acquiring better RF characteristics. Until now, the focus was mainly on the device performance such as cut-off frequency, transconductance but to uncover the figures of merit (FOM) of linearity and distortion, the impact of localized charges must be investigated. Linearity in a device is demonstrated by the absence of higher order harmonics. The presence of localized charges in a device varies the biasing point; hence, the alteration in the linearity parameter with regard to localized charges is significant. The reliability of TFET is a matter of interest for short channel devices, because of the high electrostatic field at the tunneling junction. This electrostatic field leads to the origination of defects at the semiconductor-oxide interface [12]. Besides the strong electrostatic field, the fabrication methodology may create the defects at the interface of Si-SiO_2. These charges can severely degrade the reliability and vary the defined device behavior [13]. There are several formerly published reports related to linearity and distortion performance of TFETs [14]. However, to date, very little has been accounted for the investigation of the influence of localized charges on the linearity and distortion performance of FE-DMGAA-TFET. This work investigates the impact of localized charges on linearity and distortion parameters of FE-DMGAA-TFET.

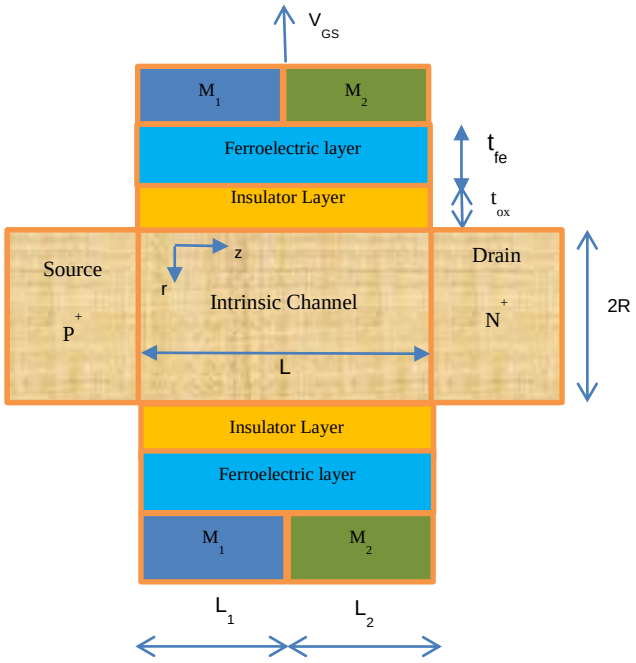


Fig. 1 – Schematic view of a cross-section of FE-DMGAA TFET

2. DEVICE DESCRIPTION

The cross-sectional view of FE-DMGAA-TFET with a ferroelectric layer of Si:HfO_2 as gate insulator and SiO_2 as an interface layer is shown in Fig. 1. The main objective of utilizing SiO_2 layer is to restrain inter-diffusion between the ferroelectric layer and semiconductor. The gate encompassing the channel is divided into two parts: (i) Tunnelling gate (M1) and (ii) Auxiliary gate (M2). The silicon channel is doped with trivalent impurity having a concentration of 10^{15} cm^{-3}. Source and drain regions are doped with Group-III and V impurities having a concentration of 10^{20} cm^{-3} and 10^{18} cm^{-3} respectively. The ambipolar effect is minimized by doping source and drain asymmetrically. The thickness of the interface layer and ferroelectric layer is 1 nm and 5 nm respectively. The diameter of silicon channel is 20 nm and channel length is 50 nm, which is divided into tunneling gate and auxiliary gate length of 25 nm each. The commercially available 3D Silvaco ATLAS TCAD tool [15] is used in numerical calculations.

The models used during numerical calculation are Field dependent mobility model, Concentration-dependent mobility model, Shockley-Read-Hall recombination model, Band gap narrowing model, Auger recombination model, and Kane's band to band tunneling model. Ferro model is enabled in our numerical calculation to include the ferroelectric effects. The ferroelectric permittivity used in Poisson's equation [15] is expressed as:

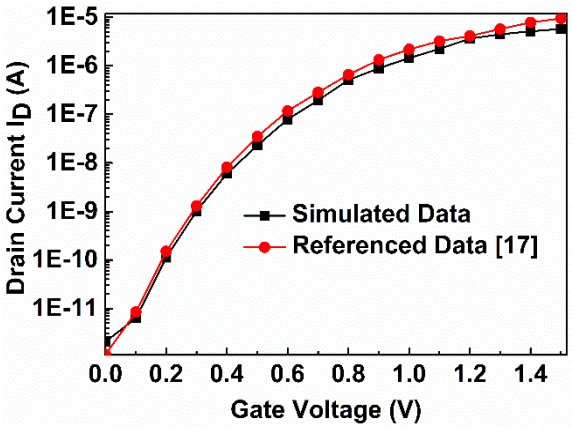
$$\varepsilon(E) = ferro.epsf + \frac{ferro.ps}{2\delta} \times sech^2\left[\frac{E - ferro.ec}{2\delta}\right], \quad (2.1)$$

where *ferro.epsf* is the permittivity, *ferro.ps* is the saturation polarization, *ferro.ec* is the coercive field, E is the electric field and δ is given by:

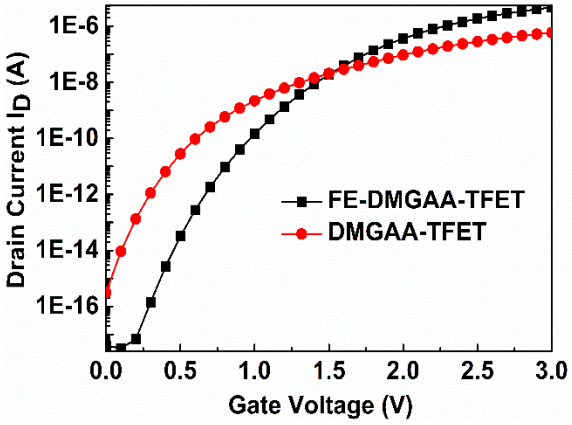
$$\delta = ferro.ec\left[log\left(\frac{1 + \frac{ferro.pr}{ferro.ps}}{1 - \frac{ferro.pr}{ferro.ps}}\right)\right], \quad (2.2)$$

where *ferro.pr* is the remnant polarization. The values of *ferro.ec*, *ferro.pr*, *ferro.ps*, and *ferro.epsf* are taken as 1.15 MV/cm, 10.75 μC/cm^2, 11.37 μC/cm^2, and 33.75 [16]. According to the previously published results, for analyzing the minimum change the value of localized interface charge density (N_f) is chosen as $N_f = \pm 10^{12}$ cm^{-2}.

The simulation models used for the analysis are calibrated against the previously published result [17]. In order to calibrate the Kane's BTBT model, its tunneling masses are tuned from their initial values to a regulated value, i.e. me.tunnel = $0.272m_0$ and mh.tunnel = $0.54m_0$, where m_0 is the electron rest mass. For model validation, all the dimensions and doping parameters are kept identical to that of [17]. Fig. 2a shows the verification of simulation framework with the referenced data [17]. Fig. 2b depicts the enhanced drive current of FE-DMGAA-TFET in contrast to DMGAA-TFET because of negative capacitance; the voltage amplification leads to increase in band bending of conduction and valence bands, which enhances the tunneling rate at source-channel junction. Both TFETs have identical device dimensions and physical oxide thickness for comparison. Low leakage current is observed for FE-DMGAA-TFET because of high band gap of ferroelectric HfO_2.



a



b

Fig. 2 – (a) Comparison of simulated and referenced data [17]; (b) transfer characteristics of FE-DMGAA-TFET and DMGAA-TFET at $V_{DS} = 1$ V

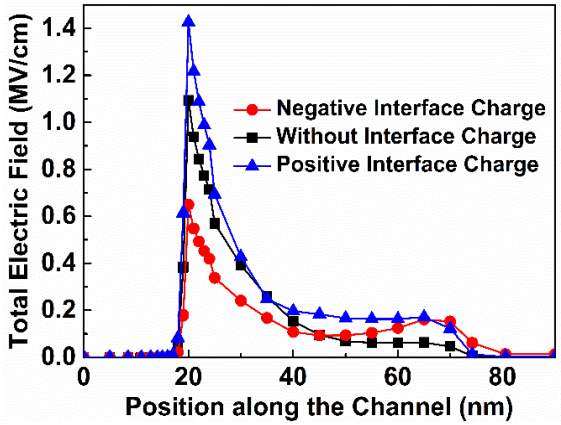
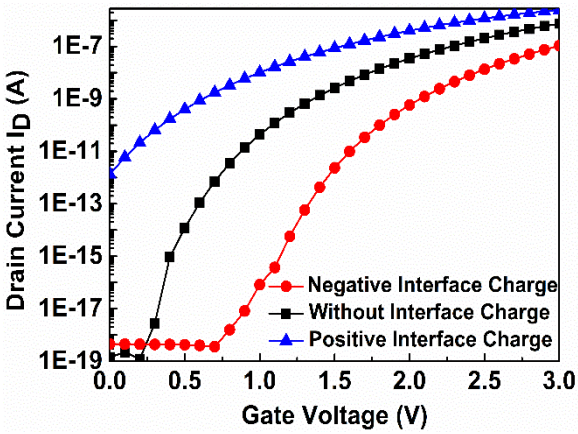


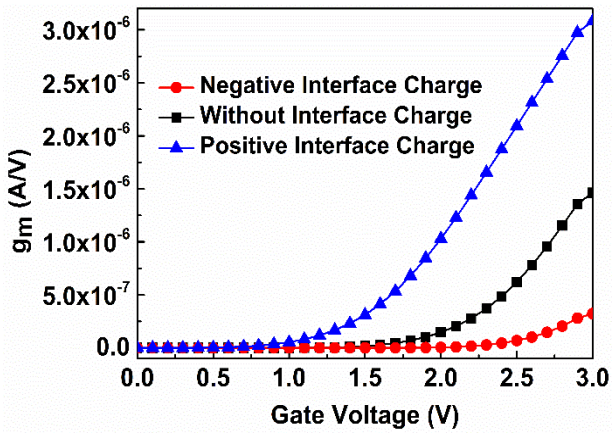
Fig. 3 – Total electric field for $N_f = \pm 1$ (× 10^{12}) cm^{-2}

3. INFLUENCE OF LOCALIZED CHARGE DENSITY

This section depicts the influence of localized charge density and polarity on FE-DMGAA TFET at room temperature. The influence of localized charge density on total electric field is shown in Fig. 3. It is explicit from Fig. 3 that the peak of electric field enhances (suppresses) by 27.27 % (45.45 %) against the fresh device (without interface charge) for positive (negative)



a



b

Fig. 4 – (a) Influence of localized charges on I_D-V_{GS} characteristics at fixed $V_{DS} = 0.1$ V; (b) influence of localized charges on transconductance as a function of gate voltage at fixed $V_{DS} = 0.1$ V

localized charges. The enhancement (suppression) of total electric field is referred to the decrease (increase) in flat band voltage (V_{FB}) for positive (negative) localized charges. Consequently, the decrease (increase) in flat band voltage enhances (suppresses) the effective gate bias, which yields in higher (lower) band bending of conduction and valence band.

Variation in transfer characteristics in presence of different localized charges is shown in Fig. 4a. Increase (decrease) in current is the reason behind the enhancement (suppression) in the band bending of conduction and valence bands caused due to decrease (increase) in flat band voltage. ON current enhances (suppresses) by 239.2 % (85.48 %) against fresh device for positive (negative) localized charges. Further, it is observed that I_{OFF} deteriorates considerably for donor trap charge from an order of 10^{-19} A to 10^{-12} A. Fig. 4b shows the variation of transconductance (g_m) with different localized charges. It is evident from the figure that g_m is higher (lower) for positive (negative) localized charge with regard to the undamaged device. Furthermore, the influence of localized charge is observed on high-frequency performance of the device i.e. cutoff frequency (f_T) and transconductance frequency product (TFP). Fig. 5 presents the impact of localized charge on f_T and TFP. f_T increases (decreases) by 111.69 % (77.87 %) for positive (negative) localized charges against undamaged device,

because of direct dependence on g_m. TFP elucidates the compromise between bandwidth and power [18]. It is clearly observable from the figure that TFP increases (decreases) by 31.6 % (66.43 %) for donor (acceptor) localized charges with regard to undamaged device.

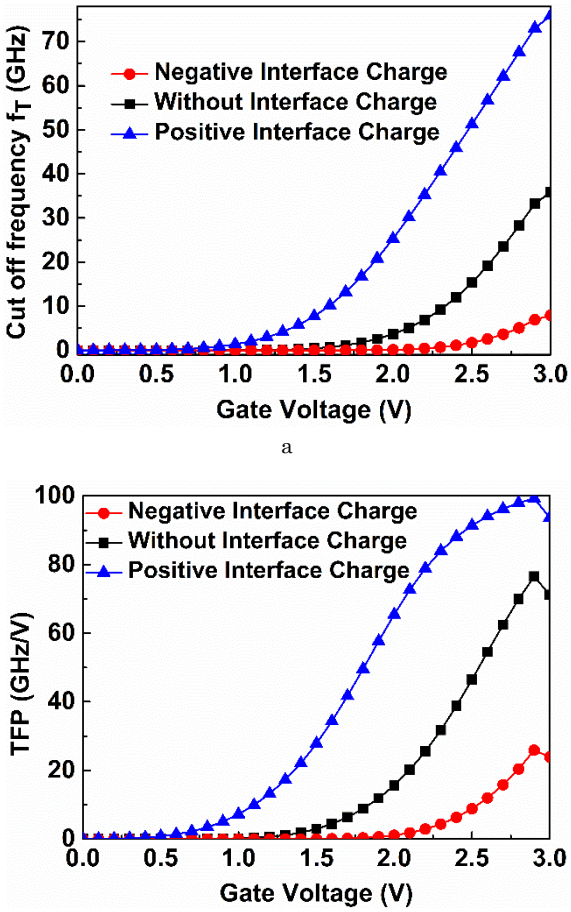


Fig. 5 – (a) Influence of localized charges on f_T as a function of V_{GS} at fixed V_{DS} = 0.1 V; (b) influence of localized charges on TFP as a function of gate voltage at fixed V_{DS} = 0.1 V

In order to improve linearity, the transconductance of the device should be invariant with regard to input bias. Unfortunately, the transconductance of TFET varies with gate voltage that depicts the non-linear characteristics of TFET. Investigation of linearity and distortion of the device is carried out by analyzing certain FOMs that are higher order transconductance (gm_2, gm_3), VIP2, VIP3, and IMD3, which are defined as:

$$VIP2 = 4\times\left(\frac{gm}{gm_2}\right), \text{where } gm_n = \frac{\partial^n I_D}{\partial V_{GS}{}^n}, \quad (3.1)$$

$$VIP3 = \sqrt{24\times\frac{gm}{gm_3}}, \quad (3.2)$$

$$IMD3 = \left[4.5\times(VIP3)^3\times gm_3\right]^2\times R_s, \quad (3.3)$$

where Rs = 50 Ω.

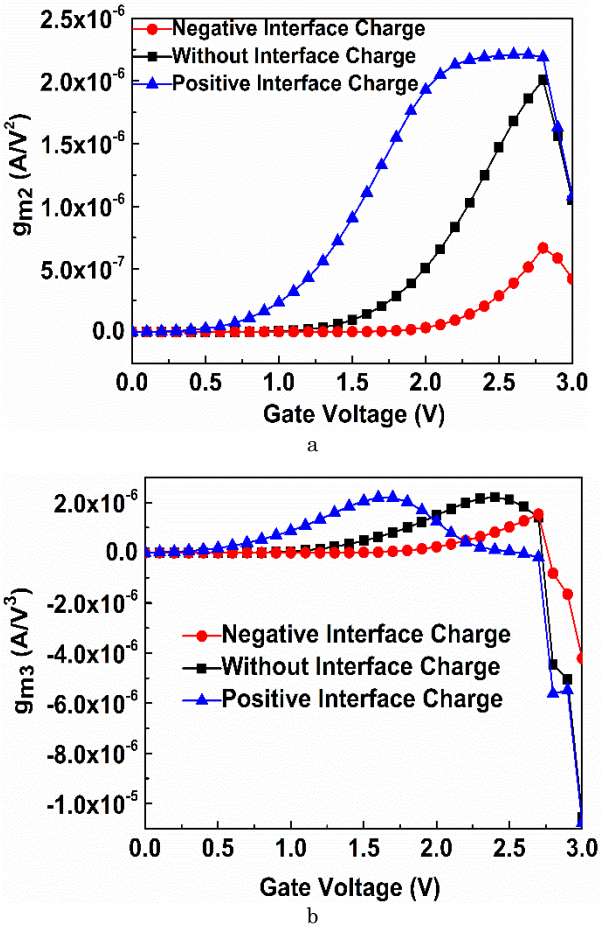
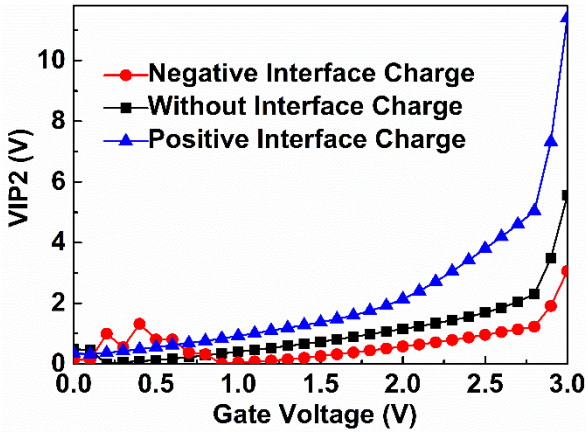


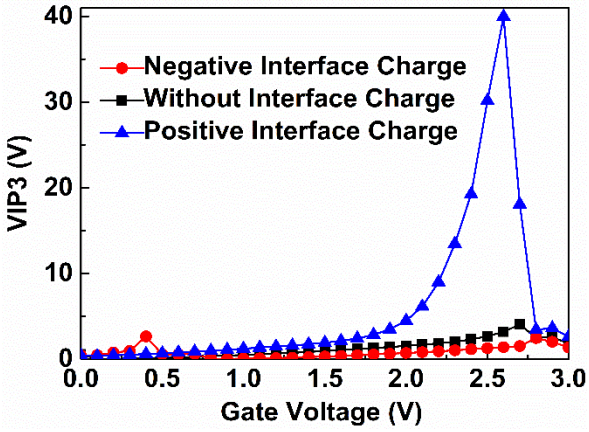
Fig. 6 – (a) Influence of localized charge on gm_2 as a function of V_{GS} at fixed V_{DS} = 0.1 V; (b) Influence of localized charge on gm_3 as a function of V_{GS} at fixed V_{DS} = 0.1 V

Second order (gm_2) and third order (gm_3) transconductances govern the limit on distortion [19]. In order to attain the least distortion, the magnitude of both high order transconductances should be low. The extrapolated input voltage at which the first and second harmonic voltages are equal is VIP2. Similarly, VIP3 depicts the extrapolated input voltage at which the first and third harmonic voltages are equal. IMD3 is the third order intermodulation distortion that depicts the extrapolated current at which the first and third order intermodulation harmonic currents are equal [20]. In order to attain high linearity and low distortion, higher values of VIP2, VIP3 and lower values of gm_2, gm_3 and IMD3 are required.

Fig. 6a presents the impact of localized charge on gm_2. It is evident from the figure that gm_2 increases (decreases) for donor (acceptor) trap charge at large V_{GS}. The variation of third order transconductance (gm_3) in the presence of localized charges is shown in Fig. 6b. To ensure better linearity, value of gm_3 should be low. The reason behind the distortion of the fundamental signal is gm_3. However, a lower (higher) value of gm_3 is observed for donor (acceptor) trap charge at higher V_{GS}. For minimizing the non-linear characteristics, the DC bias should be adjacent to zero crossover point (ZCP). ZCP is the gate voltage at which third order transconductance is zero. ZCP shifts with regard to localized charge i.e. for donor (acceptor) trap charge ZCP moves towards lower (higher) V_{GS}.



a



b

Fig. 7 – (a) Influence of localized charge on VIP2 as a function of V_{GS} at fixed V_{DS} = 0.1 V; (b) Influence of localized charge on VIP3 as a function of V_{GS} at fixed V_{DS} = 0.1 V

Fig. 7a and Fig. 7b show the influence of localized charges on VIP2 and VIP3 respectively. Higher values of VIP2 and VIP3 are required for improved linearity. It is clearly observable from Fig. 7a and Fig. 7b that the peak value of VIP2 and VIP3 increases (decreases) for positive (negative) localized charge as compared to the undamaged device. VIP2 enhances (suppresses) by 105.4 % (44.86 %) against fresh device for donor (acceptor) charges. The movement of the peaks towards higher V_{GS} depicts a larger gate to source voltage requirement to conserve the linearity. In order to have low distortion and negligible non-linearity, the value of IMD3 should be low. Variation in IMD3 in the presence of localized charge is shown in Fig. 8. Positive (negative) localized charge has lower (higher) value of IMD3 in contrast to undamaged device.

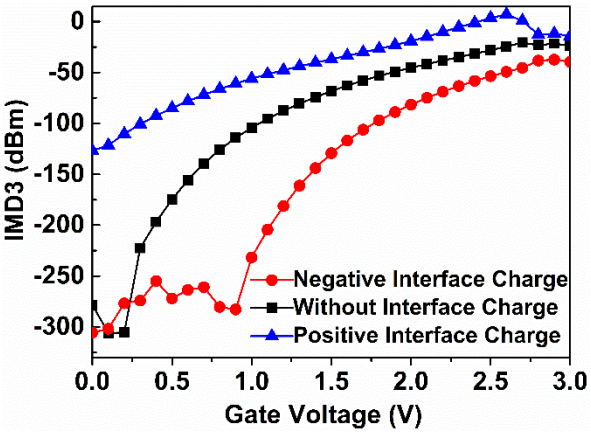


Fig. 8 – Influence of localized charge on IMD3 as a function of V_{GS} at fixed V_{DS} = 0.1 V

4. CONCLUSIONS

In this work, a ferroelectric-based tunnel FET device (FE-DMGAA-TFET) is proposed. The influence of localized charges on electrical performance and certain FOMs of linearity and distortion is analyzed. Since these localized charges always exist in practical devices, a comprehensive analysis considering the influence of these charges is required for device optimization. It has been examined that the ON-state current increases by more than ten folds after incorporating a ferroelectric material as gate insulator. It has been observed through numerical calculations that the third order intermodulation distortion (IMD3) is low for negative localized charge thereby reducing distortion, which is suitable for circuit reliability. It has also been noticed that the localized charges (donor and acceptor) present at the interface of silicon channel and interface layer alter the flat band voltage. Consequently, the donor-localized charges degrade the performance of the device. The impact of donor-localized charge in saturation region is marginal highlighting the application of proposed device for amplification applications.

REFERENCES

1. D.J. Frank, R.H. Dennard, E. Nowak, P.M. Solomon, Y. Taur, H.S.P. Wong, *Proc. IEEE* **89**, 259 (2001).
2. K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, *Proc. IEEE* **91**, 305 (2003).
3. A.C. Seabaugh, Q. Zhang, *Proc. IEEE* **98**, 2095 (2010).
4. S.O. Koswatta, M.S. Lundstrom, D.E. Nikonov, *IEEE T. Electron Dev.* **56**, 456 (2009).
5. E.H. Toh, G.H. Wang, G. Samudra, Y.C. Yeo, *J. Appl. Phys.* **103**, 104504 (2008).
6. S. Sant, K. Moselund, D. Cutaia, H. Schmid, M. Borg, H. Riel, A. Schenk, *IEEE T. Electron Dev.* **63**, 4240 (2016).
7. A.S. Verhulst, B. Sorée, D. Leonelli, W.G. Vandenberghe, G. Groeseneken, *J. Appl. Phys.* **107**, 024518 (2010).
8. M.H. Lee, Y.T. Wei, J.C. Lin, C.W. Chen, W.H. Tu, M. Tang, *AIP Adv.* **4**, 107117 (2014).
9. G.A. Salvatore, D. Bouvet, A.M. Ionescu, *2008 IEEE International Electron Devices Meeting*. **8**, 1 (2008).
10. C. Jiang, R. Liang, J. Xu, *IEEE T. Nanotechnol.* **16**, 58 (2017).
11. U. Schroeder, E. Yurchuk, J. Müller, D. Martin, T. Schenk, P. Polakowski, C. Adelmann, M.I. Popovici, S. Kalinin, T. Mikolajick, *J. Appl. Phys.* **53**, 08LE02 (2014).
12. Y. Qiu, R. Wang, Q. Huang, R. Huang, *IEEE T. Electron Dev.* **61**, 1284 (2014).
13. J. Madan, R. Chaujar, *IEEE T. Electron Dev.* **64**, 1482 (2017).
14. B. Awadhiya, S. Pandey, K. Nigam, P.N. Kondekar, *Superlattice. Microstructure.* **111**, 293 (2017).
15. *Silvaco TCAD User's Manual (2016).*
16. M. Kobayashi, T. Hiramoto, *AIP Adv.* **6**, 025113 (2016).

17. Z.X. Chen, H.Y. Yu, N. Singh, N.S. Chen, R.D. Sayanthan, G.Q. Lo, D.L. Kwong, *IEEE Electron Dev. Lett.* **30**, 754 (2009).
18. K.P. Pradhan, S.K. Mohapatra, P.K. Sahu, D.K. Behera, *Microelectron. J.* **45**, 144 (2014).
19. P. Ghosh, S. Haldar, R.S. Gupta, M. Gupta, *IEEE T. Electron Dev.* **59**, 263 (2012).
20. S. Kaya, W. Ma, *IEEE Electron Dev. Lett.* **25**, 308 (2004).

Дослідження впливу локалізованих зарядів на параметри лінійності та спотворення для транзисторів з круговим затвором з сегнетоелектричних подвійних матеріалів

Varun Mishra, Yogesh Kumar Verma, Santosh Kumar Gupta

Electronics and Communication Engineering Department, Motilal Nehru National Institute of Technology, Allahabad, India

Масштабування польових транзисторів (MOSFETs) менше 20 нм призводить до деяких ускладнень, таким як високий струм вимкненого стану через зменшення товщини оксиду затвору, індукованому стоком зниженню бар'єру та іншім ефектам короткого каналу. З цієї точки зору, тунельний польовий транзистор (TFET) є найкращим претендентом, щоб затьмарити MOSFETs у нанорозмірному режимі. Властивість негативної ємності сегнетоелектричного матеріалу поєднується з міжзонним тунельним механізмом TFET з метою посилення струму увімкненого стану пристрою. Як сегнетоелектричний шар (затворний діелектрик) використовують оксид гафнію, легований кремнієм ($Si:HfO_2$). Більш низька діелектрична проникність і сумісність з технологічним процесом робить його підходящим сегнетоелектричним матеріалом на відміну від перовскітних матеріалів. У цій роботі досліджується вплив локалізованих зарядів на електричні показники, лінійність і параметри спотворення тунельного транзистору з круговим затвором з сегнетоелектричних подвійних матеріалів (FE-DMGAA-TFET). Наявність оксидних зарядів змінює точку зміщення пристрою; отже, його вплив потрібно досліджувати з точки зору показників якості лінійності та спотворення. Локалізований заряд оксиду може бути як позитивним, так і негативним залежно від енергетичного рівня пастки щодо рівня Фермі. Виявлено, що струм вимкненого стану значно збільшується для донорно-локалізованого заряду від 10^{-19} до 10^{-12} А. Нелінійність і спотворення пристрою зменшуються у присутності негативного локалізованого заряду. За допомогою чисельних розрахунків було проаналізовано, що внаслідок донорсько-локалізованих зарядів підпороговий режим значно погіршується, підкреслюючи вимогу інтенсивного аналізу в цьому інтервалі для майбутньої ринкової ніші електроніки. Однак вплив акцепторно-локалізованих зарядів на продуктивність пристрою є незначним.

Ключові слова: Сегнетоелектрик, Локалізовані заряди, Негативна ємність, Інтермодуляційні спотворення третього порядку, Точка нульового переходу.