Journal of Nano- and Electronic Physics
Vol. **11** No 4, 04021(6pp) (2019)

Журнал нано- та електронної фізики
Том **11** № 4, 04021(6cc) (2019)

BSIM3v3 Characterization and Simulation of MOS $Si_{1-x}Ge_x$ Transistors with 130 nm Submicron Technology

M. Hebali[1,2,*], M. Bennaoum[1], M. Benzohra[3], D. Chalabi[2], A. Saïdane[2]

[1] *Department of Electrotechnical, University Mustapha STAMBOULI Mascara, 29000 Mascara, Algeria*
[2] *Laboratory: CaSiCCe, ENP Oran-MA, 31000 Oran, Algeria*
[3] *Department of Networking and Telecommunications, University of Rouen, Laboratory LECAP, 76000, France*

(Received 13 February 2019; revised manuscript received 02 August 2019; published online 22 August 2019)

A prospective of work and a feasibility study are undertaken on $MOSi_{1-x}Ge_x$ transistors with a 130 nm submicron technology. BSIM3v3 model has been used to analyze the transistors' operation, according to the study of the effect of Germanium fraction x ($x = 0$ to $x = 1$) on electrical performance of these transistors taking into account the influence of temperature. PSpice parameters of two different transistors $NMOS_{1-x}Ge_x$ and $PMOS_{1-x}Ge_x$ have been calculated and used in the modeling. The output and transfer electrical characteristics have been determined in the temperature range – 200 to 200 °C. The regime subthreshold was also addressed by calculating I_{ON} and I_{OFF} currents as a function of V_{GS} for constant V_{DD}. Simulation results show that the above transistors work properly in a regime under a threshold voltage of about 1.2 V. They can be used in low voltage and low power microelectronics by controlling the germanium x fraction.

Keywords: $Si_{1-}Ge_x$, BSIM3v3, 130 nm technology, I-V characterization, Temperature.

DOI: 10.21272/jnep.11(4).04021 PACS number: 85.30.Tv

1. INTRODUCTION

Search for increasingly enhanced electronic performance, such as speed, low power consumption, etc., requires the use of new components to meet ever increasing demands of telecommunications and multimedia technologies. The use of silicon has shown its limitations in modern telecommunications and in nanometric integrated circuit manufacturing. Reducing transistor size causes degradation in silicon transistor performance and hence a need for alternative solutions. One of such solutions is the use of III-V or IV-IV semiconductors that have better properties than silicon such as mesh size, gap width, carrier mobility, etc.

Band gap engineering has enabled significant advances in component technologies. Germanium, due to its compatibility with silicon (the two are completely miscible), its lattice mismatch, band structure, high mobility of carriers (electrons and holes), lowest gap with respect to silicon, forms with Si the material SiGe. SiGe is introduced into bipolar and CMOS technologies to boost the limits faced by silicon devices [2].

The use of SiGe materials in microelectronic devices needs an understanding of doping impurity diffusion mechanisms in these alloys in order to master concentration profiles during manufacturing of components. At present, SiGe offers mature processes and substantial yields to compete with traditional technologies [3]. Thus, SiGe heterojunction bipolar transistors and field effect transistors are good alternatives for power amplification, communication systems and digital circuits requiring high speed, high integration and low cost. The addition of Ge to Si with a fraction x gives $Si_{1-x}Ge_x$ alloys. Their use in electronic and optoelectronic devices has grown considerably due to the additional degrees of freedom it offers in the design and optimization of devices [4]. Many studies have been made on $Si_{1-x}Ge_x$ heterojunction MOS transistors with very small x values for solar cells [5], modulation, sensors, etc. applications [6]. Recently, SiGe alloy has been used to realize integrated circuits with CMOS and BiCMOS technologies like PLL, QVCO, mixer and low-noise amplifier LNA [7, 8].

The goal of this work is to optimize performance of 130 nm $Si_{1-x}Ge_x$ heterojunction MOS transistors depending on Ge fraction x in silicon. To do so, BSIM3v3 Orcad PSpice software is used with $MOSi_{1-x}Ge_x$ transistor parameters defined in terms of dimensions and doping in different areas of transistor. On the basis of determined equations, components are simulated for five values of Ge fraction x ($x = 0$, $x = 0.25$, $x = 0.5$, $x = 0.75$ and $x = 1$). Two extreme cases, $x = 0$ and $x = 1$, corresponding to pure silicon and pure germanium materials are used to set the model. This interval of x is used to study evolution of various electronic characteristics of $MOSi_{1-x}Ge_x$ transistors as a function of Ge fraction x.

2. BSIM3V3 MODEL

BSIM3v3 is the latest standard MOSFET model used in industry for highly digital and analog submicron circuit designs under the name BSIM (Berkeley Short-Channel IGFET Model). BSIM3v3 is based on Poisson's equation and the progressive approximation of the channel and a 2D quasi consistency analysis that takes into account the effects of the device geometry and process parameters [9]. For a MOSFET with a channel having a large length to width ratio, the threshold voltage assumes that the channel is uniform and uses a one dimensional Poisson equation (channel vertical direction). This model is valid only when the substrate doping is constant and uniform, and for a long channel. Under these conditions, the potential is

* mourad.hebali@univ-mascara.dz

uniform along the channel. Changes must be made when substrate doping is not uniform and/or channel dimensions are short and narrow, or both at once. The effects of these hypotheses on threshold voltage are taken into account in writing the full expression of this voltage in BSIM3v3 model.

Table 1 – The model control parameters

Parameters	Description	Values
Level	Level of the model used	7
Version	Version of the model	3.2
MobMod	Model used for mobility	1
CapMod	Capacity models	3
T_{ox}	Thickness of gate oxide (m)	$2.3\cdot10^{-9}$
X_j	Junction depth (m)	$1\cdot10^{-7}$
X_t	Doping depth (m)	$1.05\cdot10^{-7}$
N_{ch}	Channel doping concentration (cm^{-3})	NMOS $2.3549\cdot10^{17}$
		PMOS $4.1589\cdot10^{17}$
VBM	Maximum polarization of the body applied in the calculation of V_{th} (V)	NMOS-3
		PMOS-2.5
L	Channel length (nm)	130
W	Channel width (nm)	160

3. RESULTS AND DISCUSSION

Table 1 shows PSpice parameters for BSIM3v3 model.

3.1 Output Characteristics $I_D = f(V_{DS})$

Five NMOS$Si_{1-x}Ge_x$ and five PMOS$Si_{1-x}Ge_x$ transistors in forward bias mode have been investigated. V_{GS} voltage was 1.2 V and V_{DS} voltage was varied from 0 to 1.2 V to distinguish the linear and saturation regions. Fig. 1 shows $I_D = f(V_{DS})$ output characteristics for NMOS $Si_{1-x}Ge_x$ and PMOS $Si_{1-x}Ge_x$.

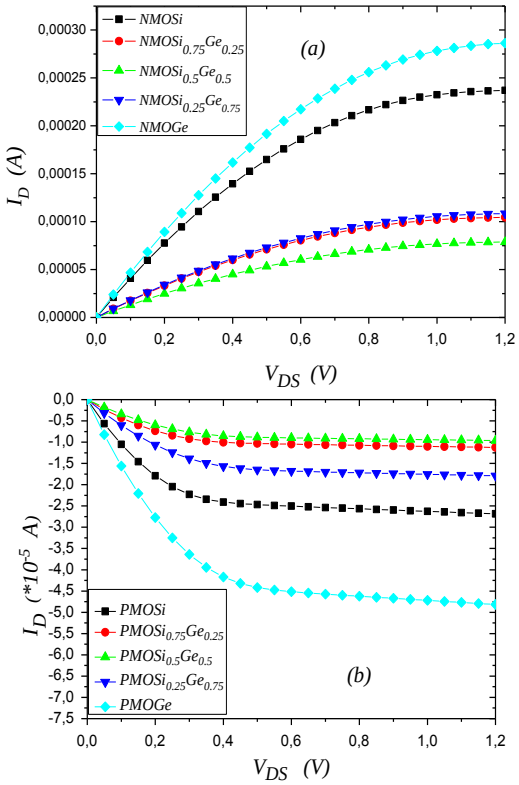

Fig. 1 – $I_D = f(V_{DS})$ output characteristics for (a) NMOS$Si_{1-x}Ge_x$ and (b) PMOS$Si_{1-x}Ge_x$

Drain current of NMOS $Si_{1-x}Ge_x$ transistors decreases with Ge fraction x from $x = 0$ (silicon transistor) to $x = 0.5$, then increases with $x > 0.5$ to $x = 1$ (germanium transistor) as shown in Fig. 2. NMOS$Si_{0.5}Ge_{0.5}$ transistors have the lowest drain current. To show I_D currents of NMOS $Si_{1-x}Ge_x$ and PMOS $Si_{1-x}Ge_x$ transistors on the same graph, drain current of NMOS $Si_{1-x}Ge_x$ has been shifted by 0.5×10^{-4} A. For the same fraction x, the drain current of NMOS $Si_{1-x}Ge_x$ transistor is 10 times larger than that of PMOS $Si_{1-x}Ge_x$ transistor. At $V_{DS} = 1.2$ V, I_D curves in Fig. 2 can be fitted to the following equations:

$$I_D = \left(15,43x^4 - 28,65x^3 + 23,28x^2 - 9,57x + 2,37\right).10^{-4}$$

for NMOS $Si_{1-x}Ge_x$ transistors and

$$I_D = \left(17,1x^4 - 29,95x^3 + 26,17x^2 - 11,18x + 2,86\right).10^{-5}$$

for PMOS $Si_{1-x}Ge_x$ transistors.

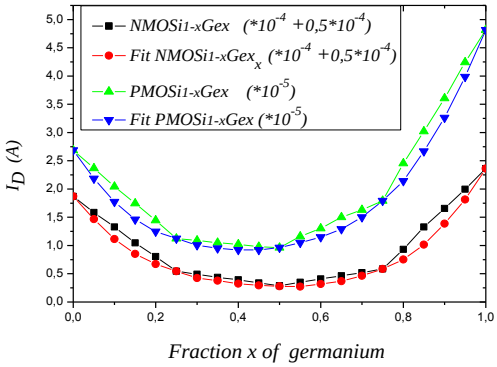

Fig. 2 – Change of absolute values of I_D with Ge fraction x

Results show that calculated and simulated transistors have good features and functions compared to those in literature [10, 11].

For NMOS $Si_{1-x}Ge_x$ transistors, the drain current characteristic $I_D = f(V_{DS})$ is:

$$I_{DS} = \mu_{eff} C_{ox} \frac{W}{L} \frac{1}{1 + V_{DS} / E_{sat} L} \left(V_{gs} - V_{th} - \frac{A_{bulk} V_{DS}}{2} \right) V_{DS} \,. \quad (1)$$

In (1), the geometrical channel ratio (W_{eff}/L_{eff}) is constant and the type of oxide used is the same for all NMOS $Si_{1-x}Ge_x$ transistors. Hence, the current is directly proportional to mobility that is responsible for changes in output characteristics. This mobility of electrons and holes in $Si_{1-x}Ge_x$ materials changes with germanium fraction x as shown in Fig. 3 [12].

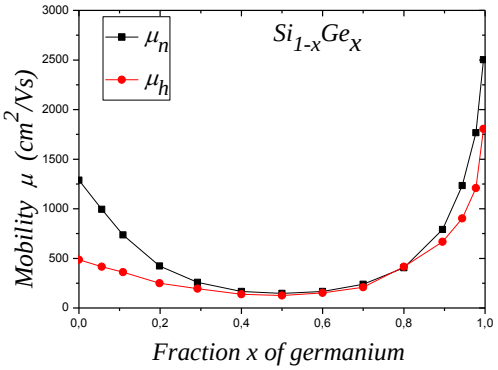

Fig. 3 – Mobility μ_n and μ_h variation in Si_xGe_{1-x} materials

One way to explain the U-shaped curves $I_D = f(x)$ of $Si_{1-x}Ge_x$ transistors is that in an alloy, the phonons will experience a greater number of collisions because the lattice sites can be occupied randomly by silicon or germanium atoms. The mean free path of germanium will be lower, thus inducing a less efficient heat transport.

$Si_{1-x}Ge_x$ transistors heat up more than silicon ones because of this low heat removal. In turn, this poor heat conduction degrades transistor electrical properties.

Fig. 4 shows the variation of thermal conductivity of $Si_{1-x}Ge_x$ with Ge fraction x [1].

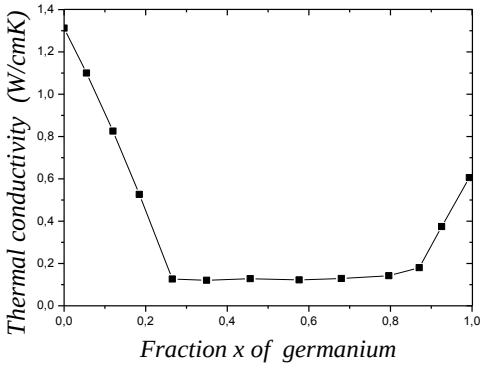

Fig. 4 – Variation of thermal conductivity of $Si_{1-x}Ge_x$ with germanium fraction x [1]

NMOS $Si_{1-x}Ge_x$ transistors are considered with boron doped substrates. According to Gavelle et al. [13], immiscibility of tetravalent dopants in $Si_{1-x}Ge_x$ is lowest when Ge x content in silicon is around 0.5. Movement of impurities in a crystal depends on activation energy, which in turn depends on migrant species nature and type. Crystal lattice (constrained and unconstrained), defects and their natures have an effect on impurity diffusion and transport phenomena in SiGe. So for a low doping, device drain current must be low compared to that of devices where x is not 0.5. In this case, the device can handle only a low power. Others authors [14, 15] have argued that the phenomenon remains unknown and there is no convincing explanation. Drain current depends strongly on boron diffusion coefficient D in $Si_{1-x}Ge_x$ as shown in Fig. 5. Thus, there is a similarity in the shape of current obtained in this work and the shape of diffusion coefficient obtained by Laitinen [16] and MacVay [17].

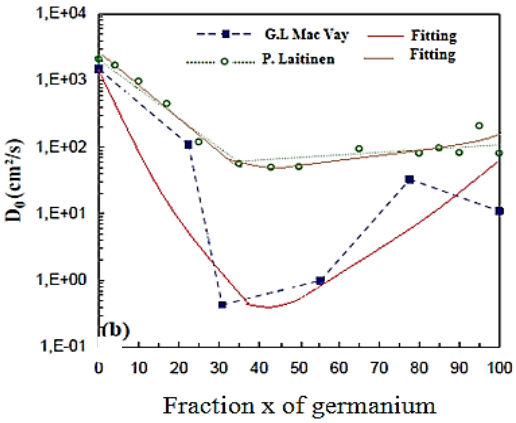

Fig. 5 – Evolution of boron diffusion at 900 °C for constrained and unconstrained SiGe alloys with % Ge content [13]

3.2 Transfer Characteristics $I_D = f(V_{GS})$

To simulate transfer characteristics $I_D = f(V_{GS})$ of NMOS $Si_{1-x}Ge_x$ transistors, an applied voltage V_{DS} = 1.2 V was used with V_{GS} voltage varied from 0 V to 1.2 V. Fig. 6 shows the results of simulation.

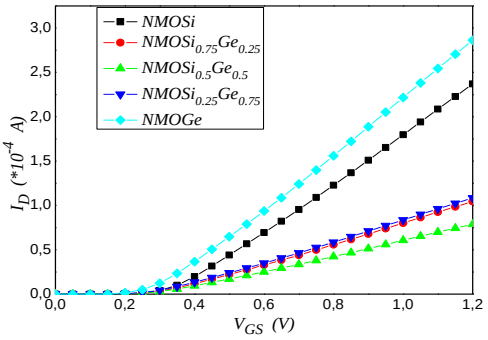

Fig. 6 – Transfer characteristics $I_D = f(V_{GS})$ of NMOS $Si_{1-x}Ge_x$

Fig. 6 shows two different operating modes: blocked and linear. It also gives the value of the threshold voltage V_{th} of each transistor as a function of the Ge fraction x. Such characteristics are found to be similar to evolution of threshold voltage of MOS transistors with germanium fraction x reported in literature [18, 19].

In the blocked region of operation, the gate-source voltage bias is less than the threshold voltage ($V_{GS} < V_{th}$). All $MOSi_{1-x}Ge_x$ transistors have the same characteristics and drain currents are very low ($I_D \approx 0$). These are leakage currents. The $MOSi_{1-x}Ge_x$ transistor operation is independent of the Ge fraction x. In the linear region, where $0 < V_{GS} - V_{th} < V_{DS}$, a gradual increase of V_{GS} ($V_{GS} > V_{th}$) leads to an increase in electron

concentration n in the channel. The conductivity of the channel increases according to:

$$\sigma = nq\mu_n . \quad (2)$$

$MOSi_{1-x}Ge_x$ transistor transfer characteristics are straight lines with the slope dI_D/dV_{GS} changing with x. The parameters affecting these slopes are the carrier concentration $n(p)$ and the mobility $\mu_n(\mu_p)$ that change with germanium fraction x. These devices become transconductances (dI_d/dV_{gs}) controlled by voltage. Results show that MOGe transistors have a high transconductance compared to the low one of MOS $Si_{0.5}Ge_{0.5}$ transistors.

3.3 Highlighting Current I_{ON} and I_{OFF}

In the model, the I_{ON} current and leakage current I_{OFF} are defined by the following relationships:

$$I_{ON} = I_D \left| V_{GS} = V_{DD}, V_{DS} = V_{DD}, V_{bs} = 0 \right. , \quad (3)$$

$$I_{OFF} = I_D \left| V_{GS} = 0, V_{DS} = V_{DD}, V_{bs} = 0 \right. . \quad (4)$$

The leakage current I_{OFF} is due mainly to the sub-threshold current and to junction currents I_{jDB} and I_{jSB}, while the gate current is negligible. Compared to current I_{OFF} at $V_{GS} = 0$ V, I_{gb}, I_{gs} and I_{jbs} currents are zero. To do so, the transistor has been biased such as $V_{DS} = V_{DD}$ and $V_{bs} = 0$ (substrate bias) and the curve $\log(I_D) = f(V_{GS})$ has been plotted:

$$log\left(I_d\right) = f\left(V_{gs}\right) . \quad (5)$$

Fig. 7 shows the simulation results.

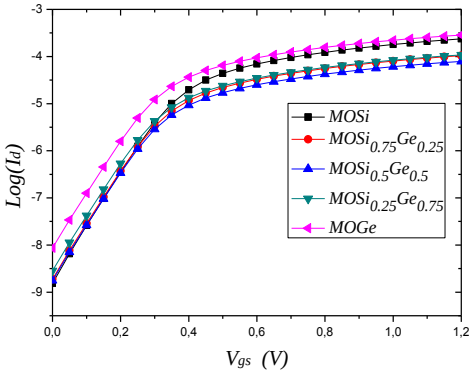

Fig. 7 – MOS $Si_{1-x}Ge_x$ transistor leakage currents I_{ON} and I_{OFF}

Table 2 shows leakage currents I_{ON} and I_{OFF} obtained from simulation. For the leakage current I_{OFF}, $Si_{1-x}Ge_x$ NMOS transistors operate in sub-threshold regime. For this regime, the drain current expression is written as [9]:

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{Th} - V_{off}}{\eta V_T}\right)\left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right). \quad (6)$$

Since the voltage V_{OFF} is very low, Eq. (6) becomes:

$$I_D = \frac{W}{L} I_0 \, exp\left(\frac{V_{GS} - V_{Th}}{\eta V_T}\right)\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (7)$$

with

$$I_0 = \mu_{eff}\sqrt{\frac{q\varepsilon_{SiGe}N_{ch}}{2\Phi_s}}V_T{}^2 = \mu_{eff}C_{ox}\left(\eta - 1\right)V_T{}^2 . \quad (8)$$

Table 2 – Leakage currents I_{ON} and I_{OFF} values for NMOS $Si_{1-x}Ge_x$ transistors

Currents / Transistors	I_{OFF} (nA)	I_{ON} (mA)
MOSi	7.89	0.237
$MOSi_{0.75}Ge_{0.25}$	1.889	0.104
$MOSi_{0.5}Ge_{0.5}$	1.775	$7.881\ 10^{-2}$
$MOSi_{0.25}Ge_{0.75}$	2.850	0.108
MOGe	8.658	0.286

The leakage current I_{OFF} is under the influence of two important variables, namely the threshold voltage and carrier mobility. To determine this leakage current, the transistor is biased such as $V_{DS} = V_{DD}$. In this case, the equation (7) is written taking into account equation (8):

$$I_{OFF} = a\mu_{eff}\left(\eta - 1\right)exp\left(\frac{-V_{Th}}{\eta V_T}\right), \quad (9)$$

where a is given by:

$$a = \frac{WC_{ox}V_T{}^2}{L}\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right). \quad (10)$$

The leakage current I_{OFF} of NMOS $Si_{1-x}Ge_x$ transistors varies with the germanium fraction x. This variation is very low and is between 1.775 nA and 8.65 nA. The current I_{ON} of NMOS $Si_{1-x}Ge_x$ transistors varies with mobility and the germanium fraction x. The effect of the threshold voltage is very low on the variation of this current, as shown in Fig. 7.

3.4 Effect of Temperature on the Operation of $MOSi_{1-x}Ge_x$ $g_m = f(T)$ Characteristic

Transconductance of MOS transistors is an important electrical parameter that characterizes their performance. The transfer characteristic is used to study the effect of temperature on transconductance g_m that is determined by the slope of the current I_D relative to the V_{GS} voltage in saturation region. It is given by:

$$g_m\left(T\right) = \frac{dI_D\left(T\right)}{dV_{GS}\left(T\right)} . \quad (11)$$

The chosen temperature range for this study is between – 200 °C and 200 °C so to make a comparison with silicon transistors. Fig. 8 shows the variation of the transconductance g_m with temperature for different values of fraction x for NMOS $Si_{1-x}Ge_x$ and PMOS $Si_{1-x}Ge_x$ transistors.

Transistors work in saturation zone ($V_{DS} > V_{dsat}$). The drain current from BSIM3v3 model is:

$$I_D = WC_{ox}\left(V_{gs} - A_{bulk}V_{dsat}\right)v_{sat} , \quad (12)$$

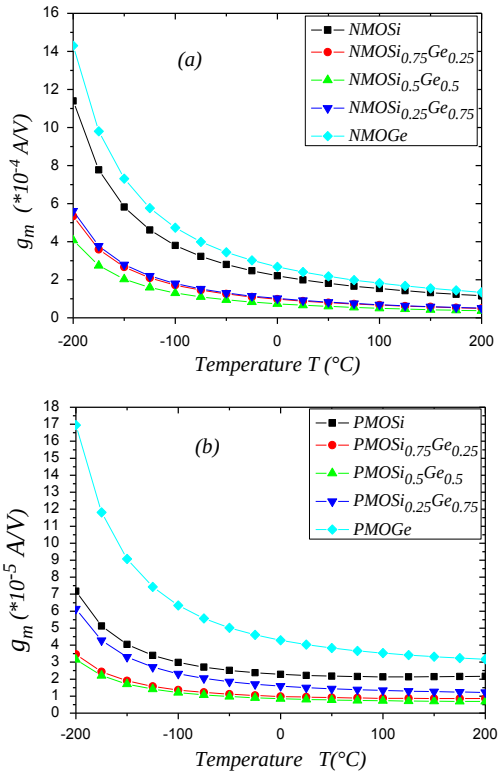

Fig. 8 – Transconductance g_m variation with temperature for different values of fraction x for (a) NMOS $Si_{1-x}Ge_x$ and (b) PMOS $Si_{1-x}Ge_x$ transistors

where A_{bulk} and V_{dsat} are independent variables that change with voltage V_{GS}. Differentiating I_D versus V_{GS}, the transconductance g_m relationship becomes:

$$g_m = \frac{dI_D}{dV_{GS}} = WC_{ox}v_{sat} = \frac{1}{2}WC_{ox}E_{eff}\mu_{eff}\,. \qquad (13)$$

Equation (13) gives the evolution of transconductance with temperature for different $MOSi_{1-x}Ge_x$ transistors. This relationship is related to the variation of velocity saturation of carriers that is function of temperature, where the variation of the mobility is itself a function of temperature. Equation (13) can also be written as:

$$g_m(T) = WC_{ox}v_{sat}(T) = \frac{1}{2}WC_{ox}E_{eff}\mu_{eff}(T)\,. \qquad (14)$$

Velocity saturation with temperature is given by:

$$v_{sat}(T) = v_{sat} - A_T\left(\frac{T}{T_{nom}} - 1\right), \qquad (15)$$

where A_T is a default setting and v_{sat} is saturation velocity at nominal temperature (T_{nom}). For this model, the velocity saturation decreases with temperature [9] as shown by equation (15). For this model, like the velocity saturation, the mobility μ_{eff} is:

$$\begin{aligned} U_a(T) &= U_A + U_{A1}\left(\frac{T}{T_{nom}} - 1\right) \\ U_b(T) &= U_B + U_{B1}\left(\frac{T}{T_{nom}} - 1\right) \\ U_c(T) &= U_C + U_{C1}\left(\frac{T}{T_{nom}} - 1\right) \\ \mu_O(T) &= \mu_0\left(\frac{T}{T_{nom}}\right)^{UTE} \end{aligned} \qquad (16)$$

where U_A, U_B, U_C, U_{C1} and UTE are default settings. As shown by the various above expressions (equation (16)), the change in velocity saturation or mobility leads to a decrease of transconductance with temperature (Fig. 8).

4. CONCLUSIONS

The PSpice parameters of MOS $Si_{1-x}Ge_x$ transistors with 130 nm technology are calculated and used in simulation under BSIM3v3 software. It has been shown that velocity saturation and mobility are responsible for the evolution of different electronic characteristics with germanium fraction x. Simulations showed that this model of transistors operates with a low voltage of about 1.2 V. They also showed that these transistors operate correctly in a regime sub-threshold and so they can be used in low voltage low power applications by controlling the germanium fraction x.

REFERENCES

1. Yann Bogumilowicz, *Epitaxie et gravure d'heterostructures $Si/Si_{1-x}Ge_x$ pour applications dans les technologies MOS* (Ecole Centrale de Lyon: 2005).
2. Pierre-Marie Mans, *Optimisation de transistors bipolaires à hétérojonctions Si/SiGe:C en technologie BiCMOS 0.25 µm pour les applications d'amplification de puissance* (L'université bordeaux I: 2008).
3. J.B. Johnson, A.J. Joseph, D.C. Sheridan, *IEEE J. Solid State Circuit*. **39**, 1605 (2004).
4. Ali K. Okyay, Duygu Kuzum, Salman Latif, David A.B. Miller, Krishna C. Saraswat, *IEEE T. Electron Dev.* **54**, 3206 (2007).
5. Sabine Abdu Hadi, Pouya Hashmi, Nicole Dilello, Ammar Nayfel, July L. Hoyt, *MRS Proc.* **1447**, 12 (2012).
6. John E. Ayers, *Heteroepitaxy of semiconductors: Theory: growth: and caracterisation* (Boca Raton, Florida, USA: CRC Press Taylor & Francis Group: 2007).
7. Jun-Da Chen, Song-Hao Wang, *Circuits Syst. Signal Process.* **36**, 2635 (2016).
8. Peter Song, Ahmet Cagri Ulusoy, Robert L. Schmid, John D. Cressler, *2014 IEEE MTT-S International Microwave Symposium (IMS2014)* (2014).
9. Yuhua Cheng, Chenming Hu, *Mosfet Modeling & BSIM3 User's Guide* (Kluwer Academic Publishers: University of California, Berkeley, USA: 2002).
10. Sergiy Durov, *High Ge content p-channel SiGe MOSFETs on Virtual Substrate* (University of Warwick: England: 2004).
11. Osama M. Nayfeh, Judy L. Hoyt, Dimitri A. Antoniadis, *IEEE T. Electron Dev.* **56**, 2264 (2009).
12. Otfried Madelung, *Semiconductors - Basic Data, 2nd revised Edition* (Springer: Verlag Berlin Heidelberg: 1996).
13. Mathieu Gavelle, *Etude expérimentale de l'interdiffusion*

Ge-Si à partir de sources solides Germanium sur Silicium. Application à la formation de couches graduelles $Si_{1-x}Ge_x$ pour les transistors pMOSFET (Micro et nanotechnologies: Microélectronique- INSA de Toulouse: 2008).
14. J.M. Bonar, A.F.W. Willoughby, A.H. Dan, B.M. McGregor, W. Lerch, D. Loeffelmacher, G.A. Cooke, M.G. Dowsett, *J. Mater. Sci.* **12**, 219 (2001).
15. P. Kuo, J.L. Hoyt, J.F. Gibbons, J.E. Turner, D. Lefforge, *Appl. Phys. Lett.* **67**, 706 (1995).
16. Pauli Laitinen, *Self- and impurity diffusion in intrinsic relaxed Silicon-Germanium* (University of Jyväskylä: Finlande: 2004).
17. G.L. McVay, A.R. DuCharme, *Phys. Rev. B* **9**, 627 (1974).
18. Wang Bin, Zhang He-ming, Hu Hui-yong, Zhang Yu-ming, Zhou Chun-yu, Li Yu-chen, *J. Cent. South Univ.* **21**, 2292 (2014).
19. Rashmi Mahajan, D.K. Gautam, *Silicon* **8**, 505 (2016).

BSIM3v3 характеристика та моделювання транзисторів MOS $Si_{1-x}Ge_x$ за 130 нм субмікронною технологією

M. Hebali[1,2], M. Bennaoum[1], M. Benzohra[3], D. Chalabi[2], A. Saïdane[2]

[1] *Department of Electrotechnical, University Mustapha STAMBOULI Mascara, 29000 Mascara, Algeria*
[2] *Laboratory: CaSiCCe, ENP Oran-MA, 31000 Oran, Algeria*
[3] *Department of Networking and Telecommunications, University of Rouen, Laboratory LECAP, 76000, France*

Перспективи та доцільність роботи представлені для транзисторів $MOSi_{1-x}Ge_x$ змодельованих за 130 нм субмікронною технологією. Модель BSIM3v3 використовувалася для аналізу роботи транзисторів відповідно до вивчення впливу фракції x германію (з $x = 0$ до $x = 1$) на електричні характеристики цих транзисторів з урахуванням впливу температури. PSpice параметри двох різних транзисторів $NMOSi_{1-x}Ge_x$ і $PMOSi_{1-x}Ge_x$ були розраховані і використані у моделюванні. Вихідні і перехідні електричні характеристики були визначені в інтервалі температур від – 200 до 200 °C. Субпороговий режим також розглядався шляхом обчислення струмів I_{ON} та I_{OFF} як функції V_{GS} для постійного V_{DD}. Результати моделювання показують, що вищезгадані транзистори працюють належним чином у режимі з пороговою напругою близько 1.2 В. Вони можуть бути використані в мікроелектроніці низької напруги та малої потужності шляхом керування фракцією x германію.

Ключові слова: $Si_{1-x}Ge_x$, BSIM3v3, 130 нм технологія, I-V характеристика, Температура.