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Optimization of *n*-MOS 6T Nanowire SRAM Bit Cell Based on Nanowires Ratio of SiNWTs

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In nowadays technology, the primary memory structure widely used in many digital circuit applications is a six transistor (6T) Static Random Access Memory (SRAM) bit cell. The main reason for minimizing memory bit cell to nanodimensions is to provide the SRAM integrated circuits (ICs) with the possible largest memory size per one chip, and the main unit in 6T SRAM bit cell is the MOSFET. One of the new MOSFET structures that overcome conventional MOSFET structure problems under minimization towards nanodimension is the silicon nanowire transistor (SiNWT). This study is the first to explore and optimize the nanowire ratio of driver to load (K_D/K_L) for a six *n*-channel SiNWT-based SRAM bit cell. The MuGFET simulation tool has been used to calculate the output characteristics of each transistor individually, and then these characteristics are implemented in the MATLAB software to produce the final static butterfly and current characteristics of nanowire 6T-SRAM bit cell. The demonstration of the driver to load transistors' nanowires ratio optimizations of nanoscale *n*-type SiNWT-based SRAM bit cell has been discussed. In this research, the optimization of K_D/K_L will strongly depend on inflection voltage and high and low noise margins (NMs) of butterfly characteristics. The improvement of NMs of butterfly characteristics has been done by increasing the drain current (I_{ds}) of the driver transistor. Also, the optimization in principle will depend on whether NMs are equal and high, and the inflection voltage (V_{inf}) is near to $V_{dd}/2$ values as possible. These principles have been used as limiting factors for optimization. The results show that the optimization strongly depends on the nanowire ratio, and the best ratio was $K_D/K_L = 4$. The increase in K_D/K_L leads to a continuous increase in NM_H, acceptable NM_L and low percentage increment of static power consumption (ΔP %) at $K_D/K_L = 4$.

Keywords: SRAM, SiNWT, Nanowire, N-MOS, Memory cell.

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1. INTRODUCTION

In nowadays technology, the primary memory structure widely used in many digital circuit applications is a six transistor (6T) Static Random Access Memory (SRAM) bit cell. Design of the integrated circuits (ICs) with higher possible integration (higher number of transistors per unit area) was considered the main Si technologies' goal in recent days, and SRAM chips are not exempt of this rule. The main reason for this issue is to provide the SRAM ICs with the possible largest memory size per one chip. The downscaling of conventional silicon metal-oxide-semiconductor-field-effect transistor (MOSFET) to nanodimensions produces many limitations. The researchers investigate new structures for FETs to overcome the downscaling limits of covenantal MOSFET structures. One of these structures is the silicon nanowire transistor (SiNWT) that has been widely investigated and studied under both the academic and semiconductor industry fields [1-6]. The research studies that have been published recently related to nanotransistors have focused on the characterization of these transistors in a wide range of applications in electronics, biomaterials, medicine, and energy production [7-20].

Fig. 1 represents the circuit diagram of the NMOS SRAM bit cell. This circuit has a MOSFET 6T SRAM bit cell consisting of two NMOS logic inverters (*n*-SiNWT-L and *n*-SiNWT-R load transistors and *n*-SiNWT-L and *n*-SiNWT-R driver transistors) and two transistors as a pass-gate to control the in (write) or out (read) bit. When the control signal word line (WL) is enabled, the pass-gate transistors are turned on and then the storage nodes (LN and RN) are connected to the vertically running bit lines (BL and NBL). That is, these transistors allow access to the cell for read and write operations, acting as bidirectional transmission gates.

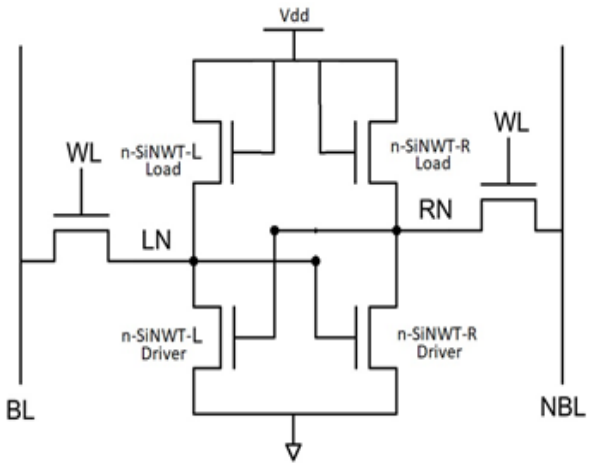

Fig. 1 – The circuit diagram of the NMOS SRAM bit cell

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2. METHODOLOGY

In this research, a new model discussed in [21] has been used to investigate the static characteristics of an *n*-SiNWT NMOS SRAM bit cell. The designed MATLAB program has been used to calculate the working points of the load and driver *n*-SiNWTs that are connected as NMOS cross-coupled logic inverters in SRAM. The MATLAB program also calculates the butterfly and I_d-V_d characteristics of the SRAM bit cell based on the individual output characteristics of each load and driver SiNWTs [21]. The MuGFET tool [22, 23] has been used to produce the output characteristics of each transistor individually. These characteristics are then implemented in the MATLAB program to produce the final static butterfly and current characteristics of a 6T SRAM bit cell [21].

The ratio of nanowires of driver to load SiNWTs has been chosen to make the SRAM bit cell work in the best possible conditions. The nanowire ratio (K_D/K_L) is the driver to load transistors (where K is the number of nanowires). The constant parameters illustrated in Table 1 have been used to study the effect of nanowire ratio on the SRAM characteristics.

In this research, the optimization of K_D/K_L will strongly depend on the improvement of the noise margins (NMs) of the butterfly characteristics by increasing the drain current (I_{ds}) of the driver transistor. Also, the optimization will depend on whether NMs are equal and high, and the inflection voltage (V_{inf}) is near to $V_{dd}/2$ values as possible. So, these parameters under such conditions are used as limiting factors. The best inverter has (as possible) equally low NM_L and high NM_H values. Both NM_L and NM_H must have high values, and the V_{inf} must be close to the $V_{dd}/2$ value.

Table 1 – SiNWT parameters used in this study

Parameter	Value
Length of channel	30 nm
Length of source	10 nm
Length of drain	10 nm
Diameter of channel	20 nm
Thickness of insulator SiO_2	2 nm
Concentration of channel	$1 \cdot 10^{10}$/cm^3 (*p*-type)
Concentration of source and drain	$1 \cdot 10^{20}$/cm^3 (*n*-type)

3. RESULTS AND DISCUSSION

The butterfly characteristics of a 6T (*n*-channel SiNWT) NMOS SRAM bit cell with different K_D/K_L are illustrated in Fig. 2, where $K_D/K_L = 3, 5, 7, \ldots, 21$ and $V_{dd} = 1$ V. From Fig. 2, it is clear that a decrease in the inflection point with increasing driver to load nanowire ratio (K_D/K_L) can occur due to an increase in nanowires in driver SiNWT. According to Fig. 2, the increase in K_D/K_L results in an increase in both noise margins NM_L and NM_H but without reaching the optimized value $V_{dd}/2$ (0.5 V). NM_H and NM_L are the high- and low-state NMs, respectively. Fig. 3 shows the current characteristics of a 6T (*n*-channel SiNWT) NMOS SRAM bit cell with different K_D/K_L, where K_D/K_L varies from 3 to 21 with a step of 2 and $V_{dd} = 1$ V. From Fig. 3, the current increases at the inflection point with increasing K_D/K_L.

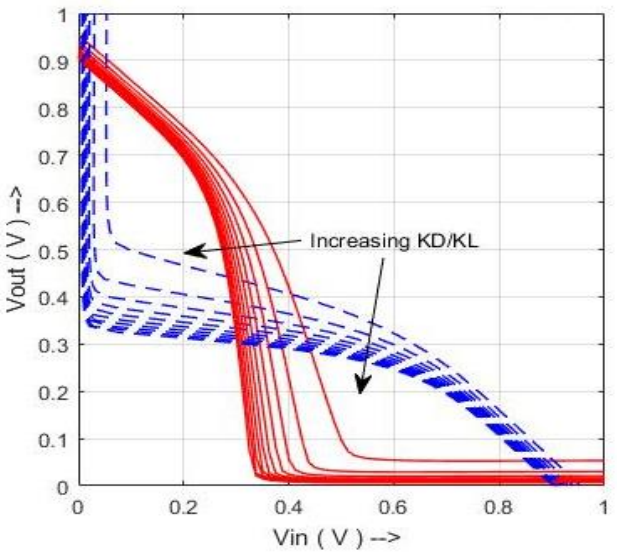

Fig. 2 – The butterfly characteristics of 6T (*n*-channel SiNWT) NMOS SRAM bit cell with different K_D/K_L and $V_{dd} = 1$ V

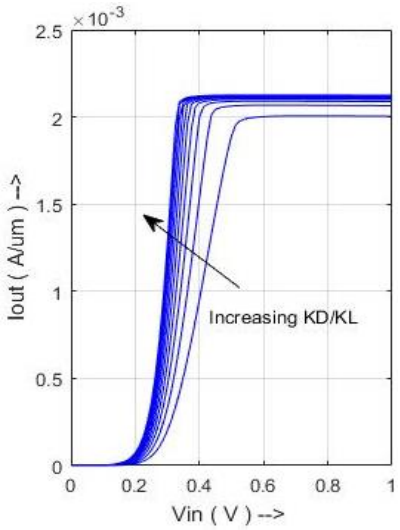

Fig. 3 – The current characteristics of 6T (*n*-channel SiNWT) NMOS SRAM bit cell with different K_D/K_L and $V_{dd} = 1$ V

Fig. 4 illustrates the variation of NM_L, NM_H and V_{inf} with increasing K_D/K_L. As shown in Fig. 4, $V_{dd} = 1$ V has an optimization point in which NM_H and V_{inf} curves intersect, and NM_L can be closer to the $V_{dd}/2$ line. Moreover, Fig. 4 illustrates that NM_L and NM_H have better values at $K_D/K_L = 4$.

According to Fig. 4, the increase in K_D/K_L leads to an increase in NM_L up to $K_D/K_L = 4$, while $NM_L = 0.12$ V at this point, and then decreases slightly, and NM_H continuously increases exponentially with increasing K_D/K_L value. NM_H and NM_L are the high- and low-state NMs, respectively. Then the best value (depending on NMs curves) of K_D/K_L will be 4 at an acceptable value of $NM_L = 0.12$ V and an excellent value of $NM_H = 0.3$ V and inflection voltage $V_{inf} = 0.331$ V, because these values are very close to reaching the optimized value of 0.5 V.

Fig. 5 illustrates the normalized value of NM_L to $V_{dd}/2$ with K_D/K_L value. According to this curve, the optimized critical value of K_D/K_L is 4 at 12.5 % of $V_{dd}/2$,

while at $K_D/K_L = 5$ it decreases to 12.1 % and decreases to 9.4 % at $K_D/K_L = 19$. This means that it is possible to use 4 as an optimized value according to NMs as limitation parameters.

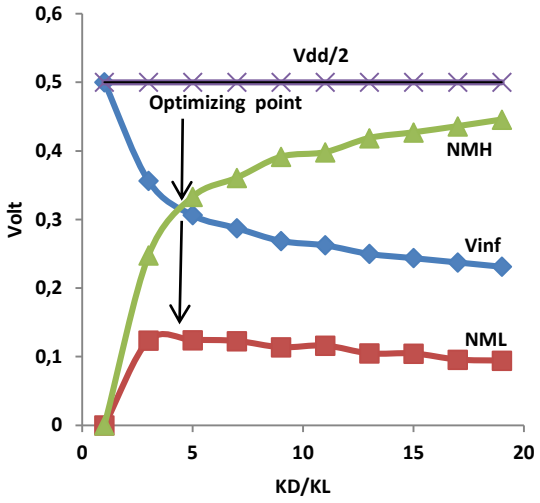

Fig. 4 – Variation of NM_L, NM_H and V_{inf} with increasing K_D/K_L

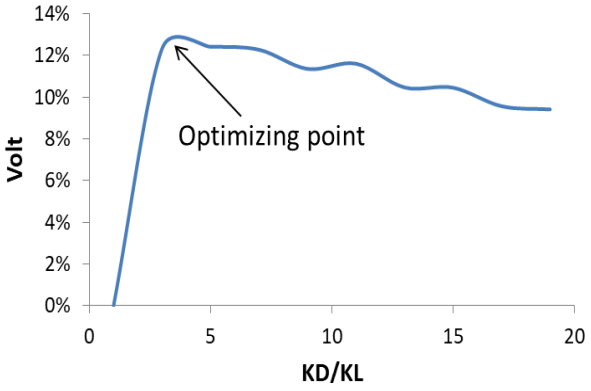

Fig. 5 – Normalized value of NM_L to $V_{dd}/2$ with K_D/K_L

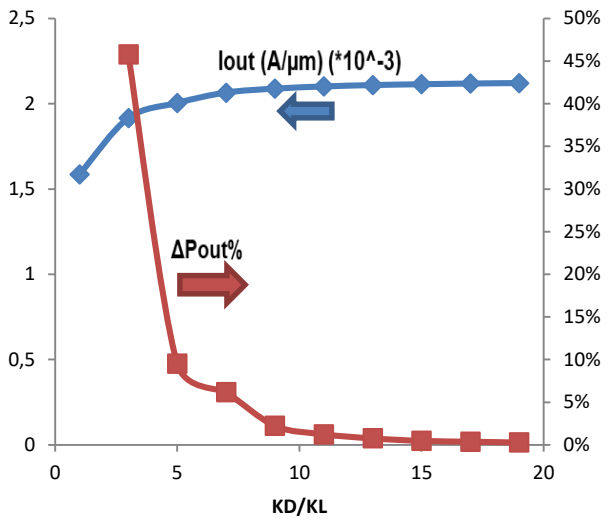

Fig. 6 – The output current (I_{out}) and percentage increment of static power consumption (ΔP %)

Fig. 6 shows the current I_{ds} and percentage increment of static power consumption (ΔP %) in SRAM cell characteristics. Current characteristics increase with increasing K_D/K_L, while the percentage increment of static power consumption decreases with increasing K_D/K_L. According to Fig. 6, it is clear that ΔP % at $K_D/K_L = 4$ is half the power at $K_D/K_L = 3$, so the optimal K_D/K_L value must be 4 depending on both NMs and ΔP % in the SRAM cell.

4. CONCLUSIONS

This study optimizes the nanowire ratio of driver to load (K_D/K_L) of the SiNWT 6T SRAM cell. The limiting factors of this optimization are NMs and an inflection voltage of butterfly characteristics with power consumption of the 6T SRAM cell. The results indicate that the optimized value of K_D/K_L ratio is 4. The increase in K_D/K_L leads to a continuous increase in NM_H, acceptable NM_L and low percentage increment of static power consumption (ΔP %) at $K_D/K_L = 4$.

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Оптимізація 6T бітової комірки із SRAM на основі співвідношення нанодротів SiNWT

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У сучасних технологіях первинною структурою пам'яті, яка широко використовується у багатьох додатках цифрових схем, є 6T бітова комірка із статичною оперативною пам'яттю (SRAM). Основною причиною мінімізації бітової комірки пам'яті до нанорозмірів є забезпечення інтегральних мікросхем SRAM найбільш можливим обсягом пам'яті на одну мікросхему, а основною частиною 6T бітової комірки із SRAM є MOSFET. Однією з нових структур MOSFET, які долають звичайні проблеми структури MOSFET при мінімізації до нанорозмірів, є кремнієвий нанодротовий транзистор (SiNWT). Це дослідження є першим, що вивчає та оптимізує співвідношення нанодротів драйвера та навантаження (K_D/K_L) для шести n-канальної бітової комірки із SRAM на основі SiNWT. Засіб моделювання MuGFET був використаний для розрахунку вихідних характеристик кожного транзистора окремо, а потім ці характеристики були реалізовані в програмному забезпеченні MATLAB для отримання кінцевих статичних характеристик 6T бітової комірки із SRAM. Обговорено оптимізацію співвідношення нанодротів драйвера та навантаження нанорозмірної бітової комірки із SRAM на основі SiNWT n типу. У роботі оптимізація співвідношення K_D/K_L буде сильно залежати від напруги перегину та високих і низьких допустимих рівнів шумів (NMs) характеристик. Покращення NMs характеристик було здійснено за рахунок збільшення струму стоку (I_{ds}) драйверного транзистора. Крім того, оптимізація в принципі буде залежати від того, чи є NMs рівними та високими, а напруга перегину (V_{inf}) наближається до значень $V_{dd}/2$, наскільки це можливо. Ці принципи використовувались як обмежувальні фактори для оптимізації. Результати показують, що оптимізація сильно залежить від співвідношення нанодротів, а найкращим співвідношенням було виявлено $K_D/K_L = 4$. Збільшення K_D/K_L призводить до постійного збільшення NM_H, прийнятного NM_L та низького процентного приросту споживання статичної енергії (ΔP %) при $K_D/K_L = 4$.

Ключові слова: MS Word, SRAM, SiNWT, Нанодріт, N-MOS, Комірка пам'яті.