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Investigation of Carbon Nanotube FET with Coaxial Geometry

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This paper aims to study the behavior of a Carbon Nanotube Field Effect Transistor (CNTFET) which is one of the nanoelectronic devices and a major replacement for Complementary Metal Oxide Semiconductor (CMOS) and MOSFETs, which have a wide range of short channel effects that play a prominent role in their disadvantages and, thus, have made us today to look for a better device. One such device is CNTFET which is better in terms of execution with low power consumption, faster switching speed, high carrier mobility, and very large scale integrated circuits. The channel of this transistor is surrounded by a carbon nanotube, and this paper mainly revolves around the simulation of its current-voltage (*I-V*) characteristics. The efficiency of this device on the whole depends on device parameters that are shown in the simulation of CNTFET, and the geometry of this device has an excellent dominance on carrier transport and permits for superior electrostatics while the gate contact wraps throughout the channel of a carbon nanotube. A carbon nanotube used for coaxial geometry has a zigzag structure and is semiconducting in nature. To ensure the efficient execution of CNTFETs as a vital part of nanoelectronic devices, chirality factor (n, m) values play an important role whose effect is shown on drain current. Further, the source/drain doping level variations that affect drain current are inspected. Also, *I-V* characteristics at different temperature conditions are examined which indirectly gives us an idea of the movement of electrons in this device with respect to change in temperature. Additionally, the analysis is also made to see the effect of nanotube length, coaxial gate voltage and gate thickness on *I-V* characteristics and also to reveal the impact of high-k materials on *I-V* characteristics.

Keywords: Carbon nanotube, CNTFETs, Coaxial, *I-V* characteristics, Semiconducting.

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1. INTRODUCTION

The miniaturization of the electronic devices over the past decade has played a major role in the electronic industry. Every stage of miniaturization results in a device which has better speed, reduced power dissipation, reduced costs, and a large number of gates on a chip [1, 2]. This has been in effect due to the famous Moor's law. It states that the number of transistors in an integrated circuit is doubled in every two years [3-7]. This integration of large numbers of metal oxide semiconductor (MOS) transistors into a small chip resulted in faster and less expensive circuits. Although a MOS field effect transistor (MOSFET) has the added advantage of increased reliability, consumes less power and is also capable of being packed in large numbers within a single integrated circuit (IC) because of small size, it brought forth many drawbacks like short channel effects, high leakage current and reliability issues [5-8]. As the size becomes smaller, scaling the silicon MOSFET becomes harder. The limiting factors are short channel effects, ballistic transport, tunneling effect [2]. Various leakage current operations such as weak inversion current, reverse-bias *p-n* junction current and drain induced barrier lowering (DIBL) current have been observed in MOSFETs [9, 10]. These drawbacks have encouraged the use of high-performance channel material and mobility enhancement technology. Hence, to have unique semiconductors as the channel material which enhances both mobility and electrostatics at every stage is the solution [11-14]. After evaluations of all possible emerging devices, researchers from the industry have suggested the use of carbon-based nanoelectronics, especially carbon nanotubes (CNTs) and graphene. Among the various qualities of CNTs and graphene, few major reasons to use CNTs and graphene are their excellent performance properties such as very little short channel effects, increased mobility, and adjustable drive currents [15].

Carbon being the most prevalent element in our universe forms various allotropes. Among the various allotropes of carbon, CNTs have shown distinguishable properties such as ballistic transport, mechanical stability and dynamic load. Carbon in CNTs has configuration of sp^2 and is bonded with strong molecular forces. The nanotube in CNTs is held together via Van der Waals forces, thereby developing high energy, low-weight materials that possess conductive electrical and thermal qualities [16, 17]. Semiconducting CNTs have attributes such as outstanding carrier mobility, higher mean free path and better electrostatics because of their non-planar structure. They also manifest ballistic transport over several hundred nanometers in length. Hence, CNTs are able to overpower the short channel effects in conventional transistors. CNTs are very appealing for nanoelectronic applications and can be further used to achieve higher speed ballistic carbon nanotube field effect transistors (CNTFETs). Hence, CNTs can be one of the exemplary replacements of silicon in conventional transistors.

CNTFETs are FETs that use a carbon nanotube as their channel instead of silicon which is one of the major differences between a CNTFET and a MOSFET.

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This increases drive current density in CNTFET and current carrier mobility as compared to MOSFETs. It has been suggested that high-k materials are of utmost significance for the upcoming transistors because they help in reducing power dissipation and leakage currents. CNTFETs with high-k materials can be operated in a ballistic range. This leads us to superfast devices because high-k dielectrics and ballistic electron transport help to improvise a current which is in direct proportion to the transistor speed [18].

2. MATERIALS AND METHODS

2.1 Simulation Setup

This section explains the methodology and the steps involved in simulation and the parameters varied to examine the current-voltage characteristics of CNTFET. The simulation of CNTFET was carried out using NANOHUB CNTFET LAB tool and MATLAB tool was used for plotting graphs. NANOHUB CNTFET tool revolves around 3D CNTFET devices and simulates ballistic transport properties. The NANOHUB CNTFET tool involves six steps which are as follows:

- **Device Settings.** This is the very first step in simulation which allows to modify nanotube length, chirality of the nanotube, geometry of the environment (planar/coaxial), source/drain doping, body doping and whether to include doping similar to MOSFET.
- **Planar/Coaxial Exterior Settings.** In this step, according to the geometry of the environment, the parameters can be varied with respect to their structures such as gate length, oxide thickness, dielectric of the gate insulator, gate thickness.
- **Boundary Settings.** This step involves making selection of boundary conditions for electrostatics. Hence, we can choose either Dirichlet or Neumann as our boundary conditions. When choosing the Dirichlet condition, the contacts will be treated as a Schottky barrier. When choosing the Neumann condition, the contacts are treated MOS-like. For simulation point of view, Neumann boundary condition is always preferred.
- **Environment Settings.** This setting allows us to choose the temperature and drain, source and gate voltages.
- **Simulator Settings.** This setting allows us to choose simulation method, simulation examples, holes consideration, maximum iterations allowed, etc.
- **Simulation.** This is the final step of the NANOHUB CNTFET tool where plots for various electrical parameters of the device are displayed.

2.2 Device Structure

The C–C bond length is 0.144 nm which is the default value. The green color atoms indicate the carbon atoms in sp^2 hybridization. The chirality of the CNT is determined by the value of (n, m). To make the nanotube semiconducting in nature, the value of (n, m) should not be an integer multiple of 3. The values $n = 13$ and $m = 0$ imply that the nanotube is semiconducting and has a zigzag structure. For metallic CNTs, the value of n can be 12.

The nanotube length is the length of the central CNT. The CNT active region is chosen to be doped which implies that the source and drain region in the CNTFET resembles that of a MOSFET. Source/drain doping region length gives an insight of the region inside the nanotube where we want to impose high doping. This region length is generally taken as 0.2 times of the nanotube length. Here our emphasis is on coaxial geometry. Fig. 1 shows that the gate is symmetrically placed with respect to the CNT. The value of the gate length can vary from zero to the maximum value of the device length. In case of overlap, the value of the gate contact is less than the CNT length.

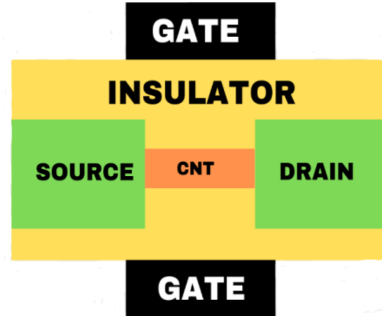

Fig. 1 – Front view of the coaxial CNTFET

Table 1 – Parameters of the coaxial CNTFET

S. No.	Parameter	Symbol	Values
1.	C–C bond length	a_0	0.144 nm
2.	Chirality	(n, m)	(13, 0)
3.	Nanotube length	L_C	5 nm
4.	S/D doping region length	$L_{S/D}$	2.5 nm
5.	Source/drain doping	$N_{S/D}$	1×10^8/m
6.	Gate length	L_G	8 nm
7.	Gate thickness	t_{GATE}	2 nm
8.	Gate insulator thickness	t_{ox}	4 nm
9.	Source/drain contact radius	r_c	1 nm
10.	Dielectric constant of nanotube interior	ε_{air}	1.0
11.	Dielectric constant of gate insulator	ε_{ox}	16.0
12.	Gate contact-CNT work function difference	ϕ_G	0.41 eV
13.	Source contact-CNT work function difference	ϕ_S	0.41 eV
14.	Drain contact-CNT work function difference	ϕ_D	0.41 eV
15.	Temperature	T	300 K
16.	Coaxial gate voltage	V_G	0.4 V
17.	Drain voltage	V_D	0.4 V

If it exceeds the CNT length, then it overlaps the source/drain contacts. The nanotube interior is filled with vacuum. Hence, the dielectric constant value chosen is 1. The dielectric constant of gate insulator can vary and CNTFET allows us to choose a wide range of high-k materials as insulators. Source and drain boundary conditions are chosen to be Neumann instead of Dirichlet. In case of the Neumann boundary conditions, the default value of the work function difference is half of the band gap value of semiconducting CNTFET

which is equal to 0.41 eV. The ambient temperature considered is 300 K. The NANOHUB CNTFET LAB and MATLAB are used for simulation and plotting electrical parameters, respectively. The CNTFET LAB simulates ballistic transport properties of the CNTFET devices [19] and was used to get the simulation results for our proposed device structure. Table 1 lists down the various parameters and their default values.

3. RESULTS AND DISCUSSION

Fig. 2 shows the plot of *I-V* characteristics for different values of coaxial gate voltage (V_G) by plotting drain current (I_D) in amperes along the *Y*-axis and drain voltage (V_D) in volts along the *X*-axis. The voltage is varied in steps of 0.05V. The nanotube length is kept constant as 5 nm. From Fig. 2 we observe that drain current increases as the gate voltage is increased from 0.2 V to 1.0 V. For V_G equal to 0.2 V, the value of I_D starts saturating from 0.05 V (drain voltage) till 0.4 V and reaches a maximum value of 0.4 μA. As the coaxial gate voltage is increased to 0.4 V, the drain current saturates from nearly 0.15 V till 0.4 V and reaches a maximum value of 3.86 μA. For V_G equal to 0.6 V, I_D saturates from nearly 0.25 V (V_D) and the saturation current is 12.7 μA. For V_G equal to 0.8 V, the drain current saturates nearly at 0.3 V and reaches a value of 21.9 μA. Finally, at coaxial gate voltage equal to 1.0 V, the drain current begins to saturate from 0.35 V and reaches a value of 30.6 μA.

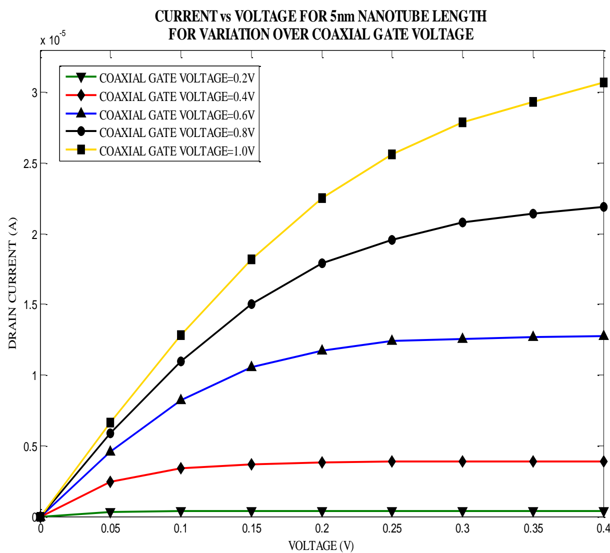

Fig. 2 – I_D vs. V_D plot for variation over coaxial gate voltage

Fig. 3 shows the plot of *I-V* characteristics for different values of dielectric constant of gate insulator by plotting drain current (I_D) in amperes along the *Y*-axis and drain voltage (V_D) in volts along the *X*-axis. The voltage is varied in steps of 0.05 V and current is in the range of 10^{-6} A. The nanotube length is kept constant as 5 nm. Hafnium dioxide (HfO_2) has a dielectric constant of 25 and silicon dioxide (SiO_2) has a dielectric constant of 3.9. From Fig. 3 we observe that drain current increases as we move towards high-k materials. For HfO_2, the drain current reaches a value of 3.88 μA for a drain voltage equal to 0.4 V. For SiO_2, the drain current reaches a value of 3.84 μA for a drain voltage equal to 0.4 V. For a dielectric having a value equal to 16, the drain current reaches a saturation value of 3.86 μA. For Al_2O_3 having a dielectric constant equal to 10, the *I*-V characteristic curve was found similar to that of SiO_2. For titanium dioxide (TiO_2) having a dielectric constant equal to 40, the *I-V* characteristic curve was the same as that of HfO_2.

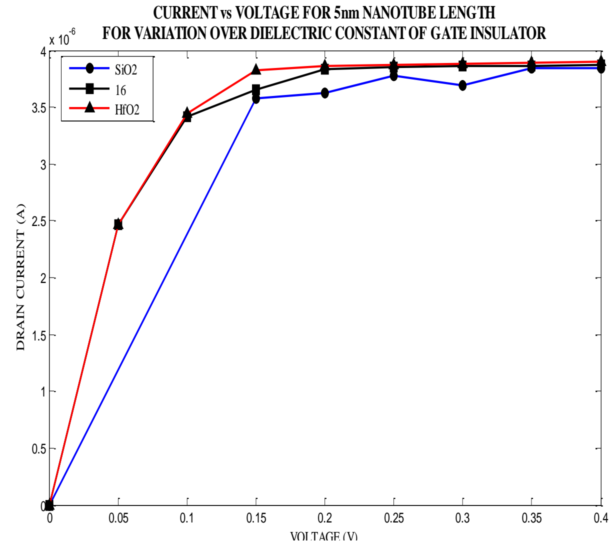

Fig. 3 – I_D vs. V_D plot for variation over dielectric constant of gate insulator

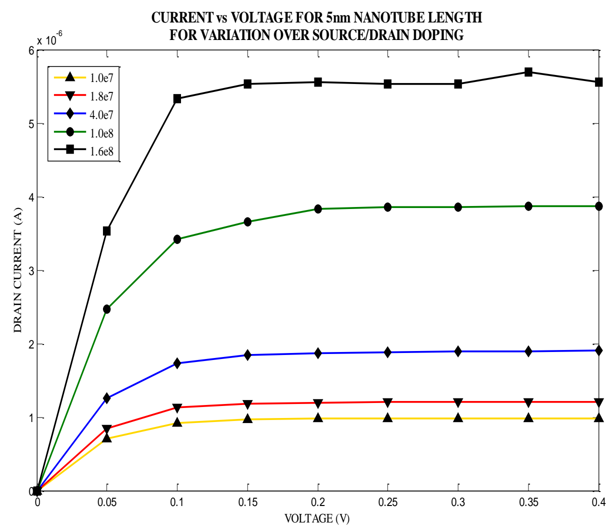

Fig. 4 – I_D vs. V_D plot for variation over source/drain doping

Fig. 4 shows the plot of *I-V* characteristics for different values of source/drain doping by plotting drain current (I_D) in amperes along the *Y*-axis and drain voltage (V_D) in volts along the *X*-axis. The voltage is varied in steps of 0.05 V and current is in the range of 10-6 A. The nanotube length is kept constant as 5 nm. From Fig. 4 we observe that drain current increases as the source or drain doping is increased exponentially. When the source/drain doping is 1.0e7, the drain current begins to saturate from 0.15 V and reaches a maximum value of 0.985 μA. For doping equal to 1.8e7, the value of I_D starts saturating from 0.2 V and reaches a maximum value of 1.21 μA. As the doping is increased

to 4.0e7, the drain current saturates from nearly 0.2 V and reaches a maximum value of 1.90 μA. For doping equal to 1.0e8, I_D saturates from nearly 0.25 V and the saturation current is 3.86 μA. When the doping is increased to 1.6e8, drain current begins to saturate from 0.25 V and reaches a value of 5.55 μA.

Fig. 5 shows the plot of gate thickness from 3 nm to 7 nm with a difference of 2 nm by plotting drain current (I_D) in amperes along the *Y*-axis and drain voltage (V_D) in volts along the *X*-axis. When the gate thickness is 3 nm we find a linear increment of drain current for variation of voltage up to 0.1 V and reach a value of 3.38 μA. Thereafter, the drain current does not increase linearly but increases slightly till the voltage reaches 0.2 V and begins to saturate from 0.25 V and attains value of 3.5 μA. When the gate thickness is increased to 5 nm, there is a decrease in the value of drain current. For a gate thickness equal to 5 nm, the drain current saturates at nearly 0.15 V and reaches a value of 2.5 μA.

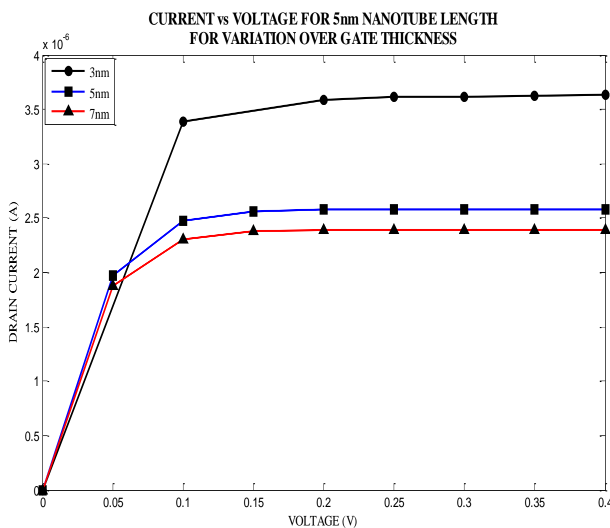

Fig. 5 – I_D vs. V_D plot for variation over gate thickness

For a gate thickness equal to 7 nm, the saturation current achieved is 2.3 μA. Hence, it can be inferred that for the increase in the gate thickness the drain current decreases.

The variation of chirality by keeping the nanotube length constant at 5 nm was also observed in such a way that mod (*n*, 3) is a non-zero value, where '*n*' represents the chirality center for a semiconducting CNT. We observe that as we increase the chirality center from 13 to 16, the saturation value of current decreases. Variation of the nanotube length (L_C) from 5 nm to 9 nm gives us the observation that drain current reduces as we increase the nanotube length. Hence, better *I*-*V* characteristics are observed for 5 nm nanotube length than in comparison to 7 nm and 9 nm. The temperature variation for 5 nm nanotube length was also considered for temperatures equal to 200 K (cold), 300 K (room temperature) and 400 K (hot). We observe an increase in the value of drain current as temperature is increased from 200 K to 400 K. Hence, the device gives efficient output.

4. CONCLUSIONS

In this study, the proposed device structure of a CNTFET is successfully simulated and the *I*-*V* characteristics of the device are formulated using NANOHUB. We can conclude that the device works effectively if the drain current values are excellent. To get these values of drain current we have used a CNTFET with the following conditions: short nanotube length, greater coaxial voltage, insulator with a high dielectric constant, high concentration of source/drain doping levels and minimum value of gate thickness. The results also reveal that the performance of the device is impeccable when operated at high temperatures and less chirality values. These results would play a major role during the process of fabrication of the devices which can then be used for a range of low power circuit applications such as processors, voltage converters and regulators, LCD displays, ASICs and FPGAs.

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Дослідження польових транзисторів на вуглецевих нанотрубках з коаксіальною геометрією

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Робота спрямована на вивчення поведінки польового транзистора на вуглецевих нанотрубках (CNTFET), який є одним з наноелектронних пристроїв та основною заміною комплементарних МОН структур (CMOS) та MOSFET, які мають широкий спектр короткоканальних ефектів, що відіграють помітну роль у їхніх недоліках і, таким чином, змусили нас шукати кращий пристрій. Одним з таких пристроїв є CNTFET, який краще з точки зору виконання з низьким енергоспоживанням, більш високою швидкістю перемикання, високою мобільністю носіїв та дуже великими інтегральними схемами. Канал такого транзистора складається з вуглецевої нанотрубки, і ця стаття в основному стосується моделювання її вольт-амперних (*I-V*) характеристик. Ефективність цього пристрою в цілому залежить від параметрів пристрою, які показані при моделюванні CNTFET, а геометрія пристрою має гарний вплив на транспортування носіїв та дозволяє покращити електростатику, в той час як контакт затвора охоплює весь канал вуглецевої нанотрубки. Вуглецева нанотрубка, що використовується для коаксіальної геометрії, має зигзагоподібну структуру і є напівпровідниковою за своєю природою. Для забезпечення ефективного виконання CNTFETs як життєво важливої частини наноелектронних пристроїв важливу роль відіграють значення коефіцієнта хіральності (n, m), вплив яких показано на струм стоку. Далі перевіряються зміни рівня легування джерела/стоку, які впливають на струм стоку. Також характеристики *I-V* досліджуються при різних температурних умовах, що побічно дає нам уявлення про рух електронів в цьому пристрої при зміні температури. Крім того, аналіз проводився для того, щоб побачити вплив довжини нанотрубки, напруги коаксіального затвора та товщини затвора на характеристики *I-V*, а також щоб виявити вплив high-k матеріалів на ці характеристики.

Ключові слова: Вуглецева нанотрубка, CNTFETs, Коаксіальний, Вольт-амперні характеристики, Напівпровідниковий.