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Simulation and Performance Analysis of a Triple-material Gate GAA SNSTFT

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A Stacked Nano Sheet Gate All Around Thin Film Transistor (SNS GAATFT) with Triple Material (TM) has been proposed in this paper. The TM of the Thin Film Transistor (TFT) is varied by applying three different work functions (WFs) by having different gate materials being used. The transistor considered here for implementation is a *p*-channel device. The analysis has been carried out using the physical model: temperature-dependent carrier transport model (DD). Mobility Model (MM) includes the effects of doping concentration and electric field, Bandgap Narrowing Model (BNM) and Shockley-Read-Hall recombination Model (SRM) are for carrier lifetime. Synopsys Sentaurus TCAD has been used for the simulation of the proposed model and thus analyzing its characteristics. The characteristics of the proposed TM have been compared to those of the previously proposed Single Material (SM) SNS GAATFT model. For the proposed model, the first and third WFs were kept constant while the WF of the middle region varied between the first and third WFs. The output characteristics analyzed proved a better result for WF values closest to the third WF. Thus, a higher value of the middle WF was used in determining the different characteristics. From the characteristics it can be analyzed that due to varying electric potentials on the gate terminal due to varying WF, the influence of high-speed moving electron is reduced from the source side, and this helps in improving the carrier transport efficiency and thus, it is clear, this, in turn, helps in lowering the hot carrier effects. The comparison result shows that drain current in a TM is found to be almost 4 times higher than that of a SM model which shows better improvement in I_{ON} current.

Keywords: Triple material (TM) gate, SNS GAATFT, Work function, Electric potential, Single material (SM) gate.

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1. INTRODUCTION

Cost reduction and functional enrichment of a smart phone plays a vital role in the market today. This means that numerous functions need to be embedded on a glass substrate of OLED display, and this is termed as System on Panel (SOP). Hence a TFT with better performance is favorable and to enhance transistor characteristics, a multi-gate transistor would be a better solution. There are many multi-gate structures, like gate all-around [1], with ultra-thin body channel [2, 3], tri-gate [4], which effectively enhance the gate control of the channel. These models help in the reduction of Short Channel Effect (SCE) and effects of leakage current. Among all other multi-gate structures, GAA is the best one to control the channels when it comes to stacking of nanosheet in TFT explained in [5]. Stacking of channels in the same structure will improve the drive current and performance of the device [6, 7]. In GAA, most of the devices having single material (SM) gate have an increased hot carrier effect on the drain side due to the increased electric field on the drain side.

Gate engineering is one of the promising solutions to reduce the hot carrier effect and thus increase the lifetime of the device. MOSFET device structures including TFT, FinFET, nanowires that employ gate material engineering [8] improve transport efficiency in the gate by adjusting the pattern of electric field and the surface potential along the channel, which results in improved carrier transport efficiency, better transconductance and also clampdown of SCEs. [9] explains the dual material gate in FET, which employs gate-material engineering, i.e. dual material in a single gate with different work functions (WFs) creating the step potential at the interface leading to better performance in carrier transport efficiency and reduced SCEs. The WFs for the materials are selected in such a way that the one near the source is of the maximum value and that near the drain is of the minimum value in the structure [10, 12] because of the consideration of the *n*-channel transistor. Having a higher WF beside the source leads to highly improved acceleration of carriers in the channel, while the lower WF beside the drain leads to reduction of the electric field peak near the drain side, thus reducing hot carrier effect. For an *n*-channel MOSFET in dual material gate engineering, WF for the first metal gate should be greater than that of the second metal gate. In case of a *p*-channel MOSFET, the second metal gate WF should be greater than that of the first metal gate.

To enhance the performance of a stacked nanosheet TFT, the advantages of triple material (TM) gate and GAA are incorporated in this paper. This structure comprises of three materials based gate electrode each having different WFs. This allows to increase the drain resistance and better control of the gate over conductance of the channel region, thus improving the gate transport efficiency. The rest of the paper comprises of the sections: Device Structure (2), Results and Discussion (3) and Conclusions (4).

2. DEVICE STRUCTURE

Fig. 1 illustrates the schematic view of the *p*-channel

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SM SNS GAATFT which is formed using the TCAD Simulation tool from the parameters that have been taken from experimental work [5]. In our previous work, the SM SNS GAATFT structure was validated and compared with different dielectrics. The result is shown in [13] and among the compared dielectrics HfO_2 produces a better performance and [14, 15] also supports this.

In Fig. 2, the SM gate is replaced by the TM gate, i.e. it is a TM SNS GAATFT. From the structure it is seen that the gate electrode consists of three different WFs (φ) based materials M1, M2 and M3 that are deposited over the lengths L1, L2 and L3, respectively, on the gate oxide layers. φM1, φM2, φM3 are the material WFs for the first, second and third gate, respectively, and it is chosen that $\varphi M1 < \varphi M2 < \varphi M3$ is the consideration for the *p*-channel transistor. The total length of the metal is L = L1 + L2 + L3, each having the same length of 333 nm. The gate material at the source end with the lowest WF [16] can be termed as the control gate. The material between the source and the drain with the next higher WF can be termed as the first screen gate, whereas the material at the drain end with the highest WF can be termed as the second screen gate. The device is composed of the first gate material with the WF WK1 = 4.4 eV (Ti), the second gate material with WK2 = 4.6 eV (Mo), and the third gate material with WK3 = 4.8 eV (Au) [17]. In the Synopsys Sentaurus TCAD, the device has been analyzed by employing a physical model, such as the DD model. The MM model was included for the effects of doping concentration and electric field, whereas the BNM and SRM models are for predicting the carrier lifetime [18]. The fabrication flow of SM SNS GAATFT has been explained in [5].

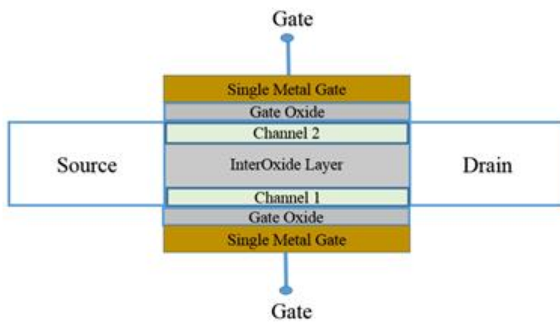

Fig. 1 – Schematic view of a SM SNS GAATFT

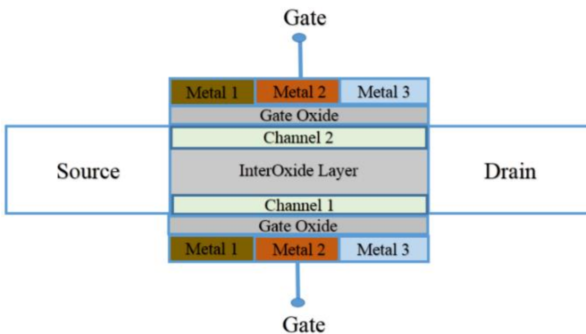

Fig. 2 – Schematic view of the proposed TM SNS GAATFT

3. RESULTS AND DISCUSSION

3.1 Electric Potential

Fig. 3 depicts the comparison of electric potentials of the SM gate (SMG) and TM gate (TMG). The values of $V_G = -0.3$ V and $V_D = -0.5$ V are considered for operation. In the SMG, it is noticed that the electric potential monotonically increases from the source to the drain, whereas there is an abrupt change near the transition of different gate materials in the TMG. It should be noticed that there are two drawbacks in the SM model. First, near the drain region the leakage current will be high due to the low negative potential causing the I_{OFF} current to increase. Second, with the monotonous electric potential, the carrier velocity and mobility will begin to decrease as the electrons move towards the drain from the source.

In case of the TM model, low electric potential in the M1 region is observed. From this it is understood that there is very little influence on the drain current after saturation with variations in V_D. This, in turn, helps to reduce the drain conductance and thus the impact of Drain-Induced Barrier Lowering (DIBL). In the saturation region, M3 absorbs additional V_D, and M1 is thus screened from the potential variations in the drain region where the M2 and M3 act as screening gates. Due to varying electric potentials, there is a reduction in the impact of high-speed moving electrons and, thus, the hot carrier effects are reduced and, in turn, the carrier transport efficiency improves.

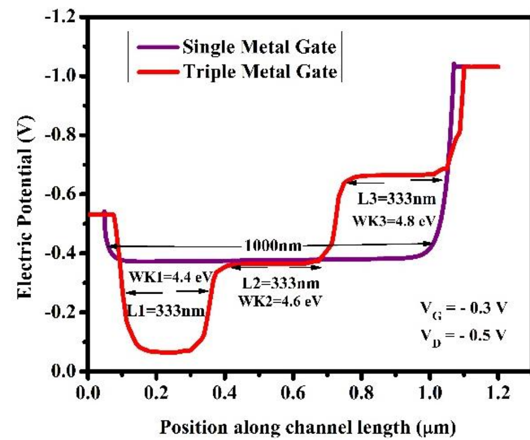

Fig. 3 – Electric potential variation for different channel lengths (μm) across the proposed TM and SM

3.2 Drain Current

Fig. 4 shows the output characteristics of the proposed TM model. The *p*-channel based transistor is applied with constant WFs WK1 and WK3 while varying WK2 from lower to higher value. The voltage is equal to the supply voltage V_{DD}, i.e., $V_G = -1$ V is applied on the gate terminal to observe the on-current (I_{ON}) of the transistor. It is observed that with the maximum WF of 4.9 eV, a higher I_{ON} of 22 μA is obtained in comparison to 7.5 μA at 4.6 eV.

Fig. 5 depicts the transfer characteristics of the *p*-channel transistor varying WF WK2 having constant $V_D = -1$ V. The characteristics obtained prove the behavior of a MOSFET, and little variation in the threshold voltage (V_T) in the saturation region can be observed. The maximum saturation current of 20 μA is also obtained as in the case of the output characteristics.

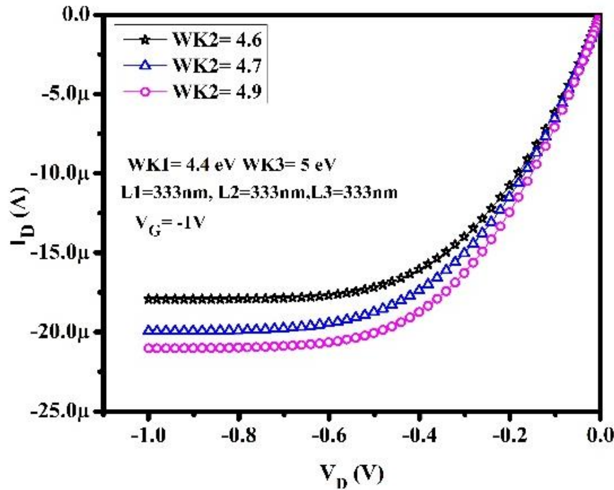

Fig. 4 – Output characteristics of the proposed TM model by varying WF WK2 keeping WK1 and WK3 constant at a constant $V_G = -1$ V

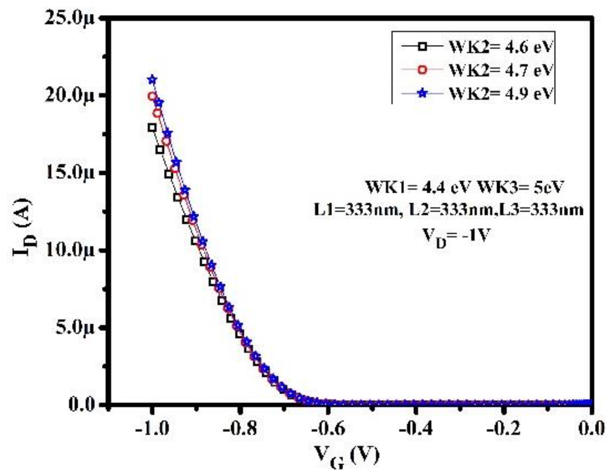

Fig. 5 – Transfer characteristics of the proposed TM model by varying WF WK2 keeping WK1 and WK3 constant at a constant $V_D = -1$ V

Fig. 6 shows the comparison of the output currents of a SM SNS GAATFT with respect to that of a TM SNS GAATFT. From the previous results for the M2, WK2 = 4.9 eV is being used due to higher I_{ON} current. As specified earlier, in the *p*-channel device the second screen gate (M3) has a higher WF compared to that of M1. We can thus infer from the comparison that the drain current in the TM is almost 4 times higher than that of the SM model.

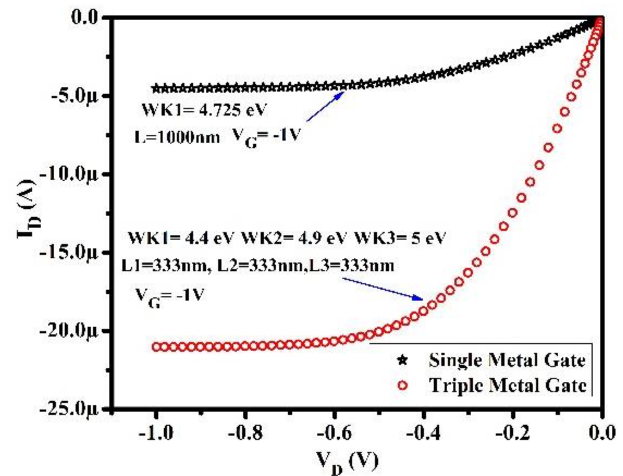

Fig. 6 – Comparison of drain currents of SMG and TMG with respect to varying drain voltage

4. CONCLUSIONS

In this paper, the simulation and performance analysis in terms of electric potential of a TM SNS GAATFT has been carried out in comparison to a SM SNS GAATFT. In the study, results prove to have better I_{ON}/I_{OFF} ratio which makes it suitable for low power applications like OLED displays.

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Моделювання та аналіз продуктивності транзисторів GAA SNSTFT із затвором з потрійним матеріалом

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У роботі запропоновано до розгляду транзистор SNS GAATFT з потрійним матеріалом (TM). TM тонкоплівкового транзистора (TFT) варіюється шляхом застосування трьох різних робіт виходу за рахунок використання різних матеріалів затворів. Транзистор, розглянутий у роботі, є *p*-канальним пристроєм. Аналіз проведено з використанням фізичної моделі – температурної залежності переносу носіїв заряду (DD). Модель мобільності (MM) включає ефекти концентрації легування та електричного поля, модель звуження забороненої зони (BNM) та модель рекомбінації Шоклі-Ріда-Холла (SRM) стосуються тривалості життя носія. Програмний продукт Synopsys Sentaurus TCAD був використаний для моделювання запропонованої моделі та аналізу її характеристик. Характеристики запропонованої моделі з TM були порівняні з характеристиками запропонованої раніше моделі SNS GAATFT з одинарним матеріалом (SM). Для запропонованої моделі перша та третя роботи виходу (WFs) підтримувались незмінними, тоді як WF середньої області варіювалася між першою та третьою WFs. Проаналізовані вихідні характеристики довели кращий результат для значень WF, найближчих до третьої WF. Таким чином, для визначення різних характеристик було використано більш високе значення середньої WF. З аналізу характеристик видно, що внаслідок різних електричних потенціалів на електроді затвору через різні WF, вплив швидкісного електрона, що рухається, зменшується з боку джерела, і це сприяє підвищенню ефективності переносу носіїв заряду і, отже, в свою чергу, допомагає зменшити ефекти гарячих носіїв. Результат порівняння показує, що струм стоку в моделі TM виявляється майже в 4 рази вищим, ніж в моделі SM, яка показує більше покращення струму I_{ON}.

Ключові слова: Затвор з потрійним матеріалом (TM), SNS GAATFT, Робота виходу, Електричний потенціал, Затвор з одинарним матеріалом (SM).