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Numerical Simulation of Field-effect Transistor with a Channel in the Form of a Nanowire

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The operation of the basic functional element of the integrated circuit – the field-effect transistor – is based on the drift of electrons and holes in the Si channel. With the use of stretching-compression of the crystal lattice of the Si substrate, by introducing impurity atoms, the mobility of carriers is somewhat reduced. At the same time, considerable interest to nanowires (NWs) based on Si (Ge) solid solution as elements for the formation of highly efficient channels of field-effect transistors necessitates studies of their structural, electrical and temperature characteristics. The paper presents the results of numerical simulation of coaxial Si-channel gate-all-around (GAA) FET structures. The structure of the *n*-type GAA NWFET and its volt-ampere characteristics were constructed using Silvaco TCAD tools. Within the framework of the diffusion-drift model of carrier transport, taking into account the Bohm quantum potential, effective operating parameters were obtained: permissible values of the threshold voltage, leakage current and I_{on}/I_{off} coefficient, and their dependences on temperature. It was obtained that the values of the threshold voltage V_t and subthreshold scattering SS remain almost unchanged with increasing temperature in the range from 280 to 400 K, which is primarily due to the additional influence of quantum effects for a given channel thickness and impurity concentrations. In addition, a typical decrease in the switch-on current by 45.5 % and leakage current by 46.4 % in a given temperature range was recorded. To assess the thermal stability of the studied transistor systems, the temperature coefficients β_{Vt}, β_{SS}, β_{Ion} and β_{Ioff} were calculated. Their values were respectively $8.63 \cdot 10^{-5}$; $-0.53 \cdot 10^{-5}$; $-3.87 \cdot 10^{-3}$ and $-3.80 \cdot 10^{-3}$ K^{-1}. The results of numerical simulations showed good agreement with the experimental data.

Keywords: GAA nanowire FET, Simulation, Temperature effects of electrical parameters.

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1. INTRODUCTION

The linear dimensions of complementary metal-oxide-semiconductor CMOS-devices with planar transistors decreased by 30% approximately every two years [1-4]. With the advent of transistors with a metal gate and high dielectric constant of the gate dielectric and other components, this pattern has become more complicated. After Field-effect transistors (FinFET) (see, for example, [3]) structures were introduced, the development of production technologies became much broader. FinFET in modern functional electronics are widely used in industrial, sensor [4] and medical equipment [5].

Of practical interest [1-4] is the formation of a transistor channel in which the distance between atoms is not equal to the crystal lattice parameter ($a_{Si} = 0.5431$ nm). They are primarily associated with the use of nanowires (NW) or nanotubes (NT) as channels for three-dimensional (3D) transistors [3, 10-13]. In addition, it is necessary to improve the performance of short-channel devices. An experimental problem is the experimental study of the microstructure and electrophysical properties of functional materials of nanoelectronics in the form of multicomponent and multilayer films [14-18].

Nanowires can be obtained by two methods: electrochemical deposition or the method of molecular beam epitaxy Ge on a Si substrate. When using the first method, the substances are deposited inside the porous membrane [6]. Transistor field structures with a built-in channel in the form of a nanowire can be formed by molecular beam epitaxy on a Si substrate by increasing the Ge layer or Si / Ge /… Si / Ge / S (S - substrate) layer structure. If a one-component nanowire with Ge is formed, the Ge and Si lattices will be conjugated. Solid solutions are formed in the contact area [7]. In layered molecular epitaxy, the entire two-component nanowire, which in the transistor field structure will act as a built-in controlled channel, can be formed us s.s. germanium atoms in silicon Ge (Si) and vice versa silicon atoms in germanium Si (Ge) depending on the atoms of individual components concentration [7, 8].

The aim of the work was to numerically model the structure and electrical parameters of the strained-Si GAA NWFET – a 3D *n*-type field-effect transistor with a strained-Si nanowire channel and a Gate-all-around (GAA).

2. NUMERICAL SIMULATION PROCEDURE

The structure of a strained-Si GAA NWFET was designed and investigated using Silvaco TCAD tools [15, 16]. The general cylindrical geometry was created using the corresponding mesh cylindrical three.d, where the cylindrical parameter specifies the radius, angle and *Z*-coordinates, and the three.d parameter creates a 3D grid [18, 19]. ATLAS [18] tools from Silvaco TCAD include both a diffusion-drift transport model and advanced quantum models. The current equations of the diffusion-drift model for electrons and

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holes have the following form [11]:

$$\boldsymbol{J_n} = qD_n \nabla n - qn\mu_n \nabla \psi - \mu_n n\left(kT\nabla\left(lnn_{ie}\right)\right), \quad (1.1)$$

$$\boldsymbol{J_p} = -qD_p \nabla p - qp\mu_p \nabla \omega + \mu_p p\left(kT\nabla\left(lnn_{ie}\right)\right), \quad (1.2)$$

where q is the electron charge, D_n and D_p are the diffusion coefficients for electrons and holes; n and p are the concentrations of electrons and holes; μ_n and μ_p are the mobilities of electrons and holes; ψ is the wave function; k is the Boltzmann constant; T is the Debye temperature; n_{ie} is the effective internal concentration.

In the nanowire channel, the carriers are limited in one direction. This affects the radial density of charges as well as the density of states. Quantum effects can be modeled in the Self-Consistent Coupled Schrödinger-Poisson Model, but it cannot solve transport problems on its own. Therefore, the latter is used in combination with the Drift-Diffusion Mode-Space Method or the Mode Space Non-Equilibrium Green's Function Approach. To model the electrophysical properties of NW devices, the Schrödinger equation in cylindrical coordinates is solved [18]. Along with this, quantum effects are included in ATLAS by changing the equations of transport models. In particular, the Bohm quantum potential (BQP) can be considered. In this case, the current equations (1.1) and (1.2) will have the form [11, 19]:

$$\boldsymbol{J_n} = qD_n \nabla n - qn\mu_n \nabla\left(\psi - Q\right) - \mu_n n\left(kT\nabla\left(lnn_{ie}\right)\right), \quad (1.3)$$

$$\boldsymbol{J_p} = -qD_p \nabla p - qp\mu_p \nabla\left(\psi - Q\right) + \mu_p p\left(kT\nabla\left(lnn_{ie}\right)\right). \quad (1.4)$$

In equations (1.3) and (1.4), the additional term Q represents the BQP, which is defined as [8, 16]

$$Q = -\frac{\hbar^2}{2}\frac{\gamma\nabla\left[M^{-1}\nabla\left(n^{\alpha}\right)\right]}{n^{\alpha}}, \quad (1.5)$$

where $\hbar$ is the Planck's constant, M is the effective mass, n is the concentration (electrons/holes), γ and α are the fitting parameters.

The BQP model has a number of features and advantages over other modeling approaches. The value of the fitting parameters γ and α is determined by the quantum constraint condition. As an example in [11, 19], the values of γ and α were 1.4 and 0.3, respectively.

Features of charge transport were modeled using operators models fermi ni.fermi cvt srh bqp.n. The fermi parameter allows to take into account the drift-diffusion charge transport within the framework of Fermi-Dirac statistics, cvt parameter – features of the inversion layer mobility, srh – Shockley-Read-Hall recombination mechanisms, bqp.n – BQP for electrons [18].

3. DEVICE STRUCTURE

The results of numerical simulation of the structure of a strained-Si GAA NWFET are presented in this part of the work.

We designed a 3D transistor with a strained-Si nanowire channel. Input data for modeling all materials are taken from Silvaco TCAD libraries [18]. The polysilicon gate was separated from the channel by insulating layers of HfO_2 and SiO_2, Al was used as the material for leakage and source electrodes, which are located at the ends (Fig. 1a). The strained-Si channel had the shape of a cylindrical tube with a length of 80 nm (Fig. 1b).

The geometric dimensions of the elements of the field-effect transistor are shown in Fig. 2. The diameter

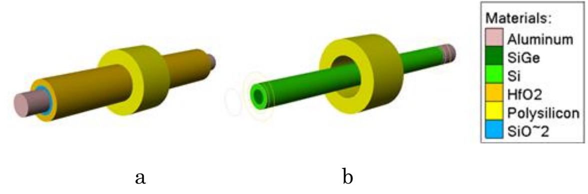

Fig. 1 – 3D structure of a strained-Si GAA NWFET (a) and separate display of its channel and gate (b)

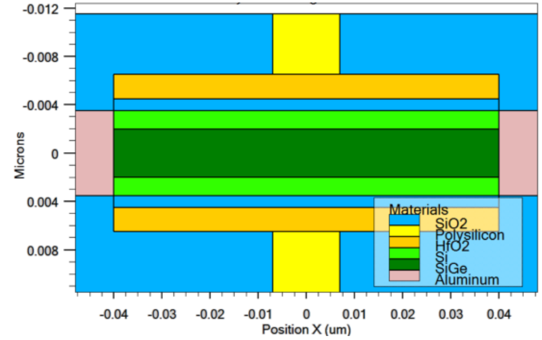

Fig. 2 – 2D structure of a strained-Si GAA NWFET with display of individual areas

and length of the s.s. Si(Ge) orientation rod were 4 nm and 80 nm, respectively, and the length of the polysilicon gate was 14 nm. The effective work function of selectrons from the gate electrode was 4.75 eV [16]. HfO_2 (k = 22) of 2 nm thick was used as the high-k dielectric, and the SiO_2 barrier layer under the high-k dielectric was 1 nm thick.

Fig. 3a shows typical 3D sections of the structure of a 3D transistor, for which numerical simulation of electrical parameters was performed, taking into account the short-channel effects (SCEs).

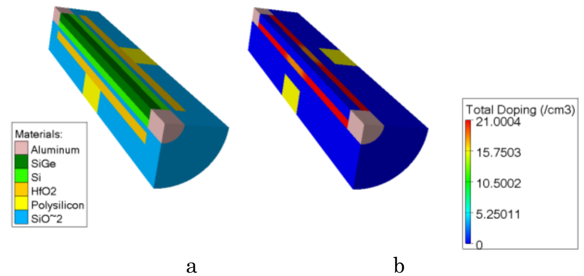

Fig. 3 – 3D slices in the structure of a strained-Si GAA NWFET with reflection of separate areas (a) and concentration distribution of impurity in the channel (b)

The concentration distribution of the donor impurity in the transistor channel is shown in Fig. 3b. The following configuration of channel doping profiles was used in the design: in the channel volume, the concentration of the acceptor impurity was 10^{18} cm^{-3}; a donor impurity with a higher concentration equal to 10^{21} cm^{-3} was introduced into the contact areas of leakage and source.

An analysis of the electrical parameters of the

transistor structures designed by us obtained on the basis of volt-ampere characteristics at different temperatures is given in the next section.

4. SIMULATION AND RESULTS

Typical dependences of the current leakage-source I_{DS} versus gate voltage V_{GS} at temperatures of 280, 300, 340, 360, 380 and 400 K for *n*-type GAA SiNWFET at fixed voltage values $V_{DS} = 0.20$ and 0.07 V are shown in Fig. 4.

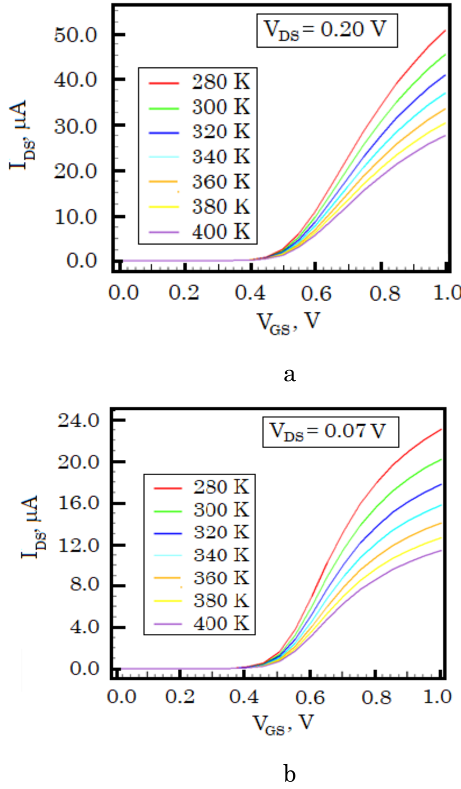

Fig. 4 – I_{DS}-V_{GS} curves of a strained-Si *n*-type GAA NWFET as a function of temperature variation and fixed values of the drain-source voltage 0.20 V (a), 0.07 V (b). The arrow direction indicates an increase in temperature

As an example, Fig. 5 shows typical I_{DS}-V_{DS} characteristics for a 3D *n*-type transistor at fixed gate voltage $V_{GS} = 1.0$ V. Using the ATLAS simulator, the main electrical parameters were determined: threshold voltage V_t, subthreshold scattering SS, switch-on current I_{on}, leakage current I_{off} and I_{on}/I_{off} coefficient (Table 1).

Table 1 – The parameters used for a strained-Si GAA NWFET as a function of working temperature

Parameters	Working temperature, K						
	280	300	320	340	360	380	400
V_t, mV	461.81	462.79	463.68	464.50	465.25	465.95	466.59
SS, mV/decade	95.01	95.00	94.99	94.98	94.97	94.96	94.95
$I_{off}\times10^{12}$, A	9.03	8.09	7.27	6.55	5.91	5.34	4.84
$I_{on}\times10^{5}$, A	5.05	4.53	4.08	3.67	3.33	3.02	2.75
$(I_{on}/I_{off})\times10^{-5}$	56.92	55.99	56.12	56.03	56.34	56.55	56.81

The following equations can be used to determine the temperature coefficients of the basic electrical parameters of FETs: based on the temperature dependences of V_t and SS, their themperature coefficients can be calculated, respectively, based on the ratios

$$\beta_{V_t} = \frac{V_t(\mathrm{T}) - V_t(300)}{V_t(300)(T-300)} \qquad (4.1)$$

and

$$\beta_{SS} = \frac{SS(\mathrm{T}) - SS(300)}{SS(300)(T-300)}. \qquad (4.2)$$

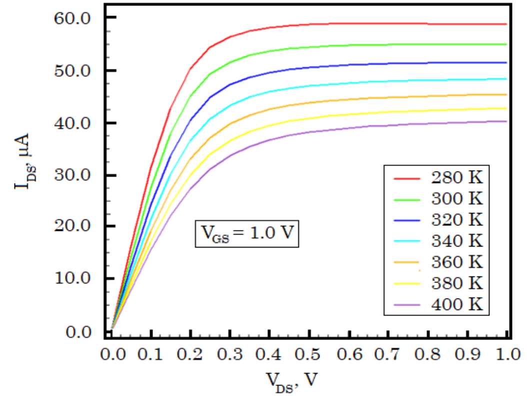

Fig. 5 – I_{DS}-V_{DS} characteristics of a strained-Si *n*-type GAA NWFET

The thermal coefficients of the filling factor switch-on current I_{on} and leakage current I_{off} can also be determined by the appropriate ratios:

$$\beta_{I_{on}} = \frac{I_{on}(T) - I_{on}(300)}{I_{on}(300)(T-300)} \qquad (4.3)$$

and

$$\beta_{I_{off}} = \frac{I_{off}(T) - I_{off}(300)}{I_{off}(300)(T-300)}. \qquad (4.4)$$

Based on equations (4.1)-(4.4), in the temperature range from 280 to 400 K, the temperature coefficients β_{Vt}, β_{SS}, β_{Ion} and β_{Ioff} are, respectively, $8.63\cdot10^{-5}$; $-0.53\cdot10^{-5}$; $-3.87\cdot10^{-3}$ and $-3.80\cdot10^{-3}$ K^{-1}.

The obtained data on the values of the temperature coefficients agree well with the experimental data for transistors based on strained-Si [1-4, 20]. It should be noted that the temperature dependences of the values of the switch-on current I_{on} and the leakage current I_{off} are typical for FETs [1-4. 13]. However, there is practically no variation between the threshold voltage V_t and the subthreshold scattering SS with increasing temperature. This is consistent with the results obtained in [21] and is associated with a significant effect of quantum effects at Si channel thicknesses less than 5 nm and impurity concentrations greater than 10^{18} cm^{-3}.

5. CONCLUSIONS

1. The influence of temperature in the range from 280 to 400 K on the volt-ampere characteristics and electrical parameters of the 3D transistor structure of a strained-Si *n*-type GAA NWFET is investigated.

2. The calculated correlations for estimating the temperature coefficients β_{Vt}, β_{SS}, β_{Ion} and β_{Ioff} are proposed, and their obtained values show good agreement with the experimental data.
3. The designed 3D structures in the framework of the diffusion-drift transport model taking into account the BQP demonstrate the allowable values of the electrical parameters such as threshold voltage V_t, subthreshold scattering SS, leakage current I_{off} and I_{on}/I_{off} coefficient. For this reason, the results can be used to further investigate the GAA NWFETs.

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Чисельне моделювання польового транзистора з каналом у вигляді нанодроту

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Робота базового функціонального елемента інтегральної схеми – польового транзистора заснована на дрейфі електронів та дірок у каналі. Із застосуванням розтягування-здавлювання кристалічної решітки кремнію Si, шляхом впровадження домішкових атомів, дещо зростає рухливість носіїв. Разом з цим значний інтерес до нанодротів на основі твердого розчину Si(Ge) як елементів для формування високоефективних каналів польових транзисторів обумовлює необхідність досліджень їх структурних, електричних та температурних характеристик. У роботі наведені результати числового моделювання коаксіальних Si-канальних транзисторних FET's структур із затвором Gate-all-around (GAA). Структура транзистора *n*-типу GAA NW FET та його вольт-амперні характеристики були побудовані з використанням інструментів Silvaco TCAD. У рамках дифузійно-дрейфової моделі транспорту носіїв із врахуванням квантового потенціалу Бома отримані ефективні робочі параметри: допустимі значення порогової напруги, сили струму витоку та коефіцієнта I_{on}/I_{off} та їх залежності від температури. Отримано, що величини порогової напруги V_t та допорогового розкиду SS залишаються майже без змін із зростанням температури в інтервалі від 280 до 400 К, що насамперед пов'язано з додатковим впливом квантових ефектів для заданих товщини каналу та концентрацій домішок. Поряд з цим фіксується типове спадання сили струму ввімкнення на 45.5 % та струму витоку на 46.4 % в заданому інтервалі температур. Для оцінки термічної стабільності досліджуваних транзисторних систем розраховані температурні коефіцієнти β_{Vt}, β_{SS}, β_{Ion} and β_{Ioff}. Їх величини становили відповідно $8.63 \cdot 10^{-5}$; $-0.53 \cdot 10^{-5}$; $-3.87 \cdot 10^{-3}$ and $-3.80 \cdot 10^{-3}$ K^{-1}. Результати чисельного моделювання показали добре узгодження з експериментальними даними.

Ключові слова: Польовий транзистор з каналом на основі нанодроту, Моделювання, Температурний

коефіцієнт електричних параметрів.