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# Analysis of Crosstalk Noise Using Graphene Nanoribbon Interconnects by Changing Wire Spacing and Electron Mean Free Path

S. Bhattacharya[1,*], S. Das[2], S. Tayal[1], J. Ajayan[1], L.M.I. Leo Joseph[1], D. Das[3]

[1] *Department of Electronics and Communication Engineering, SR University, Warangal, Telangana, India*
[2] *School of VLSI Technology, Indian Institute of Engineering Science and Technology, Shibpur, India*
[3] *Department of Electronics and Communication Engineering, Assam University, Silchar, India*

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In this article, we study the coupling capacitance ($C_C$) and its effects on crosstalk noise in next generation high performance on-chip nano-integrated circuits by changing wire spacing and electron mean free path (MFP) between two neighboring nets using graphene nanoribbon (GNR) interconnects. For coupling capacitance analysis, three multilayer graphene nanoribbon (MLGNR) interconnects with different wire spacing (variation between 10 to 300 nm) and different interconnect length (100, 200 and 300 μm) are considered. It is observed that a smaller separation gap between two neighboring nets shows 4-6× higher coupling capacitance compared to a larger wire spacing. In terms of mean free path (MFP), a higher MFP shows 20-34 % less coupling capacitance compared to a lower MFP. In crosstalk noise analysis, a tri-interconnect model with a driver load circuit (i.e., a CMOS inverter circuit with aggressor and victim net) is used to study the performance of GNR interconnects in terms of noise peak with different possible input combinations. It is also observed that the higher MFP of the MLGNR interconnect shows less noise peak (1.11 mV with 1200 nm MFP), whereas the lower MFP shows higher noise peak (3.65 mV with 300 nm MFP). This analysis is useful for area-efficient and noise-immune next generation high-speed integrated circuit design using GNR interconnects.

**Keywords:** Graphene nanoribbon (GNR), Mean free path (MFP), Interconnects, Temperature, Crosstalk.

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## 1. INTRODUCTION

Wire spacing in nanometer dimension for next generation high speed integrated circuit design is one of the challenging research areas [1]. Decreasing the wire spacing between two neighboring nets can cause crosstalk noise due to increased coupling capacitance [2, 3]. Similarly, increasing wire spacing between two neighboring nets can reduce the crosstalk effect, but it will require more on-chip area, which is contrary to Moore's law [4, 5]. As a result, we need to think about some compromise in wire spacing between two neighboring nets for next generation advance, low power and high-speed integrated circuit design. Current studies show that multilayer graphene nanoribbon (MLGNR) interconnects are one of the most promising materials for modeling interconnects because they exhibit some remarkable properties over traditional interconnect materials (for example, Cu, Al, Ni, etc.) [6-10]. It is a stack of single layer GNR (SLGNR) structures. It is a highly stable material with a wide temperature range (~ 30 to 500 K) and 40 × harder than diamonds. It demonstrates high current conduction capability ~ 10× higher than Cu nanomaterials and is highly immune to noise in nanoelectronic circuits. MLGNR interconnect also suppresses crosstalk noise with closed spacing between two neighboring nets compared to other nanomaterials. In this work, we mainly investigated crosstalk noise between two MLGNR interconnects placed in parallel using wire spacing variation and electron mean free path (MFP) variation. Cross-coupling capacitance ($C_C$) is measured with different wire spacing and different MFP. This coupling capacitance ($C_C$) is the main source of noise in nanoelectronic circuits.

The rest of the paper is organized as follows. Section 2 represents the interconnect model for noise calculation. Section 3 presents the results and discussion. The conclusions are given in Section 4.

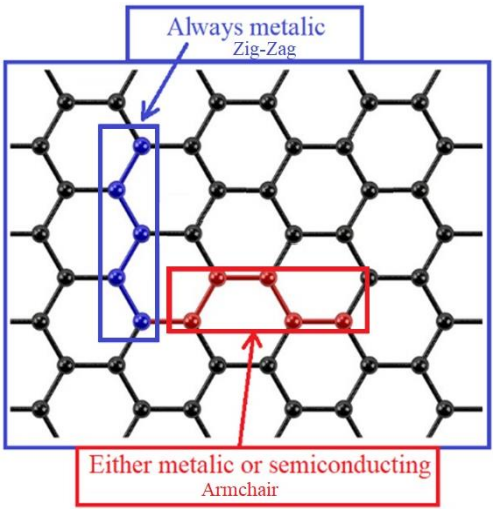


**Fig. 1** – Schematic representation of a graphene sheet with Zigzag (metallic) and Armchair (either metallic or semiconducting) nanostructures

## 2. INTERCONNECT MODEL

Fig. 1 shows one graphene sheet of atomic thickness with a two-layer orientation. The first orientation is

* sandip.bhattacharya@sru.edu.in

 

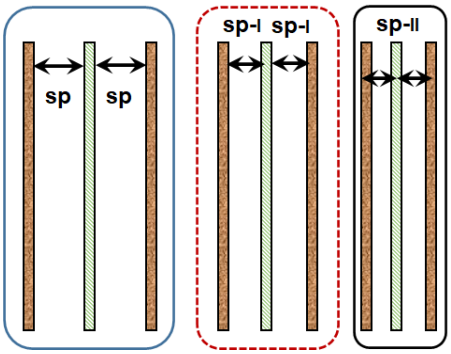


**Fig. 2** – Schematic representation of tri-interconnect MLGNR interconnect model (top-view model) with different wire spacing (sp > sp-I > sp-II)

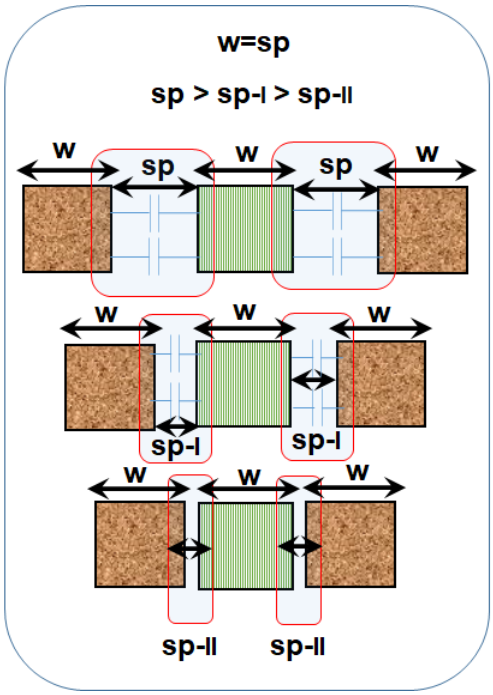


**Fig. 3** – Schematic representation of tri-interconnect MLGNR interconnect model (side-view model) with different wire spacing (sp > sp-I > sp-II)

called the Zigzag pattern, which always shows metallic properties, whereas the second orientation is called the Armchair and shows sometimes metallic and sometimes semiconducting properties. In this analysis, we considered only metallic properties for GNR-based interconnect modeling. Fig. 2 and Fig. 3 show the tri-interconnect model with top-view and side-view for MLGNR interconnect with different wire spacing (sp, sp-I, sp-II). Fig. 4 shows the GNR tri-interconnect model with driver and load circuits. Three driver and load circuits are considered for coupling capacitance ($C_C$) and crosstalk noise analysis. Each driver and load circuit is connected by GNR-based $RLC_g$ interconnect. Here, $R$ and $L$ are represented as line resistance and line capacitance, whereas $C_g$ is represented as ground capacitance. In GNR interconnect, the line resistance is distributed with the contact resistance ($R_C$), as well as with the quantum resistance ($R_Q$). Here, the line resistance is represented as $R = R_C + R_Q$. Similarly, the line capacitance ($C$) is distributed with the quantum capacitance ($C_Q$) and the electrostatic capacitance ($C_E$). Here, the line resistance is represented as $C = C_E + C_Q$. For coupling capacitance ($C_C$) analysis, we considered 1) the spatial variation between aggressor and victim net, 2) the MFP variation of MLGNR interconnect. For crosstalk noise analysis, we considered the input test pattern shown in Fig. 5. Using this test pattern, we can analyze the impact on the circuit performance. In Fig. 5, the primary condition for noise analysis is highlighted in red. When introducing aggressor net-1 and aggressor net-3, they switch from logic-0 to logic-1 and from logic-1 to logic-0, respectively, while victim net is held at logic-0 and logic-1, so, rise and fall of noise will appear at the output from the victim net. Rise and fall of noise (crosstalk noise) will degrade the circuit performance and, as a result, problems with circuit reliability will arise.

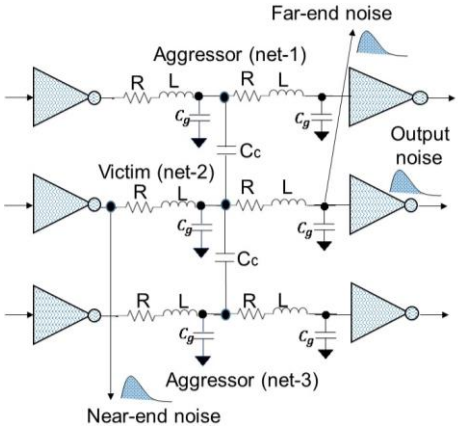


**Fig. 4** – Schematic diagram of coupled interconnects

| Sl. No | Aggressor Net I | Aggressor Net II | Victim Net | Result | Impacts |
|---|---|---|---|---|---|
| **Crosstalk Delay Analysis** | | | | | |
| 1 | 0 → 1 | 0 → 1 | 0 → 1 | Decrease in rise time | Speed-up |
| 2 | 0 → 1 | 0 → 1 | 1 → 0 | Increase in fall time | Slow-down |
| 3 | 1 → 0 | 1 → 0 | 0 → 1 | Increase in rise time | Slow-down |
| 4 | 1 → 0 | 1 → 0 | 1 → 0 | Decrease in fall time | Speed-up |
| **Crosstalk Noise Analysis** | | | | | |
| 5 | 0 → 1 | 0 → 1 | 1 → 1 | Overshoot | Reliability |
| 6 | 0 → 1 | 0 → 1 | 0 → 0 | Rise Noise/Glitch | Functionality |
| 7 | 1 → 0 | 1 → 0 | 1 → 1 | Fall Noise/Glitch | Functionality |
| 8 | 1 → 0 | 1 → 0 | 0 → 0 | Undershoot | Reliability |

**Fig. 5** – Effects of crosstalk on the circuit performance

All experiments were performed in the MATLAB and T-SPICE simulation environment. The input voltage is applied to the driver side. In this analysis, the input voltage swings from 0 to 1 V and the pulse rise/fall time is assumed to be 50 ps. Driver and load are inverting buffers designed using the latest 95 nm ITRS-2011 technology node with SPICE models from the predictive technology model.

## 3. RESULTS AND DISCUSSION

In this section, we discuss about the coupling capacitance ($C_C$) and its effect on crosstalk noise generation in next generation nano-integrated circuit design. Higher coupling capacitance generates a high noise peak, which

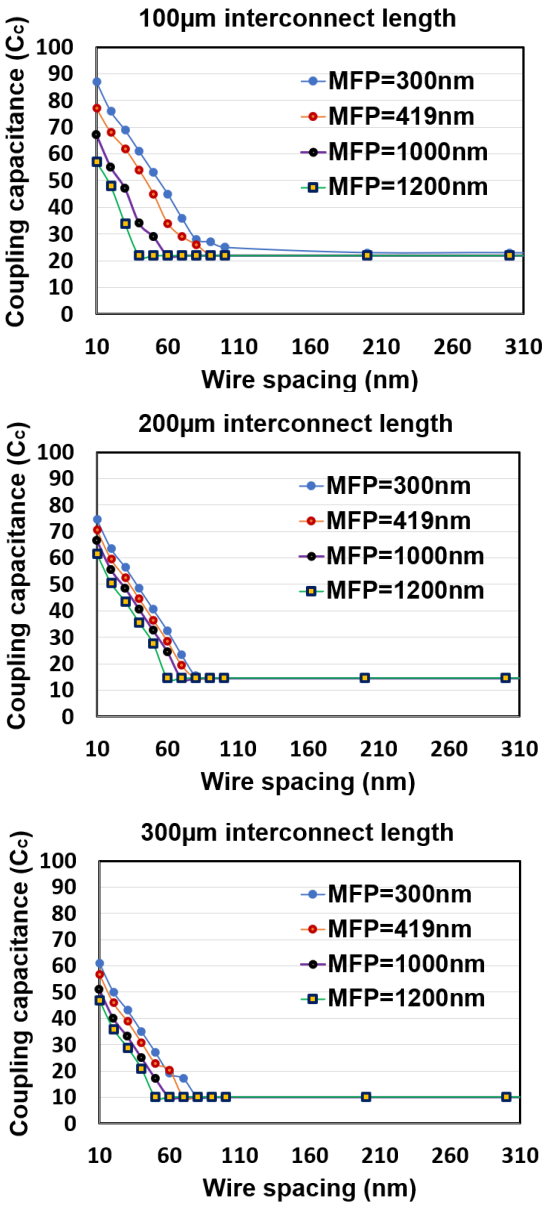


**Fig. 6** – Wire spacing (nm) vs coupling capacitance (fF) with different MFP (300, 419, 1000 and 1200 nm)

may cause circuit reliability issues. Here we show how wire spacing and a higher GNR mean free path (MFP) can reduce the coupling capacitance ($C_C$). As a result, much fewer noise peaks will be generated in the circuit, which can improve the circuit performance. Fig. 6 shows the coupling capacitance ($C_C$) vs wire spacing (nm) plot for three different interconnect lengths (100 to 300 µm). In this analysis, the interconnect length is categorized as smaller (100 µm), medium (200 µm) and larger (300 µm). For smaller length (100 µm), the coupling capacitance ($C_C$) shows ~ 90 fF at 300 nm MFP and ~ 62 fF at 1200 nm MFP with 10 nm wire spacing. Similarly, for medium length (200 µm), the coupling capacitance ($C_C$) shows ~ 75 fF at 300 nm MFP and ~ 60 fF at 1200 nm MFP with 10 nm wire spacing. Similarly, for larger length (300 µm), the coupling capacitance ($C_C$) shows ~ 60 fF at 300 nm MFP and ~ 48 fF at 1200 nm MFP with 10 nm wire spacing. It is clear from the above analysis that a larger interconnect length (300 µm) shows lower coupling capacitance compared to a smaller interconnect length (100 µm). In Fig. 7, it is observed that the higher MFP (1200 nm) shows a lower noise peak (1.1 mV) compared to the smaller MFP (300 nm) with a noise peak of 3.65 mV.

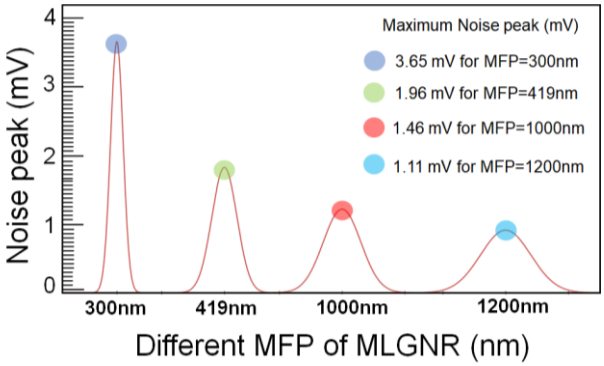


**Fig. 7** – Crosstalk noise peak (mV) vs different MFP

## 4. CONCLUSIONS

In this work, we analyzed the effect of coupling capacitance ($C_C$) in GNR interconnects in a wide range of wire spacing at nanometer dimension, different interconnect lengths at µm dimension and different MFPs at nanometer dimension. It was observed that the higher coupling capacitance in an on-chip integrated circuit produces a significant amount of crosstalk noise, which can cause logic failure and reliability issues in a nanoelectronic circuit. From this analysis, it was also observed that a GNR interconnect with a higher MFP value shows less coupling capacitance that also results in reduced crosstalk noise, which can improve the circuit performance in terms of signal integrity.

## ACKNOWLEDGEMENTS

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## Аналіз шуму перехресних перешкод за допомогою міжз'єднань графенової наностpічки шляхом зміни відстані між дротами та середнього вільного пробігу електронів

S. Bhattacharya[1], S. Das[2], S. Tayal[1], J. Ajayan[1], L.M.I. Leo Joseph[1], D. Das[3]

[1] *Department of Electronics and Communication Engineering, SR University, Warangal, Telangana, India*
[2] *School of VLSI Technology, Indian Institute of Engineering Science and Technology, Shibpur, India*
[3] *Department of Electronics and Communication Engineering, Assam University, Silchar, India*

Ми вивчаємо вплив емності зв'язку ($C_C$) на шум перехресних перешкод у високопродуктивних вбудованих наноінтегральних схемах наступного покоління шляхом зміни відстані між дротами та середнього вільного пробігу (MFP) електронів між двома сусідніми мережами за допомогою міжз'єднань графенової наностpічки (GNR). Для аналізу емності зв'язку розглядаються міжз'єднання трьох багатошарових графенових наностpічок (MLGNR) з різною відстанню між дротами (від 10 до 300 нм) і різною довжиною міжз'єднання (100, 200 і 300 мкм). Помічено, що менший зазор між двома сусідніми мережами демонструє в 4-6 разів більшу емність зв'язку порівняно з більшою відстанню між дротами. З точки зору MFP електронів, більша величина MFP показує на 20-34 % меншу емність зв'язку порівняно з меншою величиною MFP. При аналізі шуму перехресних перешкод модель із трьома з'єднаннями зі схемою навантаження драйвера (тобто схемою CMOS-інвертора з мережею агресора та жертви) використовується для вивчення продуктивності з'єднань GNR з точки зору пікового шуму з різними можливими комбінаціями входів. Також помічено, що більша величина MFP міжз'єднання MLGNR демонструє менший пік шуму (1,11 мВ з MFP = 1200 нм), тоді як менша величина MFP демонструє вищий пік шуму (3,65 мВ з MFP = 300 нм). Наведений аналіз корисний для проектування високошвидкісних інтегральних схем нового покоління, які є ефективними за площею та стійкими до шуму, з використанням з'єднань GNR.

**Ключові слова:** Графенова наностpічка (GNR), Середній вільний пробіг (MFP), Міжз'єднання, Температура, Шум перехресних перешкод.