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Performance Estimation of Recessed Modified Junctionless Multigate Transistor

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Scaling has been instrumental in improving speed and power consumption. Moore's law insists on a constant periodic decrease in the size of devices. Gate dielectric engineering is one of the means to reduce the size of devices. This paper describes the simulation of the electrical characteristics of a reduced channel width and an increased dielectric thickness at the gate edges of a junctionless multigate transistor. The novelty of the work is the increased gate oxide thickness at the edges that reduces the leakage current. HfO_2 is used as a dielectric material because thin SiO_2 layer causes leakage through the gate oxide and into the channel. The excellent property of HfO_2 is its high dielectric constant value (20-25), which is 4 to 6 times higher than of SiO_2. In this work, the performance parameters of a double-gate junctionless FET, namely the threshold voltage (V_{th}), OFF-current, ON-current, ON-to-OFF current ratio, and subthreshold swing (SS), have been investigated for the gate work function window from 4.6 to 5.0 eV. In the work function window, optimal performance has been found for a gate work function of 4.9 eV. The proposed device has low I_{OFF} and subthreshold swing when compared to conventional junctionless FET. This paper presents the simulation of a junctionless transistor using Atlas Silvaco TCAD tool. The device shows OFF-current of the order of 10^{-16} A/μm, ON-to-OFF current ratio of the order of 10^{11} and subthreshold swing of 59.78 mV/dec. The device shows constant subthreshold swing for the work function range of 4.6 to 5.0 eV. The simulation results show that the proposed device is suitable for low power applications.

Keywords: Junctionless field effect transistor (JLFET), Work function (WF), Recessed modified JLFET, Subthreshold swing (SS), Oxide thickness at the gate edges, Reduced channel width, HfO_2.

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1. INTRODUCTION

Junctionless field effect transistor (JLFET) was introduced by J.E. Lilienfeld in the 1920s and the device was fabricated in 2010 [1, 2]. The requirements for JLFET are that the transistor must be heavily doped ($1 \cdot 10^{19}$ cm^{-3}), and the channel thickness has to be on the nanometer scale (10 nm) [2]. JLFET is a variable resistor turned on by the gate voltage [3, 4]. JLFET is described as an accumulation mode device, in which the doping concentration is the same in source, channel and drain [5, 6]. As the gradient of the doping concentration between source and channel or drain and channel is zero, no *p-n*-junction formation is necessary during the fabrication, which eliminates the need for expensive annealing techniques and allows the fabrication of devices with shorter channels [7, 8]. In JLFET, the electric current flowing through it is controlled by the applied gate voltage. Two gates, i.e., front and back gates, and an ultra-thin body reduce short channel effects (SCEs) in double gate devices [9]. In JLFET, the work function (WF) difference between metal and semiconductor maintains the device in the OFF state. Due to the scaling effect, the reduction in transistor size decreases the gate oxide thickness, which causes SCEs by hot carriers such as an increase in the parasitic current on the gate oxide and an increase in power consumption. The recessed channel reduces SCEs [10]. As the electric field is low in JLFET, the hot carrier effect is reduced [11]. Performance can be improved by using a high-*k* dielectric material (HfO_2) as the gate oxide, since scaling of SiO_2 results in more leakage as its thickness decreases [12, 13]. Modifying the gate oxide structure changes the energy bands of the carriers under the gate, resulting in a reduction of the leakage current.

Increasing the gate oxide thickness at both edges reduces band to band tunnelling [14]. In the case of a recessed double-gate JLFET (R_DGJLFET) in the OFF-state, fewer charge carriers in the channel were found, resulting in lower I_{OFF}, much better I_{ON}/I_{OFF}, and smaller subthreshold swing (SS). By increasing the WF value, greater gate control over the channel region is achieved, and hence a reduction in I_{OFF} is observed with better I_{ON}/I_{OFF} [15]. SS is a parameter used to measure how quickly the current decreases when the transistor turns to the OFF state [16]. SS of a conventional FET is limited to 60 mV/decade due to the current generation dependent on thermionic emission. For low I_{OFF}, SS should be small. It has a great influence on the leakage current, power consumption, and ON-to-OFF current ratio. JLFETs are highly doped semiconductors, which are volume depleted in the OFF state [17]. The device has good turn-off characteristics [18, 19]. Here, recessed modified JLFET is proposed using the concept of increased thickness at the gate edges and recessed channel. The paper also provides a detailed analysis of how the variation in WF results in changes in the performance parameters, namely V_{th}, I_{OFF}, I_{ON}, ON-to-OFF current ratio (I_{ON}/I_{OFF}), and SS. The performance of R_DGJLFET against variations in the gate WF was further improved by a structure called recessed modified double-gate JLFET (R_M_DGJLFET). The

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range of WF values from 4.6 to 5.0 eV was identified as the work function window (WFW) to obtain optimal performance of R_M_DGJLFET for low power applications. JLFET does not charge in the OFF state, considerable V_{DS} can lead to band overlap between the channel and drain regions. Band overlap causes tunnelling [17]. The dielectric thickness at the edges is increased and a minimum thickness is maintained at the center, resulting in less tunnelling in the device. Drain-induced barrier lowering (DIBL), which is SCE, represents the reduction of the FET threshold voltage at higher drain voltages. DIBL is reduced in R_M_DGJLFET. The proposed R_M_DGJLFET design is optimized by incorporating the best results from the TCAD simulations. The whole paper is categorized into three sections: the first section of the paper includes device parameters and simulations, the second section discusses the results, and the conclusions are included in the last section.

2. DEVICE STRUCTURE, PARAMETERS AND SIMULATION MODELS

Fig. 1 represents the schematic structure of R_M_DGJLFET using HfO_2 as a high-k dielectric medium. The gate oxide thickness is 5 nm at the edges (t_{ox1}) and 1 nm in the central region (t_{ox2}), the physical gate length (GL) is 20 nm. The device consists of a source with an effective length of 10 nm and a drain with an effective length of 10 nm, the silicon film thickness (T_{Si}) is 10 nm. The gate WF is set to 4.9 eV and other parameters are varied accordingly. The doping concentration of the device is set to 1·19 cm^{-3} (n-type). Fig. 2 explicitly shows the variation between the simulated and published models [15]. The leakage current in the proposed model is less compared to the published model. All simulations are implemented in the Silvaco 2D simulator, technology computer aided design (TCAD) with concentration-dependent carrier mobility. The Shockley-Read-Hall Model uses fixed minority carrier lifetimes, the Lombardi CVT Model takes into account mobility degradation, the Bandgap Narrowing Model considers bandgap narrowing effects, the Fermi-Dirac Model takes into account high doping in the channel, the Band-to-Band (Nonlocal) Model analyzes the effect of band-to-band tunnelling (BTBT). The parameters used for device simulation are listed in Table 1. The simulated data of the characteristic curves are found out by using Plot Digitizer tool.

3. RESULTS AND DISCUSSION

The results were obtained using Silvaco Atlas TCAD tools. Fig. 3 represents the simulated I_{DS} versus V_{GS} graph with the variation of gate WF from 4.6 to 5.0 eV. The OFF-state current is reduced to 7.47e-16 A/μm as WF increases from 4.6 to 4.9 eV. The OFF-state current is 1.60e-17 A/μm for a WF of 5.0 eV as V_{th} increases to 0.66 V. So, a WF of 4.9 eV is considered the optimal value. Fig. 4 shows I_{ON}/I_{OFF}. The current ratio I_{ON}/I_{OFF} is observed to increase with increasing WF, because the OFF-current decreases. Fig. 5 depicts an increase in the threshold voltage with increasing WF. A higher applied voltage is needed to decrease the potential to enable

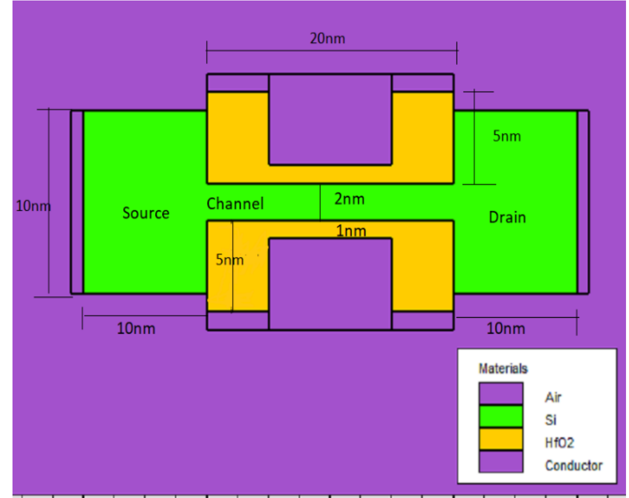

Fig. 1 – Cross-sectional 2D structure of R_M_DGJLFET

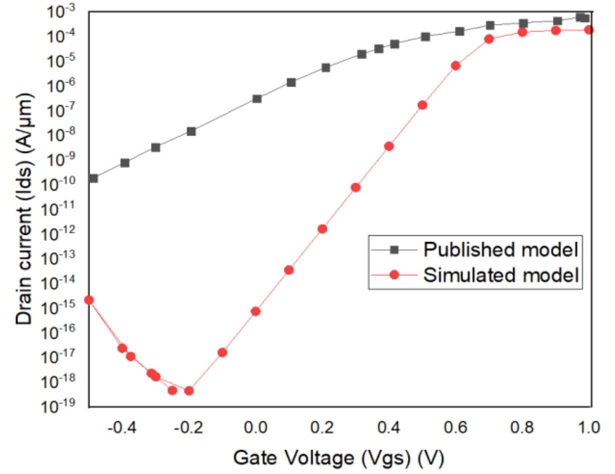

Fig. 2 – Drain current of the simulated and published models [15]

Table 1 – Device parameters of R_M_DGJLFET

Parameters	Values
Doping concentration	1×10^{19} cm^{-3}
Gate length (GL)	20 nm
Source length (SL)	10 nm
Drain length (DL)	10 nm
Channel thickness (T_{Si})	10 nm
Gate oxide thickness at the edges (t_{ox1})	5 nm
Gate oxide thickness in the center (t_{ox2})	1 nm
Gate work function (WF)	4.9

electron flow, hence V_{th} increases with WF. Table 2 lists the electrical parameters of the proposed model for a WFW of 4.6-5.0 eV. As the WF value increases, I_{OFF} decreases due to good volume depletion in the OFF state. SS is equal to 59.78 mV/dec, as shown in Table 2. This feature is a slight improvement when compared to conventional JLFET having 60 mV/dec [7]. In n-channel JLFETs, electron tunneling from the valence band of the channel to the conduction band of the drain leaves behind holes in the channel, which increase the channel potential [17]. In the proposed design at V_{GS} =0.0 V, V_{DS} = 0.05 V, a decrease in WF results in lowering the electric field along the channel, as shown in Fig. 6. The

concentration of electrons in the channel and potential variation along the channel also decrease. Lowering the electric field reduces the hot carrier effect, which is one of SCEs. It has been observed that the proposed device achieves improved depletion with a lower electron concentration in the OFF state due to the reduced silicon thickness in the channel region.

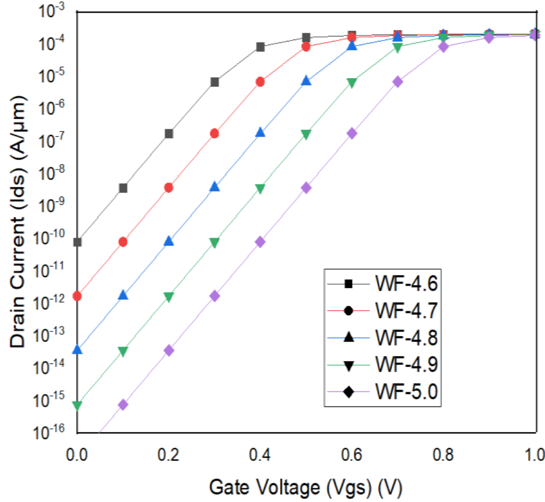

Fig. 3 – Transfer characteristics of I_{DS} (drain current) vs. V_{GS} (gate voltage) for different values of gate WF varied from 4.6 to 5.0 eV for *n*-type JLFET. For doping of $1 \cdot 10^{19}$ cm^{-3}, V_{GS} = 0-1.0 V, V_{DS} = 0.05 V

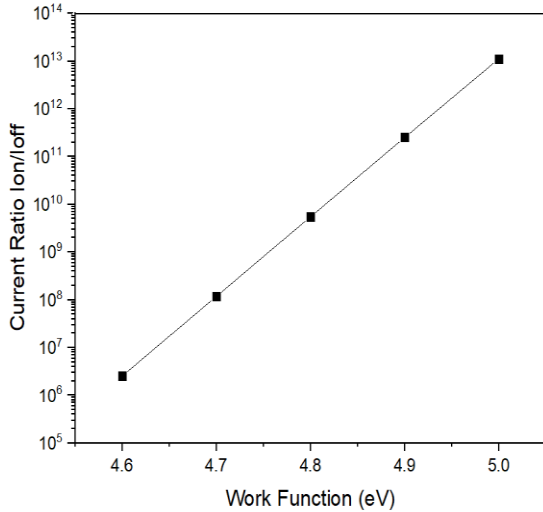

Fig. 4 – Transfer characteristics of I_{ON}/I_{OFF} vs. WF for *n*-type JLFET at V_{DS} = 0.05 V, V_{GS} = 0-1 V

Fig. 7 shows the transfer I_{DS}-V_{GS} characteristics for *n*-type JLFET as a function of V_{DS} (drain to source voltage). It is seen from the figure that the drain voltage will have very little effect on the drain current, which indicates good gate control over the leakage current. However, the drain current slowly increases with increasing V_{DS}, as shown in Table 3. The ON state current of 2.23e-04 A/μm is obtained at V_{DS} = 0.6 V. The I_{ON}/I_{OFF} current ratio begins to increase with increasing V_{DS} due to an increase in the ON current.

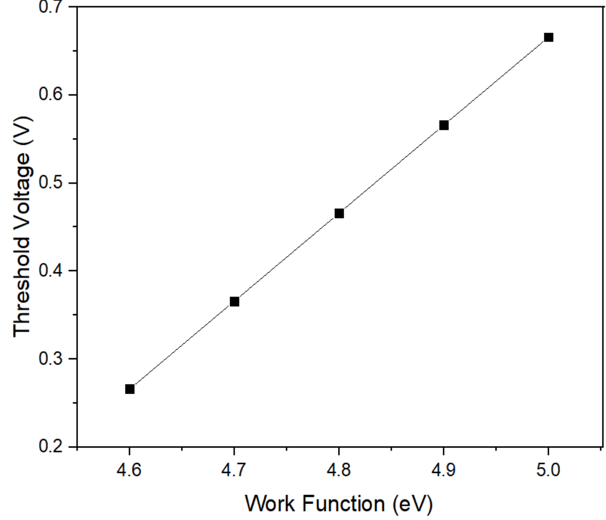

Fig. 5 – Transfer characteristics of the threshold voltage (V_{th}) vs. WF for *n*-type JLFET at V_{DS} = 0.05 V, V_{GS} = 0-1 V

Table 2 – Performance comparison for different WF values in R_M_DGJLFET

Parameters	Values				
WF (eV)	4.6	4.7	4.8	4.9	5
V_{th} (V)	0.27	0.37	0.47	0.57	0.67
SS (mv/dec)	59.81	59.79	59.78	59.78	59.78
I_{OFF} (A/μm)	7.78e-11	1.65e-12	3.52e-14	7.47e-16	1.60e-17
I_{ON} (A/μm)	1.98e-04	1.96e-04	1.94e-04	1.89e-04	1.79e-04
I_{ON}/I_{OFF}	2.54e+06	1.19e+08	5.52e+09	2.53e+11	1.12e+13

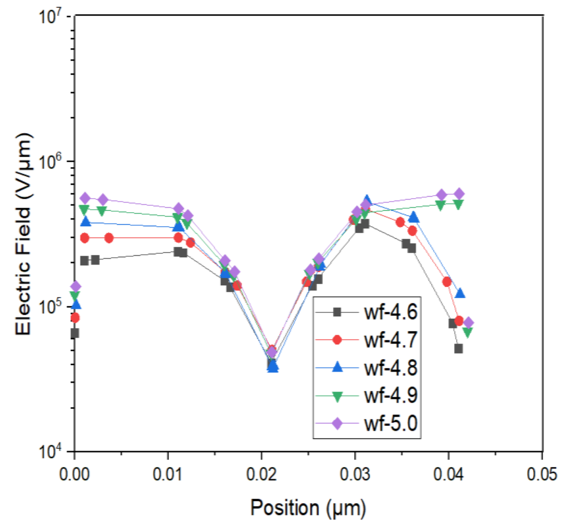

Fig. 6 – Electric field in the device in the OFF state, V_{GS} = 0 and V_{DS} = 0.05 V using the BTBT (Nonlocal) model

Now, the doping level of the device varies between $1 \cdot 10^{17}$ to $1 \cdot 10^{20}$ cm^{-3}. A doping level of $1 \cdot 10^{19}$ cm^{-3} is taken as the optimal value, as SS is 59.78. At a doping level of $1 \cdot 10^{20}$ cm^{-3}, SS increases to 61.44, so doping remains at a level of $1 \cdot 10^{19}$ cm^{-3}. An increase in the concentration increases I_{ON}, but due to the requirement of low SS, the doping level is kept at $1 \cdot 10^{19}$ cm^{-3}.

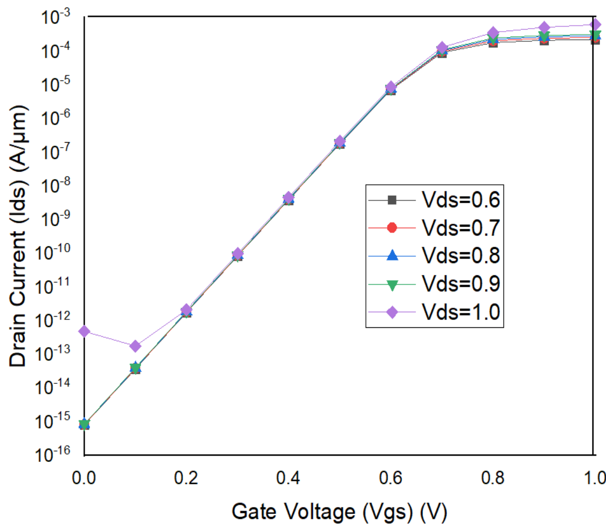

Fig. 7 – Transfer characteristics of V_{GS} vs. I_{DS} for *n*-type JLFET for different V_{DS} values

Table 3 – Performance comparison for different V_{DS} values in R_M_DGJLFET

Parameters	Values				
V_{DS} (V)	0.6	0.7	0.8	0.9	1
V_{th} (V)	0.57	0.57	0.57	0.58	0.14
SS (mV/dec)	59.78	59.78	59.77	59.77	59.78
I_{OFF} (A/μm)	7.89e–16	8.17e–16	8.36e–16	8.50e–16	4.76e–13
I_{ON} (A/μm)	2.23e–04	2.56e–04	2.86e–04	3.14e–04	6.17e–04
I_{ON}/I_{OFF}	2.83e+11	3.13e+11	3.42e+11	3.70e+11	1.30e+09

A decrease in the OFF-current with decreasing T_{Si} is due to the fact that BTBT from the channel to the drain is lower for JLFET with a thin device layer. JLFET with thick T_{Si} has high drain control over the channel, so the tunneling barrier width between the channel and the drain will be slightly smaller compared to devices with thin T_{Si} [17]. When the dielectric thickness at the gate edges increases, it changes the energy band distributions of the carriers near the gate sidewall. This prevents a sharp drop/rise in the energy band from the gate region to the drain and source regions of the device, and then lessens the overlap between the valence and conduction bands in the channel and the drain separately to reduce the effect of BTBT [14]. In the simulated model, 2 nm T_{Si} and 5 nm edge thickness are used in order to reduce I_{OFF} and tunnelling width when compared to a thick channel layer. In the output, for 5 nm edge thickness and 2 nm T_{Si} a gradual decay of the bands from the channel to the drain is observed. Fig. 8 shows the band energies for gate edge thicknesses of 5 and 1 nm. For 1 nm thickness, there is an abrupt drop in the conduction and valence band energies. So, electron tunnelling will be greater at 1 nm thickness.

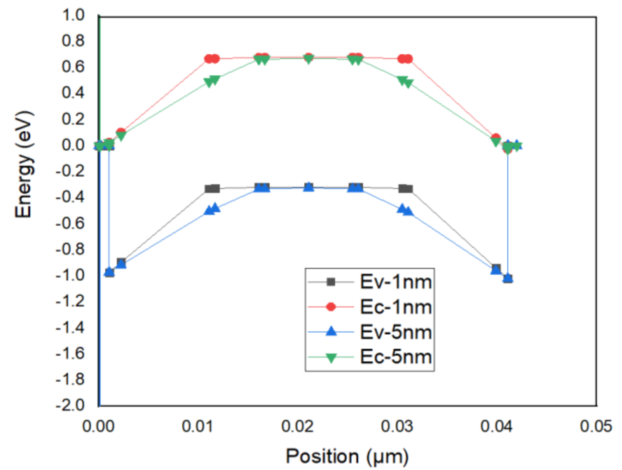

Fig. 8 – Conduction and valence band energies for thicknesses of 1 and 5 nm at the gate edges

4. CONCLUSIONS

R_M_DGJLFET device was formed by reducing the channel width and increasing the dielectric thickness at the edges. The device performance was compared to that of R_DGJLFET. Depending on WF and dielectric thickness, the performance of the device increased. The effects of change in WF, drain voltage, oxide thickness, and electric potential were analyzed. I_{OFF} was optimized at a WF of 4.9 eV and an oxide thickness of 5 nm at the edges. An increase in the WF decreases the electron concentration, electric field and potential in the channel in the OFF state. An increase in the oxide thickness at the gate edges changes the energy bands, slowing down band bending, hence tunnelling is reduced.

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Оцінка продуктивності модифікованого безперехідного багатозатворного транзистора із вбудованим каналом

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Масштабування відіграло важливу роль у покращенні швидкості та енергоспоживання. Закон Мура наполягає на постійному періодичному зменшенні розмірів пристроїв. Інженерія затворних діелектриків є одним із засобів зменшення розмірів пристроїв. У роботі описується моделювання електричних характеристик зменшеної ширини каналу та збільшеної товщини діелектрика на краях затвора безперехідного багатозатворного транзистора. Новизна роботи полягає у збільшеній товщині оксиду затвора по краях, що зменшує струм витоку. HfO_2 використовується як діелектричний матеріал, оскільки тонкий шар SiO_2 викликає виток через оксид затвора в канал. Відмінною властивістю HfO_2 є його висока діелектрична проникність (20-25), яка в 4-6 разів перевищує проникність SiO_2. У роботі були досліджені параметри продуктивності двозатворного безперехідного FET, а саме порогова напруга (V_{th}), струм вимкнення (I_{OFF}), струм увімкнення (I_{ON}), відношення струму увімкнення до струму вимкнення (I_{ON}/I_{OFF}) та підпорогове коливання (SS) для вікна роботи виходу затвора від 4,6 до 5,0 еВ. У вікні роботи виходу було знайдено оптимальну продуктивність для роботи виходу затвора 4,9 еВ. Запропонований пристрій має низький струм вимкнення та підпорогове коливання порівняно зі звичайним безперехідним FET. У роботі представлено моделювання безперехідного транзистора за допомогою інструменту Atlas Silvaco TCAD. Пристрій показує струм вимкнення порядку 10^{-16} А/мкм, відношення струму увімкнення до струму вимкнення порядку 10^{11} і підпорогове коливання 59,78 мВ/дек. Пристрій демонструє постійне підпорогове коливання для діапазону робот виходу від 4,6 до 5,0 еВ. Результати моделювання показують, що пропонований пристрій підходить для малопотужних застосувань.

Ключові слова: Безперехідний польовий транзистор (JLFET), Робота виходу (WF), Модифікований JLFET із вбудованим каналом, Підпорогове коливання (SS), Товщина оксиду на краях затвора, Зменшена ширина каналу, HfO_2.