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Extensive Study of Position-Dependent Multi-Channel GAA MOSFET and its Effect on Device Performance

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In this paper, a simulation study is carried out for a multi-channel gate all around (GAA) MOSFET with channel separation calculation. The simulation is performed in lower technology nodes by taking the quantum effect into consideration. The insulator used in this model is a high-k dielectric, which allows the device to be scaled down. The separation between the silicon channel and its effect on device performance is investigated extensively. The performance thus obtained is compared with different channel separations in terms of drain current (I_D), threshold voltage (V_{th}), transconductance (g_m) and switching ratio (I_{on}/I_{off}). Further, the leakage current and associated short channel effect such as subthreshold swing (SS) and its dependence on channel separation are studied in detail. An improved value of on-current of 28.9 % along with SS of 70.34 mV/dec is achieved for a separation of 10 nm. However, a switching ratio of 9.13e+08 is obtained for a separation of 6 nm which is comparatively higher than 9 and 10 nm separation.

Keywords: GAA, High-k, Leakage current, Subthreshold swing, Quantum.

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1. INTRODUCTION

With the continuous downscaling of device dimensions to preserve Moore's law for the next generation, MOSFET is considered as the driving force that provides valuable solutions in lower technology nodes [1, 2]. GAA device architectures provide optimal electrostatic control, thereby enabling ultimate scaling of CMOS devices. As the size of transistors is scaled down the performance of the device also gets affected, and an unwanted effect like subthreshold swing (SS) called the short channel effect appears [3-5]. Moreover, the GAA structure provides the minimum leakage current (I_{off}) with a steeper subthreshold slope [6, 7]. To mitigate the short channel effect, various device structures were proposed by considering different engineering techniques such as gate and channel engineering [8]. Today FinFET is used exclusively for CMOS technology [9-12]. However, FinFET faces multiple hurdles in the process of integrating and scaling. Although GAA MOSFET is considered the leader in the present transistor family, the driving current capability can be further increased by adding some device level modifications or adding to the device physics. A unique structure is introduced by adding multiple numbers of nanowires as a cannel instead of a single channel [13]. To get comparatively better performance and layout area, GAA MOSFET should include several vertical stacked nanowires as channels. The introduction of vertical nanowires as a channel not only improves the device performance, but also provides additional mechanical strength of the proposed device. The advantages that will enable an increase in device performance are that silicon rods as a channel are controlled by a single gate. The arrangement of silicon pillars as a channel affects the device performance extensively. The position of the silicon channels and the distance between the channels leads to a significant change in device performance. Separation between channels affects the electron mobility as well as the potential distribution in individual silicon channels when they are close and far from each other. Improved drain current with low SS and lower threshold voltage is obtained for different cases studied throughout the manuscript.

2. DEVICE DESIGN AND SIMULATION

A 3D device structure along with a 2D cross section view is proposed and depicted in Fig. 1. The dimensions of the device include a gate length of 20 to 6 nm with a gate metal work function of 4.7 eV. A doping concentration of 1×1020 cm^{-3} is applied to the source and drain. However, the channel is doped with a doping concentration of 1×1016 cm^{-3} to make it intrinsic. A spacer with a length $L_{sp} = 6$ nm is applied to both sides to mitigate the fringing capacitance effect. A temperature of 300 K along with a uniform doping method is applied to the proposed structure. The details of the device dimensions are included in Table 1. Different transport models are used for simulation, including Fermi-Dirac, band gap narrowing (BGN), drift-diffusion, velocity saturation, band-to-band tunneling, and carrier mobility models. The drift-diffusion model is used to examine the current transport behavior of the proposed model. The simulation of this work is performed using Sentaurus TCAD device simulator from Synopsys [14]. The simulator is a state-of-the-art device-simulation tool having various models depending on the type of material and its structural complexity.

Physics is present to simulate the device at both higher and lower technology nodes. Apart from the drift diffusion model, this simulator also includes a quantum-based model in order to simulate devices with very short gate lengths, and source and drain very close to each other.

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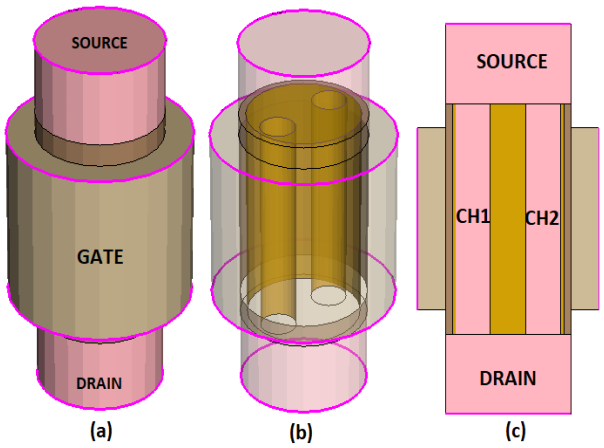

Fig. 1 – (a) 3D structure, (b) internal structure, (c) cross-sectional view of a high-k dielectric based on multi-channel GAA MOSFET structure

These models are supplied with almost all physics to make the simulation more accurate and error free. The device under simulation is scaled down to 20 nm from 60 nm to investigate changes in device characteristics. We have introduced a high-k dielectric material (HfO_2), and Si_3N_4 is used as an interfacial oxide layer for easy fabrication with silicon channel. Table 1 lists all dimensions of the device taken into consideration in the simulation.

Table 1 – Device dimensions of the proposed structure

Device dimensions	Multi-channel GAA MOSFET
Channel length (L_g)	20-60 nm
Doping concentration (N_S/N_D)	Phosphorus (1e+20)
Doping concentration (N_A/N_D)	Boron (1e+16)
Oxide thickness (t_{ox})	16 nm Si_3N_4, 2 nm HfO_2
Channel thickness (t_{si})	10 nm
Source/drain extension (L_S/L_D)	20 nm

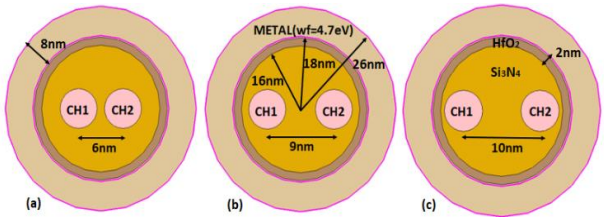

Fig. 2 – (a) 3D structure, (b) internal structure, (c) cross-sectional view of a high-k dielectric based on multi-channel GAA MOSFET structure

In order to get a clear idea into the device structure, a cross-section of the device along with the position of the channels and their separation is shown in Fig. 2. The channels, represented as channel 1 (CH1) and channel 2 (CH2), are separated by a distance of 6, 9 and 12 nm from each other, with other device dimensions as constant. The effect of the relative electric field and surface potential leads to a significant change in device performance in terms of drain current, threshold voltage and subthreshold slope.

3. RESULTS AND DISCUSSION

In this section, the effect of an electric field on an individual channel and the corresponding profile are illustrated in Fig. 3. Apart from the individual electric field distribution in the radial direction at the drain end, the distributed electric field is observed when both channels are weakly and strongly separated. When both channels are at a separation distance of 6 nm, the field is radiated more vertically than horizontally due to the relative field of the other channel. However, with a larger separation, the field is distributed radially inward, as shown in Fig. 3.

Fig. 4 illustrates the transfer characteristic curve for different separation distances of the channel-based device. From the figure, it is well observed that with an increase in the separation between the channels from 6 to 10 nm, the drain current increases significantly. However, a kink is observed in the transport characteristic curve. And this kink becomes more prominent as the separation increases. In order to get a clear insight, a log scale representation of the transfer characteristic is included in the inset of Fig. 4.

From Fig. 4, it can be observed that at low voltage there is a bending of the transfer characteristic in the subthreshold regime. And this bending becomes more prominent as the separation increases. This bending is due to the leakage current arising from the separation of the channels and the effect of the dielectric between them. The exact values of on-current, off-current and other parameters are illustrated in Table 2, where on-current, off-current, threshold voltage and SS are calculated for all three separation distances. The I_{on}/I_{off} ratio is found to be higher for 6 nm separation, but other parameters are better for the case of larger separation, as shown in Table 2.

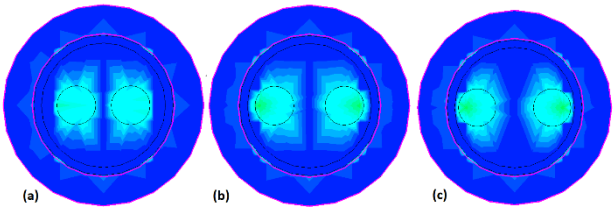

Fig. 3 – (a) Electric field distribution, (b) internal structure, (c) cross-sectional view of a high-k dielectric based on multi-channel GAA MOSFET structure

Table 2 – Device performance for different channel separations

V_{GS} = 1 V, V_{DS} = 0.5 V, L_g = 50 nm	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	V_t (V)	SS (mV/dec)
Channel separation 6 nm	8.378e-06	9.174e-15	9.13e+08	0.534	76.379
Channel separation 9 nm	1.072e-05	5.236e-13	2.05e+07	0.545	72.009
Channel separation 10 nm	1.179e-05	1.038e-12	1.14e+07	0.551	70.332

Table 3 – Different FOMs of the proposed device for a channel separation of 6 nm

Channel separation 6 nm	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	V_t (V)	SS (mV/dec)
V_{GS} = 0.7 V, V_{DS} = 0.5 V, Lg = 50nm	4.522e-06	9.174e-15	4.93e+08	0.534	76.007
V_{GS} = 1 V, V_{DS} = 0.5 V, Lg = 50 nm	8.378e-06	9.174e-15	9.13e+08	0.534	76.379
V_{GS} = 1.5 V, V_{DS} = 0.5V, Lg = 50 nm	1.165e-05	9.174e-15	1.27e+09	0.532	77.202

Table 4 – Different FOMs of the proposed device for a channel separation of 9 nm

Channel separation 9 nm	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	V_t (V)	SS (mV/dec)
V_{GS} = 0.7 V, V_{DS} = 0.5 V, Lg = 50nm	5.806e-06	5.306e-13	1.09e+07	0.543	71.720
V_{GS} = 1 V, V_{DS} = 0.5 V, Lg = 50 nm	1.072e-05	5.236e-13	2.05e+07	0.545	72.009
V_{GS} = 1.5 V, V_{DS} = 0.5V, Lg = 50 nm	1.450e-05	5.777e-13	2.51e+07	0.544	72.877

Table 5 – Different FOMs of the proposed device for a channel separation of 10 nm

Channel separation 10 nm	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	V_t (V)	SS (mV/dec)
V_{GS} = 0.7 V, V_{DS} = 0.5 V, Lg = 50nm	6.525e-06	1.032e-12	6.32E+06	0.550	70.076
V_{GS} = 1 V, V_{DS} = 0.5 V, Lg = 50 nm	1.179e-05	1.038e-12	1.14e+07	0.551	70.332
V_{GS} = 1.5 V, V_{DS} = 0.5V, Lg = 50 nm	1.472e-05	1.050e-12	1.40e+07	0.533	71.244

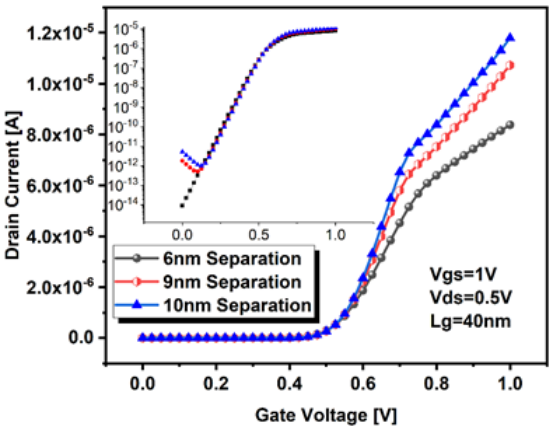

Fig. 4 – Transfer characteristic of the proposed structure for different channel separation distances

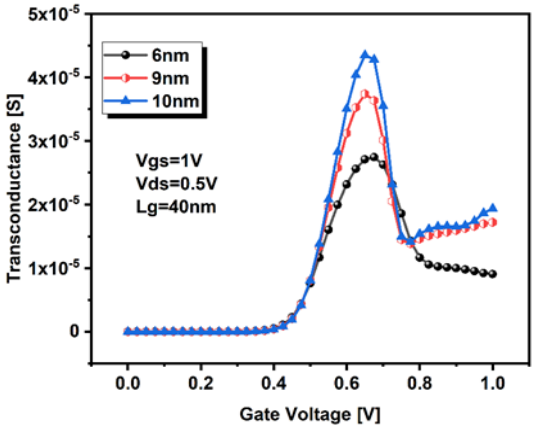

Fig. 5 – Transconductance of the proposed structure for different channel separation distances

The analysis is further extended to the extraction of transconductance (g_m) for the above-mentioned separation. As transconductance is one of the important device parameters when calculating device performance, an improved transconductance value is desirable for higher voltage gain and better analog performance. From Fig. 5, it can be observed that a higher value of transconductance is obtained for greater separation between the channels, and vice versa.

The threshold voltage of the device is extracted by transconductance method and is illustrated in Fig. 6. The threshold voltage at a voltage of 1 V and drain voltage of 0.5 V for a 60 nm device at different channel separation is shown in Fig. 6. From the figure, it can be observed that the threshold voltage is comparatively lower if the channel separation is less, and vice versa.

The analysis is then extended to the above mentioned three cases for different gate and drain bias. The gate voltage is taken as 0.7, 1 and 1.5 V to verify the superiority of the device in voltage scaling. The corresponding switching ratio along with SS is indicated clearly in Table 3, Table 4 and Table 5 for a channel separation of 6, 9 and 10 nm, respectively. For a channel separation of 6 nm, the switching ratio is better compared to the other two counterparts, but the swing is comparatively high. However, the threshold voltage is almost the same, as shown in tables.

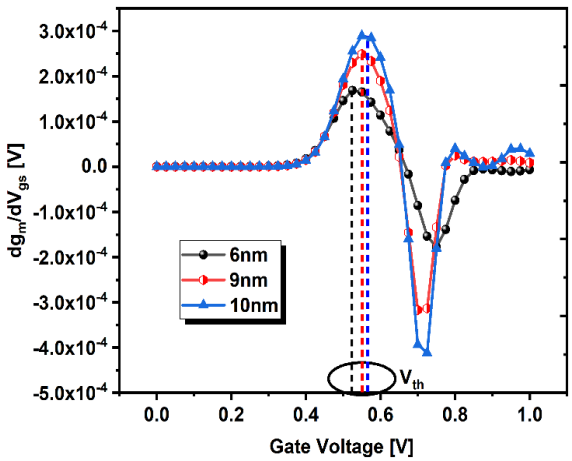

Fig. 6 – Threshold voltage extraction of the proposed structure for different channel separation distances

4. CONCLUSIONS

In this work, a multi-channel GAA MOSFET structure is introduced, and device performance is investigated extensively. The analysis is further extended to study the effect of the distance between the channels, which was taken equal to 6, 9 and 10 nm. An improved

value of on-current by 28.9 % for SS of 70.34 mV/dec is achieved for a separation of 10 nm. However, a switching ratio of 9.13e+08 is obtained for a separation of 6 nm at a gate voltage of 1 V and 1.27e+09 at a gate voltage of 1.5 V. This analysis confirmed the effect of channel position on device performance and its correct positioning to obtain a state-of-the-art device for next generation circuit applications.

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Розширене дослідження позиційно-залежного багатоканального GAA MOSFET та його впливу на характеристики пристрою

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У роботі проведено симуляційне дослідження багатоканального польового транзистора з горизонтальним розташуванням каналів та круговим затвором (GAA MOSFET) з розрахунком розділення каналів. Моделювання виконується у низько-технологічних вузлах з урахуванням квантового ефекту. Ізолятор, який використовується в розглянутій моделі, є high-k діелектриком, що дозволяє зменшити масштаб пристрою. Детально досліджуються розділення кремнієвих каналів та його вплив на характеристики пристрою. Отримані таким чином характеристики, а саме струм стоку (I_D), порогова напруга (V_{th}), крутизна (g_m) та коефіцієнт перемикання (I_{on}/I_{off}), порівнюються для різних розділень каналів. Крім того, детально вивчається струм витоку та пов'язаний з ним короткоканальний ефект, такий як підпорогове коливання (SS), та його залежність від розділення каналів. Покращене на 28,9 % значення струму включення при SS, рівному 70,34 мВ/дек, досягається для розділення каналів в 10 нм. Однак коефіцієнт перемикання 9,13e+08 отримано для розділення в 6 нм, що порівняно вище, ніж для розділення в 9 і 10 нм.

Ключові слова: GAA, High-k, Струм витоку, Підпорогове коливання, Квантовий.