JOURNAL OF NANO- AND ELECTRONIC PHYSICS
Vol. **14** No 1, 01023(4pp) (2022)
ЖУРНАЛ НАНО- ТА ЕЛЕКТРОННОЇ ФІЗИКИ
Том **14** № 1, 01023(4cc) (2022)

1064 nm Wavelength *p*-i-*n* Photodiode with Low Influence of Periphery on Dark Currents

M.S. Kukurudziak*

Rhythm Optoelectronics Shareholding Company, 244 Holovna St., 58032 Chernivtsi, Ukraine

(Received 04 January 2022; revised manuscript received 20 February 2022; published online 28 February 2022)

In the process of carrying out various studies, the problem of an uncontrolled increase in the dark current level of guard-ring photodiodes is observed, being manifested both at a temperature $T = 293$ K and (largely) when testing devices at elevated temperature ($T = 358$ K). As it is known, microelectronics technology always uses surface protection (passivation) of semiconductor devices and integrated circuits. In this case, the best solution is a thermally grown SiO_2 layer. However, even a surface protected by a dielectric layer does not always remain stable. The article presents the results of the development of a *p*-i-*n* photodiode based on high-resistivity *p*-type silicon of increased responsivity and reduced dark current level of the guard ring at a wavelength of 1064 nm. In the proposed design of the photodiode, the thickness of the peripheral oxide of the crystal is decreased to reduce the influence of the dislocation component of the current and charge states on the inverse characteristics. After phosphorus diffusion (driving-in), phosphorosilicate glass was removed, and additional photolithography was performed, during which the entire layer of peripheral oxide was etched. In the second stage of phosphorus diffusion (distillation), the antireflection oxide 190-220 nm thick was grown in photosensitive areas and at the periphery of the crystal. The photosensitive areas, the guard ring, and the peripheral part of the crystal were separated by an oxide 650-700 nm thick grown in the first thermal operation. The production of photodiodes was performed using the same operating conditions as in commercial production, and their parameters were compared with devices manufactured in a standard design. The analysis showed that the photodiodes of the proposed design are characterized by lower and more stable dark currents than commercial devices not only at room temperature, but also at a temperature of 358 K.

Keywords: Photodiode, Silicon, Dark current, Guard ring, Periphery, Responsivity.

DOI: 10.21272/jnep.14(1).01023 PACS numbers: 85.60.Dw, 89.20.Bb

1. INTRODUCTION

With due regard for increasing market demand for photodiodes (PDs) of increased current monochromatic responsivity, Rhythm Optoelectronics Shareholding Company deals with solving technical and technological problems in the field. To provide maximum responsivity and minimum capacitance of PDs, *p*-type silicon of resistivity $\rho \approx 16\text{-}20$ kOhm/cm and minority carrier lifetime $\tau \approx 1400\text{-}1800$ μs is used.

In the course of the research, an uncontrolled increase in the dark current of guard-ring (GR) PDs was observed, which manifested itself both at a temperature $T = 293$ K and (to a large extent) during tests at elevated temperature $T = 358$ K. In some cases, there was an increase in the GR current (I_r) more than 52 μA/mm^2. In the production of low-voltage PDs and PDs not intended to achieve high responsivity, the phenomenon is not observed or manifested to a lesser extent. After all, it is inexpedient to use such a high-resistivity material to make devices of the kind. In this case, to ensure the parameters of the devices, the optimal resistance of silicon is 10-14 kOhm/cm. Evidently, the mentioned phenomena can be explained by the fact that a lower concentration of defects or impurity ions is required to change the reversed characteristics of the required device made on the basis of high-resistivity silicon.

The mechanisms of such a growth of dark currents in semiconductor devices are known, these are defects created during the production of devices, influence of the periphery of the crystal, moisture on the surface of a semiconductor, charge states (fixed and mobile charges) in the oxide or at the silicon/silicon oxide (Si/SiO_2) interface, in particular [1, 2].

The presence of defects is minimized by chemical and dynamic polishing of both the front and back sides of semiconductor wafers and adherence to the technology that ensures the creation of a high-quality surface of crystals. For instance, a multilayer film of moisture, containing foreign impurities absorbed from etchants and rinsing water, is deposited on the surface of a semiconductor. A significant part of these impurities are positive alkali metal ions. Under the action of a voltage applied to the interface, the ions drift in the film of moisture, thus creating an ion source current, the value of which grows with increasing humidity [3]. The surface leakage current is often the main component of the reverse current through the *p-n* junction. This phenomenon is eliminated by treatment in baths with appropriate solutions of acids and alkalis, drying of crystals or devices in the manufacturing process according to the technology, and in some cases by wiping with distilled acetone.

As it is known, microelectronics technology always uses protection (passivation) surfaces of semiconductor devices and integrated circuits. The best solution in this case is a thermally grown SiO_2 layer. However, even a surface protected by a dielectric layer does not always remain stable [4]. The fact is that in a dielectric, especially in the region of its interface with a semiconductor, there can be inclusions of impurities and their complexes with various structural defects, which usually have an electric charge. Under the influence of elec-

*mykola.kukurudzyak@gmail.com

 © 2022 Sumy State University

tric fields, which always exist in the operating device, it is possible to slowly move these impurities and defect-impurity complexes both deep into the dielectric and to the interface with the semiconductor (or drift to the responsive elements (REs) in the case of localization of these impurities at the periphery of the crystal) [5]. The result is known: a change in the degree and nature of filling the interface and electric fields with electronic states in this area, the drift of the surface potential and related characteristics, the occurrence of local leaks and dielectric breakdown, leading to increased dark currents.

Given the above phenomena, a very important task is to develop a PD of greater stability, without significant loss of responsivity ($S_{I\lambda}$, $S_{pulse} \geq 0.45$ A/W) [6] in commercial production. It is a question of stability of the GR dark current value for a long time, which will not increase both at room temperature and when tested at elevated temperatures.

The purpose of the work was to create and study the design of a four-element segmental PD with decreased peripheral crystal oxide thickness to reduce the influence of the dislocation component of current and charge states on its dark currents of the sensitive areas and GR.

2. PHOTODIODE DESIGN

It is known that an increase in the dark current is mainly due to the dislocation mechanism and the presence of inversion layers near the semiconductor/dielectric interface, which occur due to the presence of a fixed charge in the dielectric. The dark current generation component of *p*-i-*n* PDs can be reduced by coupling dislocations on surfaces that generate them and preventing the movement of current carriers generated on the peripheral part of the substrate and in inversion layers outside the output region of the *p*-*n* junction on the surface of the semiconductor crystal.

This can be realized by creating areas of restriction of loss channels of the same conductivity type as the substrate. These areas isolate the peripheral part of the substrate from the exit point of the *p*-*n* junction to its surface. Creation of such areas of restriction requires the introduction of one more photolithography and two thermal operations, that is, diffusion of boron into the front part of the wafer and distillation of boron, which simultaneously grows SiO_2 oxide to passivate the surface, which significantly increases the cost of devices. In addition, the introduction of additional thermal operations will lead to degradation of the lifetime of minority carriers, and, accordingly, to a decrease in responsivity, which is unacceptable in this case.

We have proposed a much cheaper solution to this problem, implemented in the following design of the PD crystal shown in Fig. 1. In the proposed design of the PD crystal, it was decided to reduce the thickness of the peripheral oxide 2 (outside the GR from the side of the crystal edge) and partially in the interval between the RE and the GR. This oxide is formed by the method of dry oxidation of silicon. After all, according to the standard diffusion-planar technology, during the first thermal operation of oxidation, a layer of masking oxide 3 of about 650-700 nm in thickness is grown.

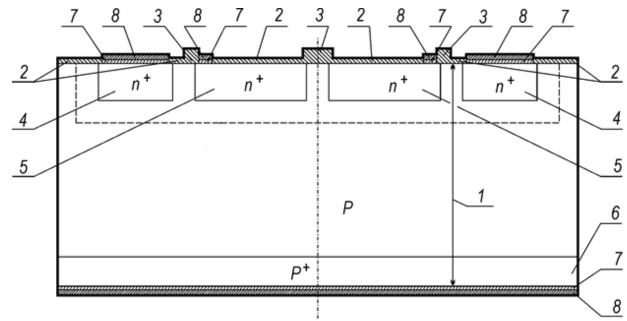

Fig. 1 – Cross-section of the proposed PD crystal: 1 – silicon substrate (*p*-type wafer), 2 – silicon dioxide film 190÷220 nm thick, 3 – silicon dioxide film 650÷700 nm thick, 4 – n^+-type GR, 5 – n^+-type RE, 6 – p^+-type region obtained by boron diffusion, 7 – chromium sublayer, 8 – gold metallization

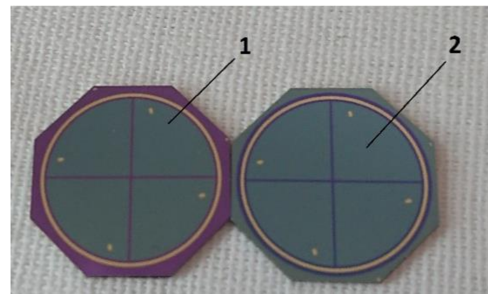

Fig. 2 – PD crystals: 1 – commercial, 2 – proposed

It is known that due to the difference in the coefficients of thermal expansion of Si and SiO_2 on a silicon wafer in the presence of a thick oxide layer, a mechanically stressed layer is formed. And at high temperatures, there is relaxation of mechanical stresses, which leads to the generation of structural defects and, as a consequence, an increase in the generation component of dark currents. In particular, the first thermal oxidation of a total duration of about 180 min is carried out according to the "dry-wet-dry" principle, which increases the probability of introducing alkali metal ions in wet oxidation.

Fig. 2 shows the visual difference between commercial 1 and proposed 2 PD crystals, where the difference in the thicknesses of the peripheral oxide of the two devices is clearly visible, as well as the same thickness of the peripheral oxide and the illuminated PD in the proposed crystal.

The given design of the device is realized only when using two-stage phosphorus diffusion. Therefore, after phosphorus diffusion (driving-in), phosphorosilicate glass in a solution of $HF:H_2O = 1:10$ was removed and additional photolithography was performed, during which the entire peripheral oxide layer was etched. In the second stage of phosphorus diffusion (distillation), the antireflection oxide $d \approx 190$-220 nm thick was grown in sensitive areas and at the periphery of the crystal. The sensitive areas, the GR, and the peripheral part of the crystal were separated by an oxide $d \approx 650$-700 nm thick grown in the first thermal operation (oxidation) [7]. Reducing the thickness of this passivation coating resulted in a decrease in the resistance of the interconnection and, as a consequence, in breakdown at low voltages.

The thickness of the antireflection coating was chosen to provide the maximum transmittance of yttrium-aluminum garnet laser radiation, at the wavelength of which the investigated PDs operate (λ_p = 1064 nm). The optimal oxide thickness can be found from the formula that determines the condition of the minimum reflection of optical radiation of the operating wavelength [8]:

$$\lambda_{op}/4 = nd,$$

where nd is the optical thickness of an antireflection film with thickness d and refractive index n.

For SiO_2 n = 1.42, then for the given value of λ_{op} we obtain d = 187 nm.

3. RESULTS AND DISCUSSION

The production of PDs was performed under the same operating conditions as in commercial production, and their parameters were compared with devices manufactured in a standard design (Table 1). It should be noted that both series of PDs are suitable for operation according to the specifications for these products.

As seen from the data in Table 1, there is a slight decrease in the coupling resistance R_{rev} at room temperature for commercial products, which can give rise to uncontrolled growth of I_r, breakdown or deterioration of photoelectric coupling between REs. This is due to the above mechanisms, which are manifested in this case even at T = 293 K. When testing commercial PDs at T = 358 K, there was a significant increase in the dark currents of GR at a rate of 20 μA/min, which indicated temperature drift of current carriers generated at defects and dislocations of the peripheral part of the substrate and in inversion layers outside the output region of the p-n junction on the crystal surface. Such phenomena were not observed in the experimental samples. New devices have much lower values of dark currents I_d and I_r, since they do not have a thick oxide, which is the main generator of mechanical stresses (and, accordingly, structural defects) in the wafer and the source of charge states. The thickness of the antireflection peripheral oxide on the front side of the wafer grown by distillation of phosphorus is less than usual for masking coatings. As known, mechanical stresses that occur at the Si/SiO_2 interface are proportional to the oxide thickness, and the use of a SiO_2 layer of less than 300 nm thickness makes it possible to avoid the generation of structural defects (dislocations).

Table 1 – Parameters of experimental (PD-E) and commercial (PD-C) PDs

Parameter	Parameter value	
	PD-E	PD-C
Dark current of the RE, I_d, A/mm^2	0.0023-0.0031	0.0052-0.0104
Dark current of the GR, I_r, μA/mm^2	0.41-0.3	0.243-0.74
The total coupling resistance between all REs and the GR at $R_l = 10^4$ Ohm, $\sum R_{rev}$, Ohm	20-15	5-2↓
Dark current of the RE at T = 358 K, $I_d^{(358\ K)}$, μA/mm^2	0.234-0.322	0.65-0.1
Dark current of the GR at T = 358 K, $I_r^{(358\ K)}$, μA/mm^2	12.23-14.24	16.84-26.34↑
Pulse monochromatic responsivity at λ_{op} = 1.064 μm, pulse duration τ_{pulse} = 500 ns, operating voltage U_{op} = 120 V, S_{pulse}, A/W	0.46-0.48	0.46-0.48
Monochromatic responsivity at modulated radiant flux of f_{mod} = 20 kHz at λ_{op} = 1.06 μm and U_{op} = 31 V, $S_{I\lambda}$, A/W	0.45-0.47	0.45-0.47
Capacitance of the RE, C_{RE}, pF	11.9-12.2	12-13

Note. Parameters were monitored in accordance with GOST 1772-88 under the condition of observing dark current measurements for 1 min to detect uncontrolled growth and instability of I_g levels. Cases of continued rise or fall of PD parameters at the end of the specified time are indicated by arrows.

4. CONCLUSIONS

PDs with reduced values of dark currents of the GR and sensitive areas have been created. Experimental verification confirmed the initial assumptions, and it was possible to minimize the influence of generation components on the inverse characteristics of the devices by reducing the thickness of the peripheral oxide. PDs of the proposed design are characterized by lower and more stable, in comparison with commercial devices, dark currents both at room temperature and at a temperature of 358 K. The proposed design largely reduces the dislocation component of dark currents. Also, to reduce the impact of the component caused by the charge states, it is possible to effectively use areas of restriction of loss channels of the same conductivity type as the substrate to the material of the semiconductor substrate, although this will slightly increase the cost of devices and reduce responsivity due to the introduction of additional thermal operations.

Thus, the introduction of one additional photolithography slightly complicated the manufacturing technology of PDs and, accordingly, slightly increased their cost, but at the same time allowed to reduce the dislocation component and the component caused by the charge states of the dark current.

REFERENCES

1. O.V. Aleksandrov, A.I. Dus, *Semiconductors* **45**, 467 (2011).
2. S. Zafar, A. Callegari, V. Narayanan, S. Guha S., *Appl. Phys. Lett.* **81**, 2608 (2002).
3. Yasuhiro Ebihara, Kenta Chokawa, Shigenori Kato, Katsumasa Kamiya, Kenji Shiraishi, *Appl. Phys. Lett.* **100**, 212110 (2012).

4. D.R. Islamov, V.A. Gritsenko, T.V. Perevalov, O.M. Orlov, G.Y. Krasnikov, *Appl. Phys. Lett.* **109**, 052901 (2016).
5. Yu.B. Zolochevsky, V.P. Romanov, A.Yu. Sokolov, *Int. J. Appl. Fund. Res.* **6-4**, 651 (2016) [in Russian].
6. M.S. Kukurudziak, O.P. Andreeva, V.M. Lipka, *Tekhnologiya i Konstruirovanie v Elektronnoi Apparature,* **5-6**, 16 (2020).
7. Method of manufacturing a crystal of silicon p-i-n photodiode: pat. 149108 Ukraine: H01L31/00/ M. C. Kukurudziak, V.M. Lipka, O. B. Shimanovskiy. – № u202101103; stated 05.03.2021; published 20.10.2021, bulletin № 42/2021. – 5 p.
8. M.S. Kukurudziak, Yu.G. Dobrovolsky, *Technology and design in electronic equipment.* **1-2**, 61 (2021) [in Ukrainian].

***p*-i-*n* фотодіод на довжині хвилі 1064 нм із низьким рівнем впливу периферії на темнові струми**

М.С. Кукурудзяк

ЦКБ «Ритм», вул. Головна, 244, 58032 Чернівці, Україна

В процесі проведення досліджень помічено проблему неконтрольованого зростання рівня темнового струму охоронного кільця фотодіодів, що проявлялось як за температури $T = 293$ К, так і (значною мірою) при випробуванні приладів за підвищеної температури ($T = 358$ К). У статті представлено результати розробки *p*-i-*n* фотодіода на основі високоомного кремнію *p*-типу провідності з підвищеною чутливістю та пониженим рівнем темнового струму охоронного кільця на довжині хвилі 1064 нм. У пропонованій конструкції фотодіода зменшено товщину периферійного оксиду кристалу для зниження впливу дислокаційної складової струму та зарядових станів на зворотні характеристики. Для реалізації розробленої конструкції приладу використовується двохстадійна дифузія фосфору. Після дифузії (загонки) фосфора знімалося фосфоросилікатне скло і проводилася додаткова фотолітографія, під час якої стравлювався весь шар периферійного оксиду та частини окислу між ОК та ФЧЕ. На другій стадії дифузії фосфора (розгонці) вирощувався просвітлюючий оксид товщиною 190-220 нм на фоточутливих площадках і на периферії кристалу. Фоточутливі площадки, охоронне кільце та периферійна частина кристалу відмежовувались оксидом товщиною 650-700 нм, вирощеним на першій операції. Виготовлення фотодіодів виконувалося з використанням таких режимів технологічних процесів, як і у серійному виробництві, а їхні параметри порівнювались із приладами, виготовленими в стандартній конструкції. Аналіз показав, що фотодіоди запропонованої конструкції характеризуються нижчими та стабільнішими, ніж серійні прилади, темновими струмами ОК та ФЧЕ, причому не тільки за кімнатної температури, але й за температури 358 К.

Ключові слова: Фотодіод, Кремній, Темновий струм, Охоронне кільце, Фоточутлвий елемент, Периферія, Чутливість.