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Electrical and Temperature Characteristics of Transistors with a Channel in the Form of a Carbon Nanotube

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Carbon nanotubes (CNTs) are promising materials for the formation of field-effect transistors (FETs) due to their excellent electrical, thermal, mechanical and other properties. High productivity, low power consumption, minimization of the impact of short-channel effects, etc., are of significant practical interest primarily to coaxial CNTFETs. This paper presents the results of numerical simulation of coaxial gate-all-around (GAA) CNTFETs. The structure of GAA CNTFETs is designed using Silvaco TCAD tools and their electrical parameters are investigated. The drift diffusion model of transport, taking into account the Bohm quantum potential, demonstrates excellent characteristics for three-dimensional models, in particular, valid values are obtained for the threshold voltage V_t, subthreshold swing SS, switching current I_{on}, leakage current I_{off} and I_{on}/I_{off} coefficient. The influence of temperature on the specified electrical parameters at low bias voltages is studied and the typical character of temperature dependences for semiconductor devices is obtained. It is established that the values of the threshold voltage V_t and subthreshold swing SS decrease and increase, respectively, with increasing temperature from 250 to 500 K. Along with this, there is a slight decrease in the switching current by 1.6 % in a given temperature range at the source voltage $V_{DD} = -1.0$ V. The thermal stability of coaxial structures of nanotransistors with a channel in the form of a single-walled CNT is evaluated by the temperature coefficients β_{V_t}, β_{SS}, $\beta_{I_{on}}$ and $\beta_{I_{off}}$, which at $V_{DS} = 0.10$ V are respectively $3.2 \cdot 10^{-4}$ K^{-1}, $3.2 \cdot 10^{-3}$ K^{-1}, $-6.2 \cdot 10^{-5}$ K^{-1} and $1.0 \cdot 10^{-4}$ K^{-1}.

Keywords: GAA CNTFET, Modeling, Simulation, Temperature coefficients of electrical parameters.

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1. INTRODUCTION

The development of modern microelectronics is associated with the introduction and use of new functional nanoscale materials in the form of multicomponent and granular films based on metals and semiconductors, multilayer film materials, high-entropy alloys, etc. Field-effect transistors (FETs) are the basic active elements of integrated circuits, in which the channel can be nanowires or nanotubes, which increases the efficiency of their parameters in terms of thermal stability and performance. Devices and equipment based on chips with FETs are widely used in sensor electronics, wave optics and medicine [1-3].

Carbon nanotube (CNT) is a graphene sheet folded in a certain direction – the chirality of the nanotube. Depending on the chirality indices (n, m), CNTs can be made either leading if ($n - m$) is divisible by 3 or semiconductor if ($n - m$) is not divisible by 3. According to the chirality indices, typical CNT structures are distinguished: normal (n, m), "chair" (n, n) and "zigzag" (n, 0). CNT semiconductors with the same chirality have the same state density and similar properties. In addition, the geometry of CNTs has a significant effect on the transport of charge carriers [4-8]. CNT diameters can be in a wide range of values from units to hundreds of nanometers. On the one hand, CNTs become more conductive with increasing diameter; on the other hand, this worsens the controllability of the gate. In addition, this increases the leakage current and, consequently, the power consumption, also reduces the band gap and reduces the threshold voltage of the transistor [4-10]. This significantly further affects the electrical characteristics of FETs. Along with this, the peculiarities of the transport of charge carriers in such devices can be manifested by changes in the conditions of their operation (changes in temperature, strain, etc.).

In [4-6], planar and coaxial FETs with a channel in the form of CNTs were studied. The influence of source/drain doping and chirality on the leakage current, volt-ampere characteristics was considered. In addition, an analysis was made of the effect of CNT length and gate thickness on the volt-ampere characteristics, as well as the effect of high-k materials on these characteristics. It was shown that the leakage current increases with decreasing CNT length. Along with this, the optimal value of the gate width of 5 nm was obtained in [5]. It was noted that the electrical parameters for such transistors were much better than those of similar ones with a gate length of 2 or 3 nm.

In [7], it was noted that FETs with a channel in the form of CNT have significant leakage currents in the off state. This leads not only to an increase in power consumption, but also to potentially incorrect logic functionality. The authors experimentally demonstrated a model with asymmetric valves built on the basis of CNTs. The latter allowed to reduce the leakage current in the off state by more than 60 times at the same bias voltage.

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The work [8] is devoted to the study of electrical conductivity taking into account quantum tunneling in polymer nanocomposites based on single- and double-walled CNTs with different chirality. The uncertainty of geometric parameters and intersection points of the latter was modeled by the Monte Carlo method. It was shown that tunneling effects are most evident for short single- and double-walled CNTs. For longer single-walled CNTs and networks based on them, tunneling effects play a minor role that can be neglected.

The authors of [10] designed a FET with a tunnel channel in the form of a CNT with the so-called electrostatic doping (ED-Tunnel CNTFET). Additional electrodes around the source and drain replaced the corresponding doping with impurities in these areas. This avoided problems associated with low Fermi levels, impurity deactivation, etc. and improved productivity.

In addition, in our works [10-12], the materials of transistor electrodes were analyzed in many aspects – from their manufacturing technology, structure, and electrophysical properties to the distribution of individual components in the gate in terms of effective output, and so on.

The aim of this work was to numerically model the structure and electrical parameters of an *n*-type coaxial FET with channels in the form of single-walled CNTs.

2. NUMERICAL SIMULATION PROCEDURE

Technology Computer-Aided Design (TCAD) software is widely used to design semiconductor devices. It usually consists of two parts, the first of which allows you to describe and simulate the technological process of structure formation, and the second – to model its electrophysical properties.

TCAD Silvaco was used in [13, 14]. According to the initial data, the structure of the device was designed (basic areas, functional materials, doping with impurities, etc. were determined). Next, the selection of transport models was made and test volt-ampere characteristics were obtained. After that, the parameters of the structure, material characteristics, coefficients for transport models were specified.

As in our previous work on modeling cylindrical devices, their general geometry was created by means of the `mesh cylindrical three.d` operator, where the parameter `cylindrical` allowed to set the radius, angle and *Z*-coordinates, parameter `three.d` informed that a 3D mesh was created. The features of charge transport were determined using the `models fermi bqp.n SRH ni.fermi bqp.ngamma=1.089 bqp.nalpha=0.5 evsatmod=1 fldmob print bqp.qdir=3 temp=300`. The parameter `fermi` made it possible to take into consideration the drift-diffusion transport of charges within the framework of Fermi-Dirac statistics. The parameter `srh` allowed to take into account Shockley-Read-Hall recombination mechanisms, `bqp.n` determines the Bohm quantum potential for electrons, etc. [4, 15-19].

As known, ATLAS software from Silvaco TCAD includes a drift-diffusion transport model and advanced quantum models. Along with this, quantum effects are included in ATLAS by changing the equations of transport models. In particular, Bohm quantum potential can be considered [1, 13]. In this case, the current equations for 3D channels will look like [4]:

$$\boldsymbol{J_n} = qD_n\nabla n - \bar{q}n\mu_n\nabla(\psi - Q) - \bar{\mu}_n n\left(kT\nabla\left(ln n_{ie}\right)\right), \quad (2.1)$$

$$\boldsymbol{J_p} = -qD_p\nabla p - \bar{q}p\mu_p\nabla(\psi - Q) + \mu_p p\left(kT\nabla\left(ln n_{ie}\right)\right), \quad (2.2)$$

where q is the electron charge, D_n and D_p are the diffusion coefficients for electrons and holes, n and p are the concentrations of electrons and holes, μ_n and μ_p are the mobilities of electrons and holes, respectively, ψ is the wave function, Q is the Bohm quantum potential, k is the Boltzmann constant, T is the Debye temperature, and is the effective internal concentration.

Equations for the diffusion coefficients in terms of Fermi-Dirac statistics for electrons (similar expressions are used for holes):

$$\bar{D} = \frac{\left(\frac{kT_L}{q}\mu_n\right)F_{1/2\left\{\frac{1}{kT_L}\left[\varepsilon_{F_n}-\varepsilon_c\right]\right\}}}{F_{-1/2}\left\{\frac{1}{kT_L}\left[\varepsilon_{F_n}-\varepsilon_c\right]\right\}}, \quad (2.3)$$

$$\bar{\varepsilon}_{F_n} = -q\phi_n = \bar{\psi} - \frac{kT_L}{q}\ln\left(\frac{n}{n_{ie}}\right),$$

where F_a, ε_c, ε_{Fn}, ϕ_n and n_{ie} are the Fermi-Dirac integral of order a, conduction band energy, quasi-Fermi level, quasi-Fermi potential and effective intrinsic carrier concentration, respectively.

It should be noted that online resources NanoHUB and others are widely used and freely distributed for the design of planar and coaxial structures of FETs with a channel in the form of CNTs and others. They are based on the ability to model nanoscale electronic devices, which is implemented by finding solutions to systems of Poisson and Schrödinger equations within the Non-Equilibrium Green Function (NEGF) approach. A 3D model is used to solve the Poisson equation that connects charges and potentials inside the channel of the device, and a mesh is built around each atom of the structure. The 2D Schrödinger function determines the possibility of finding the charge carrier in the channel sections, and transport is taken into account by a 1D equation [16-19]. In addition, within the Landauer-Büttiker formalism (ballistic transport), the current of 1D channels is determined by the relation [5]:

$$\bar{I}_{DS}\left(V_{DS}, V_{GS}\right) = \\ = \frac{2q}{h}\int_{-\infty}^{+\infty}\left\{T\left(E, V_{DS}, V_{GS}\right)\left[f_S\left(E - E_{FS}\right)\right] - \bar{f}_D\left[E - E_{FD}\right]\right\}dE, \quad (2.4)$$

where $T(E, V_{DS}, V_{GS})$ is the transmission coefficient, E_{FS} and E_{FD} are the source and drain Fermi levels, $f_S(E, E_{FS})$ and $f_S(E, E_{FD})$ are the source and drain Fermi-Dirac functions, respectively.

3. DEVICE STRUCTURE

The results of modeling the coaxial structures of FETs with a channel in the form of CNTs are presented in this part of the work. The input data for GAA CNTFET modeling are taken from [1-3] and Silvaco TCAD libraries [13].

The GAA CNTFET gate was separated from the channel by insulating layers of HfO_2 and SiO_2; Pd was used as the material of the source and drain electrodes located at the ends (Fig. 1a). The channel had the form of a single-walled CNT (Fig. 1b).

a b

Fig. 1 – 3D structure of GAA CNTFET (a) and a separate display of its channel and gate (b)

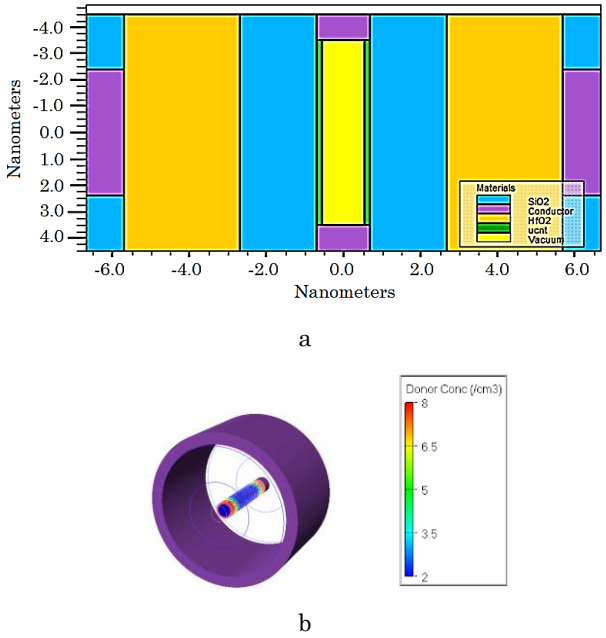
Table 1 shows the simulation parameters. The effective output for the Pd gate was 5.22 eV [1]. HfO_2 ($k = 25$) with a thickness of 3 nm was taken as the high-k dielectric, and the SiO_2 ($k = 3.9$) barrier layer under the high-k dielectric was 2 nm thick.

Table 1 – Various parameters used for modeling and simulation of the CNTFET device with surround gate geometry

Device parameters	Symbol	Values
CNT chirality	$Ch(n, m)$	(6, 2)
CNT diameter	D_{CNT}	1.41 nm
Channel length	L	7 nm
Band gap	E_g	0.61 eV
Density of states in CB	DOS (N_C)	8.88e20
Density of states in VB	DOS (N_V)	7.36e20
Inner oxide thickness (SiO_2)	T_{oxi}	2 nm
Inner oxide dielectric constant	K_{oxi}	3.9
Stacked outer gate oxide (HfO_2) thickness	T_{oxt}	3 nm
Stacked outer gate oxide (HfO_2) dielectric constant	K_{oxt}	25
Source/drain doping	N_{SD}	10^8 cm^{-3}
CNT dielectric constant	K_{CNT}	1
Electron affinity	E_{ea}	3.2 eV
Metal gate work function	Φ_m	5.22 eV
Permittivity	e	9.7 Fm^{-1}
Mobility of electrons	μ_n	$8.0 \cdot 10^4$ cm^2/V · s
Mobility of holes	μ_p	$7.8 \cdot 10^4$ cm^2/V · s

The geometry and dimensions of the main elements of the studied structure of GAA CNTFET are given in Fig. 2a. A CNT of a typical chiral structure with a channel diameter of 1.41 nm was chosen as the transistor channel. The gate was 5 nm long.

Note that the impurity concentration distribution in the induced n-type transistor channel was taken from the data of [5, 6], where a donor impurity with a concentration of 10^8 cm^{-3} is introduced into the contact areas of the source and drain. The configuration of the channel doping profiles, which was used in this design, is shown in Fig. 2b.



a

b

Fig. 2 – Structure of GAA CNTFET: a – 2D structure of GAA CNTFET with channel and gate lengths of 7 nm and 5 nm, respectively; b – 3D structure of GAA CNTFET with impurity concentration distribution in the channel

It should be noted that coaxial geometry of CNTFETs is considered more productive [4, 5] than planar [6]. In the latter, both a horizontal metal electrode and an additionally doped silicon substrate under the insulating layer can be used as a gate.

4. SIMULATION AND RESULTS

Fig. 3a shows typical I_{DS}-V_{DS} output characteristics for the studied FET geometry at fixed values of the gate voltage V_{GS} from – 1.0 to 1.0 V. The operating temperature range was from 250 to 500 K. Typical I_{DS}-V_{GS} transmission characteristics for fixed values $V_{DS} = 0.05$ V and $V_{DS} = 0.10$ V in the temperature range from 250 to 500 K are shown in Fig. 3b.

The main electrical parameters were determined using the ATLAS simulator: threshold voltage V_t, subthreshold swing SS, switching current I_{on}, leakage current I_{off} and I_{on}/I_{off} coefficient (Table 2). As the temperature increases, the values of the threshold voltage and switching current decrease, but the value of the leakage current increases exponentially. Such dependences are considered typical of GAA CNTFETs [21, 22]. It should be noted that GAA CNTFETs are characterized by some peculiarities in determining the studied electrical parameters [7-10].

As an example, the threshold voltage can have different values determined by the values of the work functions of gate materials (channel conductivity type) [10], Schottky barriers at the metal electrode/semiconductor nanotube contact points [23], charges on the oxide surface near the nanotube [6] and other factors.

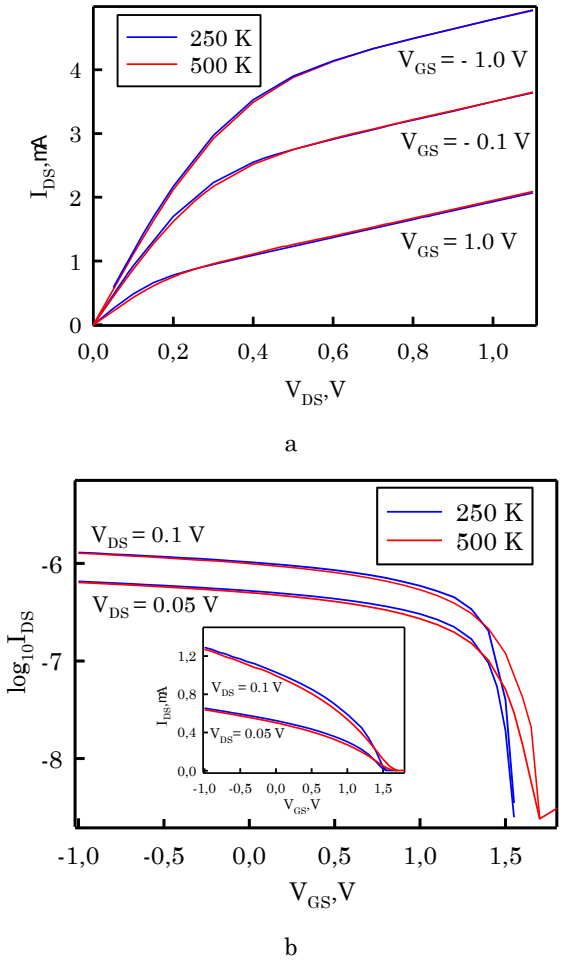


Fig. 3 – I_{DS} (a) and I_{DS}-V_{DS} (b) curves of n-type GAA CNTFET as a function of temperature variation

Table 2 – Parameters used for GAA CNTFET as a function of operating temperature for $V_{DD} = -1.0$ V

Parameters	$V_{DS} = 0.05$ V		$V_{DS} = 0.10$ V	
	250 K	500 K	250 K	500 K
V_t, V	0.26	0.28	0.25	0.27
/SS/, mV/decade	108.24	194.76	101.18	182.45
I_{on}, μA	0.65	0.64	1.29	1.27
$I_{off}\times10^3$, μA	2.85	3.08	3.17	3.25
$(I_{on}/I_{off})\times10^{-4}$	2.28	2.08	6.23	5.64

The values of the temperature coefficients of the threshold voltage β_{V_t}, subthreshold swing β_{SS}, switching current $\beta_{I_{on}}$ and leakage current $\beta_{I_{off}}$ were determined. The working ratios for determining the latter are given by us in [22]. In the temperature range from 250 to 500 K at $V_{DD} = -1.0$ V and $V_{DS} = 0.1$ V we obtained: $\beta_{V_t} = 3.2\cdot10^{-4}$ K^{-1}, $\beta_{SS} = 3.2\cdot10^{-3}$ K^{-1}, $\beta_{I_{on}} = -6.2\cdot10^{-5}$ K^{-1} and $\beta_{I_{off}} = 1.0\cdot10^{-4}$ K^{-1}.

It should be noted that the electrical characteristics were obtained using diffusion equations to describe the ballistic transport of charge carriers [15-20] in FETs with 3D channels and contacts.

In addition, the compact simulation data of GAA CNTFETs indicate high thermal stability of their electrical parameters and the possibility of wide application, although there is a problem of significant leakage current, low reproducibility of parameters in the manufacture of such devices, etc. In terms of heat resistance, the results show an improvement in the performance of CNTFETs compared to FETs with Fin or nanowire channels [23].

5. CONCLUSIONS

The influence of temperature (in the range of 300-400 K) on the volt-ampere characteristics and electrical parameters of the 3D structure of n-type GAA CNTFETs has been studied. The temperature coefficients of current and voltage are estimated. The values of the calculated temperature coefficients agree well with the known experimental data. Coaxial structures of n-type GAA CNTFETs, designed within the framework of the drift-diffusion transport model, taking into account Bohm quantum potential, demonstrate the allowable values of the electrical parameters: threshold voltage V_t, subthreshold swing SS, leakage current I_{off} and I_{on}/I_{off} coefficient. For this reason, the results can be used to further study and predict parameters of modern FETs with vertical gates.

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REFERENCES

1. I. Pazukha, I. Protsenko, *Tech. Phys.* **55** No 4, 571 (2010).
2. L.V. Odnodvorets, I.Yu. Protsenko, O.P. Tkach, Yu.M. Shabelnyk, N.I. Shumakova, *J. Nano- Electron. Phys.* **9** No 2, 02021 (2017).
3. Y. Bereznyak, L. Odnodvorets, Yu. Shabelnyk, L.V. Odnodvorets, I.Yu. Protsenko, *Springer Proceedings in Physics* **210**, 17 (2018).
4. B. Singh, P.B.D. Kumar, *Mater. Res. Express.* **7**, 015916 (2020).
5. L. Xu, J. Yang, C. Qiu, S. Liu, W. Zhou, Q. Li, B. Shi, J. Ma, C. Yang, J. Lu, Z. Zhang, *ACS Appl. Mater. Interfaces* **13**, 31957 (2021).
6. Q. Cao, S. Han, A.V. Penumatcha, M. M. Frank, G.S. Tulevski, J. Tersoff, W. E. Haensch, *ACS Nano* **9** No 2, 1936 (2015).
7. T. Srimani, G. Hills, X. Zhao, D. Antoniadis, J.A. del Alamo, M.M. Shulaker, *Appl. Phys. Lett.* **115**, 063107 (2019).
8. J.Doh, S.-I.Park, Q.Yang, N.Raghavan, *Nanotechnology* **30**, 465701 (2019).
9. S. Bala, M. Khosla, *Superlatt. Microst.* **124**, 160 (2018).
10. D. Zhong, C. Zhao, L. Liu, Z. Zhang, L.-M.Peng, *Appl. Phys. Lett.* **112**, 153109 (2018).
11. I.P. Buryk, A.O. Holovnia, M.M. Ivashchenko, L.V. Odnodvorets, *J. Nano- Electron. Phys.* **12** No 3, 03005 (2020).
12. I.P. Buryk, T.M. Hrychanovs'ka, D.V. Poduremne, A.O. Stepanenko, *J. Nano- Electron. Phys.* **10** No 5, 05026 (2018).
13. T.M. Grychanovs'ka, V.V. Bibyk, I.P. Buryk, O.S. Gryschuk, L.A. Sheshenya, *J. Nano- Electron. Phys.* **5** No 1, 01014 (2013).
14. Silvaco, *ATLAS User's Manual Device Simulation Software* (Santa Clara CA: Silvaco International: 2018).
15. G. Iannaccone, G. Curatola, G. Fiori, *SISPAD 2004* **2004,** 275 (2004).

16. S. Datta, *Lessons from Nanoelectronics. Part A: Basic Concepts* (Singapore: World Scientific: 2017).
17. S. Datta, *Lessons from Nanoelectronics: A New Perspective on Transport – Part B: Quantum Transport* (Singapore: World Scientific: 2018).
18. M. Lundstrom, *Fundamentals of Nanotransistors* (Singapore: World Scientific: 2018).
19. M. Lundstrom, Jung Guo, *Nanoscale Transistors: Physics, Modeling, and Simulations* (New York: Springer: 2006)
20. P. Vimala, L. Krishna, K. Maheshwari, S.S. Sharma, *J. Nano-Electron. Phys.* **12** No 5, 05027 (2020).
21. A. Naderi, S.M. Noorbakhsh, H. Elahipanah, *J. Nanomaterials* **2012**, 532625 (2012).
22. Y. He, J. Zhang, S. Hou, Y. Wang, Z. Yu, *Appl. Phys. Lett.* **94**, 093107 (2009).
23. I.P. Buryk, A.O. Holovnia, I.M. Martynenko, O.P. Tkach, L.V. Odnodvorets, *J. Nano- Electron. Phys.* **13** No 4, 04030 (2021).

Електричні та температурні характеристики транзисторів з каналом у вигляді вуглецевої нанотрубки

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Вуглецеві нанотрубки (CNTs) – перспективні матеріали для формування каналів польових транзисторів (FETs) завдяки їх відмінним електричним, термічним та механічним властивостям. Висока продуктивність, низьке енергоспоживання, мінімізація впливу короткоканальних ефектів обумовлюють значний практичний інтерес насамперед до коаксіальних CNTFETs. У роботі наведені результати числового моделювання коаксіальних структур CNTFETs із затворами типу Gate-all-around (GAA), які були змодельовані з використанням інструментів Silvaco TCAD для дослідження їх електричних параметрів. У рамках дрейф-дифузійної моделі транспорту із врахуванням квантового потенціалу Бома продемонстровано відмінні характеристики для тривимірних моделей, зокрема, отримано допустимі значення порогової напруги, допорогового розсіювання, струму «включення», струму витоку та коефіцієнта підсилення. Досліджено вплив температури на вказані електричні параметри при малих напругах зміщення, отримано типовий характер температурних залежностей для напівпровідникових приладів. Установлено, що величини порогової напруги і допорогового розсіювання зменшуються та збільшуються, відповідно, із зростанням температури від 250 до 500 К. Поряд з цим фіксується незначне спадання струму ввімкнення на 1,6 % у заданому інтервалі температур при напрузі джерела $V_{DD} = -1{,}0$ В. Термічна стійкість транзисторних напівпровідникових структур була оцінена на основі визначених температурних коефіцієнтів β_{V_t}, β_{SS}, $\beta_{I_{on}}$ та $\beta_{I_{off}}$, які при напрузі $V_{DS} = 0{,}10$ В мали значення $3{,}2 \cdot 10^{-4}$ К$^{-1}$, $3{,}2 \cdot 10^{-3}$ К$^{-1}$, $-6{,}2 \cdot 10^{-5}$ К$^{-1}$ та $1{,}0 \cdot 10^{-4}$ К$^{-1}$.

Ключові слова: GAA CNTFET, Моделювання, Симуляція, Температурні коефіцієнти електричних параметрів.