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Modelling and Implementation of Double Gate *n*-channel FET with Strain Engineered Tri-Layered Channel System for Enriched Drain Current

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The strain silicon technology with FET is a dominant technology providing enrichment in carrier velocity in nanoscale devices by engineering the band structure arrangement. Leakage reduction while enhancing drain current is another major objective, therefore the development of a nano-regime double gate FET with a strained channel is perceived. So, implementation of a double gate strained heterostructure on insulator (DG-SHOI) FET with tri-layered channel (s-Si/s-SiGe/s-Si) is the core. Physics of the biaxial strain is studied and generated in the channel by inculcating three layers with optimal thicknesses, while narrow channel depletion regions are strongly controlled by equipotential gates. Consequently, maximum charge carriers accumulate in the channel due to carrier quantum confinement, instigating ballistic transport across the 22 nm channel length device, leading to lessening of intervalley scattering. In comparison to existing 22 nm DGSOI FET, drain current augmentation of 56 % and transconductance amplification of 87.6 % are observed, while DIBL is prudently reduced for this newly designed and implemented DG-SHOI FET, signifying advancement in microelectronic technology.

Keywords: Strain silicon, Carrier quantum confinement, Ballistic transport, Nanoengineering, DG-SHOI FET devices.

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1. INTRODUCTION

Due to shortening of channel length, gate tends to lose its control over the channel and the device, so subthreshold leakage current flows through the device [1-3] prompting abnormality in device performance. Hence, developing vertical FETs in the form of double-gate/tri-gate structures and integrating them with unconventional technologies (SOI, high-k, etc.) are some of the alternatives that researchers are looking for since the last decade for augmentation of device performance at the nanoscale [4, 5]. One of the promising device structures that emerged in nano regime with an additional gate on other side for better control over the channel depletion region employing SOI technology is the double gate silicon-on-insulator (DG SOI) MOSFET, which avoids field penetration from source/drain to the substrate, ensuing reduction in leakage, enriching the output characteristics [6].

DG SOI FET provides superior performance but for devices with L_g at sub-50 nm and beyond the performance worsens due to major short channel effects such as DIBL and punchthrough [7], which leads to the stimulation of quantum tunneling in the nanodevice. Consequently, the strain engineering phenomenon is ordained in device physics.

The concept of strain technology was first incepted in semiconductor physics in 1980s by growing a strain silicon film over relaxed SiGe [8], but then the strain effect was largely overlooked. In 2008, Kumar et al. [9] developed a dual channel-based strain silicon technology device for improved performance at 100 nm channel length. For nanodevices below 100 nm, the mobility becomes field dependent due to an increase in the lateral and vertical electric fields. Thus, velocity saturation and negligible scattering of carriers near the surface strongly influence the mobility and drive current of the device, as observed by Khiangte et al. [10] and Dhar et al. [11]. Thereby, Khiangte et al. [10] developed a tri-layered (s-Si/s-SiGe/s-Si) channel heterostructure on insulator (HOI) planar MOSFET, where the concept of strain channel engineering was employed to modify the band structure, increasing the mobility and drain current. HOI MOSFET incubated ~ 49 % drive current advancement for 40 nm channel length device [11]. On scaling down to $L_g = 30$ nm, HOI MOSFET had to be deformed [11] for enriched performance with allowable short channel effects as per the international technology roadmap for semiconductor (ITRS) 2015 [12]. Hence, further scaling of the gate length is nearly impossible in planar MOSFETs. Henceforth, the development of a novel device with the established HOI system in the vertical form may be a probable solution and is therefore the need of the hour.

Having the concept for inducing strain engineering in the channel region of FET to eliminate quasi-neutral floating body effect in SOI FETs to deepen drain current by quantum carrier confinement and ballistic transport of carriers is the motivation, so employing HOI system in DG structure to develop a novel DG-SHOI FET for the first time with the distinguished tri-layered channel system sandwiched between the two-gates is therefore the focus of this paper.

2. THEORY AND DEVICE STRUCTURE

To develop the proposed structure of the double gate strained heterostructure on insulator (DG-SHOI) n-channel transistor, a detailed theory and understanding of the device need to be established based on the strain

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engineering that is incorporated into the device channel. A schematic three-dimensional (3D) device structure is shown in Fig. 1a, while Fig. 1b provides the cross-sectional view of the channel. The device structure is designed and developed using Sentaurus TCAD employing the parameters and constraints as tabulated in Table 1. The drift diffusion and piezo-resistive coefficient models are combined along with the Shockley Read Hall (SRH) doping dependence parameters, while modelling the device in Sentaurus TCAD. The buried oxide layer is incubated in the device to prevent the penetration path of the electric field from source/drain to the substrate as in the case of SOI MOSFETs, thereby a DG-SHOI structure is modelled and developed.

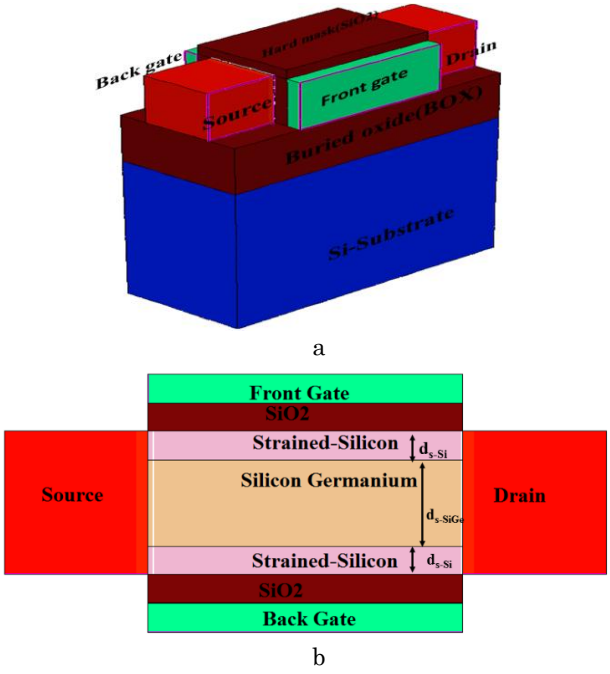


Fig. 1 – Schematic structure of the DG-SHOI FET on 22 nm channel length (a); cross sectional view of the channel region along with source and drain in the DG-SHOI FET (b)

SiO_2 (gate oxide) layers are grown on both sides of the s-Si layer as a hard mask to avoid field penetration from the top, avoiding the formation of additional defects in the structure, which may deform the expected device performance. The strained heterostructure channel forms a tri-layered system consisting of s-Si/s-SiGe/s-Si with 2-6-2 nm thicknesses, nurtured between the front and back gates, as depicted in Fig. 1b. Both gates are symmetrically designed, have the same work function, and are electrostatically coupled. So, a strong electric potential is developed across the channel, effectively controlling source and drain energy barriers for carrier transport with less scattering effect than in planer MOSFETs for $L_g = 30$ nm and beyond that creates a variety of short channel effects [9-11].

Based on the design developed by Harrington et. al. [13], the strain for the proposed DG-SHOI FET device is calculated as:

$$\varepsilon_{strain} = \frac{d_{sub} - d_{ch}}{d_{sub}}, \qquad (1)$$

Table 1 – Double gate SHOI FET with tri-layered channel parameters

Parameters	Dimensions
Channel length (L_g)	22 nm
Channel width (W_{ch})	100 nm
BOX thickness (d_{Box})	1 μm
Ge mole fraction (m_0)	0.4
s-Si layer thickness ($d_{s\text{-}Si}$)	2 nm
s-SiGe layer thickness ($d_{s\text{-}SiGe}$)	6 nm
Gate oxide thickness (d_{ox})	2 nm
Si source and Si drain doping (N_D)	10^{18} cm^{-3}
Channel doping (N_A)	10^{16} cm^{-3}

where d_{sub} and d_{ch} are the substrate and strained channel thicknesses, while d_{ch} comprises of three layers ($d_{s\text{-}Si}$, $d_{s\text{-}SiGe}$, $d_{s\text{-}Si}$), and the thickness of each layer is given in Table 1, so the strain for the entire device is:

$$\varepsilon_{strain} = \frac{d_{soi} - d_{ch}(\varepsilon_{ch-strain})}{d_{soi}}, \qquad (2)$$

where biaxial strain is induced in the channel region as $\varepsilon_{ch\text{-}strain}$ which is a function of d_{ch}. From Eq. (2), the total strain of the device is calculated considering the mismatch strain along with the SOI substrate. $\varepsilon_{ch\text{-}strain}$ is calculated as the sum of the total strain between layers in the channel, and as s-SiGe is 6 nm thick, it equally serves (3 nm each) as the base for both s-Si layers of the device and is calculated as:

$$\varepsilon_{ch-strain} = \sum \frac{d_{s-\mathrm{SiGe}} - d_{s-\mathrm{Si}}}{d_{s-\mathrm{SiGe}}}. \qquad (3)$$

So, the total channel strain ($\varepsilon_{ch\text{-}strain}$) is given by:

$$\varepsilon_{ch-strain} = 2\left(\frac{d_{s-\mathrm{SiGe}} - d_{s-\mathrm{Si}}}{d_{s-\mathrm{SiGe}}}\right). \qquad (4)$$

By substituting $\varepsilon_{ch\text{-}strain}$ into Eq. (2), the total device strain ε_{strain} is achieved for a tri-layered system:

$$\varepsilon_{strain} = \frac{d_{soi}d_{s-\mathrm{SiGe}} - 2\left(d_{s-\mathrm{SiGe}} - d_{s-\mathrm{Si}}\right)}{d_{s-\mathrm{SiGe}}d_{soi}}, \qquad (5)$$

where $d_{s\text{-}Si}$ and $d_{s\text{-}SiGe}$ are different lattice thicknesses in the channel, as shown in Fig. 1b, and d_{soi} is the substrate thickness. On incorporation of this biaxial strain in a strong electric field, a negligible degradation in the mobility of electrons and holes is observed due to the reduction in the effective mass of the material [14]. The valence and conduction band energy level splitting along the channel thickness alters the band structure and can affect the carrier transport phenomenon as the atomic lattice spacing in the region becomes loosely packed in s-Si layers enhancing electron mobility and leading to ballistic transport in nanoscale; an oblivious occurrence with less scattering events [8, 14, 15]. Thereby, with the inclusion of biaxial strain along with the cohort of additional control over the channel in a nanochannel DG-SHOI FET, enhanced carrier mobility is expected, leading to an impact on device performance by enriching the drive current.

3. RESULTS AND DISCUSSION

The novel DG-SHOI FET structure is designed and developed for the first time solving the carrier continuity and Poisson equations simultaneously in both dielectric interfaces, while inducing the solved biaxial strained lattice calculation for the hetero-tri-layered (s-Si/s-SiGe/s-Si) interface along with the 1D Schrödinger equation. The design accuracy is based on the exactness of calculating the threshold voltage of the device. The threshold voltage for the unstrained silicon DG FET is given by [16]:

$$V_{th} = V_{FB} + \varphi_{ms} + V_T ln\left(\frac{Q_{inv}}{n_a d_{ch}}\right), \quad (6)$$

where $V_{FB} = \frac{\varphi_m - \varphi_s}{q}$ is the flat band voltage, φ_m and φ_s are metal and semiconductor work functions, q is the electron charge, φ_{ms} is the gate work function with respect to intrinsic silicon, n_a is the acceptor doping concentration present in the channel, d_{ch} is the silicon channel thickness, V_T is the thermal voltage and Q_{inv} is the inversion charge density of the device. Now for the present DG-SHOI device, the induced biaxial strain parameter developed in Eq. (4) is considered and substituted into Eq. (6) along with the potential work function of hetero-materials in the channel, and finally the threshold voltage, V_{th}, for the DG-SHOI FET is calculated as:

$$V_{th} = V_{s-FB} + \varphi_{ms} + V_T ln\left(\frac{Q_{inv}}{2n_a\left(\frac{d_{s-\mathrm{SiGe}} - d_{s-\mathrm{Si}}}{d_{s-\mathrm{SiGe}}}\right)}\right), \quad (7)$$

where $V_{s-FB} = \frac{\varphi_m - (\varphi_{s-\mathrm{Si}} + \varphi_{s-\mathrm{SiGe}} + \varphi_{s-\mathrm{Si}})}{q}$.

The calculated threshold voltage, V_{th}, and DIBL for DG-SHOI FET is plotted and compared with HOI MOSFET [10] and DGSOI FET [14] devices, as shown in Fig. 2. As evident, V_{th} for 22 nm DG SHOI FET is observed to be less with respect to DGSOI FET, while an enormous reduction of 57.6 % in DIBL is perceived, subsequently authorizing the benefit of engaging the device with strained channel. The V_{th} and DIBL of HOI MOSFET and DG-SHOI FET are found to be similar, which is highly advantageous as the leakage is kept within limits, though the device dimension is scaled drastically from 50 to 22 nm in the gate length, while forming the DG structure. Consequently, these effects are expected to stimulate improvement in mobility of the DG-SHOI FET device.

The increased electron mobility, as seen in Fig. 3a, causes the velocity to reach velocity overshoot condition as observed in Fig. 3b in comparison with 50 nm HOI MOSFET [10]. Fig. 4 clearly depicts the drift velocity variations for three layers of the channel in this novel 22 nm DG-SHOI FET. The maximum number of carriers are confined in the s-Si layers, and relentless electron mobility is observed along the lateral channel direction, as shown in Fig. 3a. Though, mobility enrichment is observed, but in the novel design of DG-SHOI FET, the leakage is within the ITRS 2015 standards [12], as is shown in Fig. 5 in comparison to other existing devices.

The electron and drift velocities are observed along the channel length by applying the gate bias voltage (V_{GS} = 0.28 V) at two gates. The strong inversion layer is developed by coupling two gates at s-SiGe interface

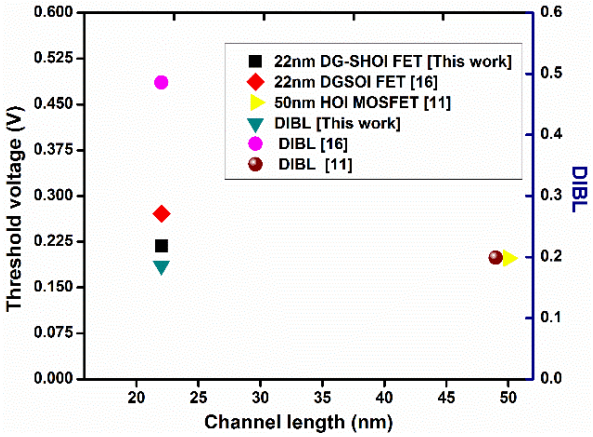
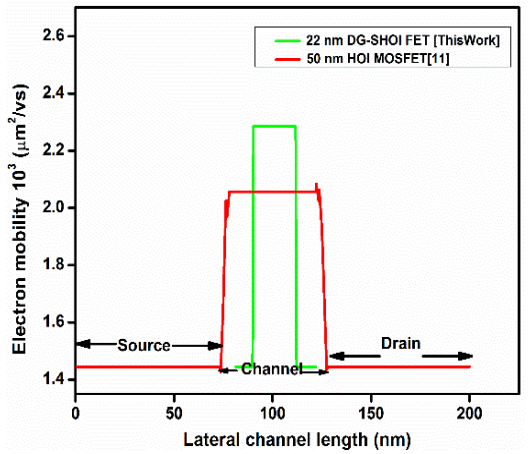
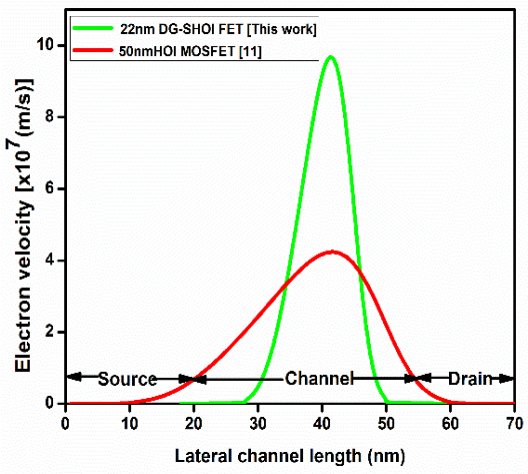


Fig. 2 – Comparison of the threshold voltage and DIBL for DG-SHOI FET, DGSOI FET and HOI MOSFET



a



b

Fig. 3 – Comparison of the electron mobility of DG-SHOI FET on 22 nm channel length with 50 nm HOI MOSFET (a), examination of the electron velocity along the channel length (b)

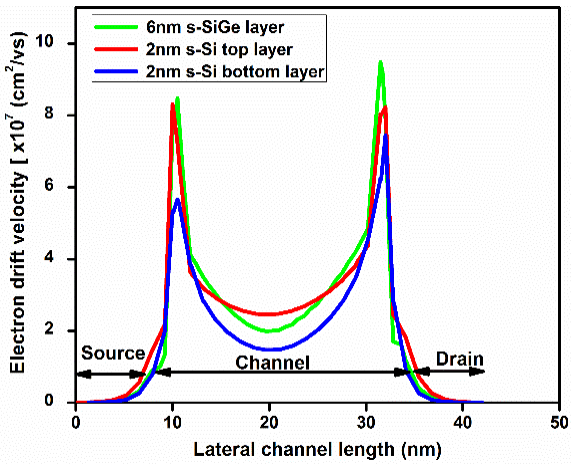


Fig. 4 – Study of the electron drift velocity within three layers (s-Si/s-SiGe/s-Si) in DG-SHOI FET

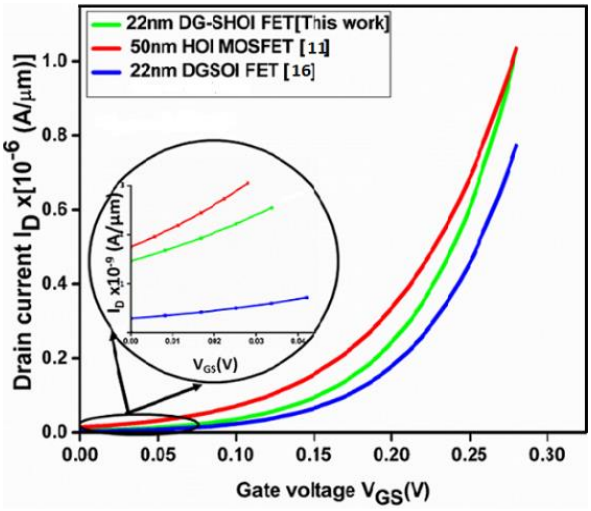


Fig. 5 – I_D-V_{GS} transfer characteristics of DG-SHOI FET compared with HOI MOSFET and DGSOI FET for determining the subthreshold leakage current variation

layer, which is sandwiched between two s-Si layers, so that majority charge carriers reside in the s-SiGe layer and a high electron velocity is observed as shown in Fig. 3b. The maximum charge carriers flow from source towards drain due to extreme drift velocity acquired by electrons as a result of ballistic transport in a short channel (length and width) device, so that less intervalley scattering and a maximum drift velocity (8.0×10^7 cm²/s) are achieved by carriers, as perceived in Fig. 3. The current-voltage transfer characteristics (I_D-V_{GS}) at $V_{DS} = 0.5$ V of a novel 22 nm channel length DG-SHOI FET are analyzed and compared with 50 nm channel length HOI MOSFET [10] and conventional 22 nm DGSOI FET [16] in Fig. 5. It is evident that the HOI MOSFET provides better performance at lower voltage, while at $V_{GS} > 0.28$ V, the current of DG-SHOI FET merges, indicating boosted performance with less scattering and increased mobility, a fact conserved due to quantum carrier confinement and tunnelling effect in the system. The inset of Fig. 5 hence pinpoints a lesser leakage for the present proposed novel device of 22 nm gate length in comparison to the 50 nm HOI MOSFET, though both leakages are within acceptable range as per the ITRS 2015 [12]. This is due to a 10.6 % reduction in threshold voltage roll-off for carrier quantum confinement compiled with the implementation of a narrow channel width in the device.

The low leakage observed for DG-SHOI FET is substantiated by the increase in mobility and is further evidence that excludes the assessment of transconductance ($g_{m(max)}$) to DIBL for FET devices. As the device is detected to have less subthreshold leakage, the transconductance is alleged to maximize for DG-SHOI FET in comparison to other devices at very low DIBL, providing boosted device performance. The improvement in transconductance by 87.6 % for 22 nm channel length DG-SHOI FET creates the velocity overshoot condition with simultaneous decrease in DIBL.

This is a huge gain for the novel DG-SHOI FET with respect to HOI MOSFET [10] that suffers from the trade-off due to short channel effects at nano regime (below $L_g = 50$ nm). The potential barrier lowering exponentially increases the source to drain leakage current; therefore, DIBL becomes a crucial parameter measuring the performance of the device at 22 nm technology node. But, with DIBL reduction and increased transconductance, the 22 nm DG-SHOI FET proves to be quite beneficial, thus providing enhanced carrier mobility due to carrier quantum confinement and ballistic transport across the device, which is overlaid in Fig. 6 with augmented drain current characteristics. These effects and observations are caused by nominal threshold voltage roll-off, and the occurrence of reduced scattering events under the influence of biaxial strain owes to band bending and splitting of conduction band energy levels in the hetero-tri-layered channel structure of the novel device.

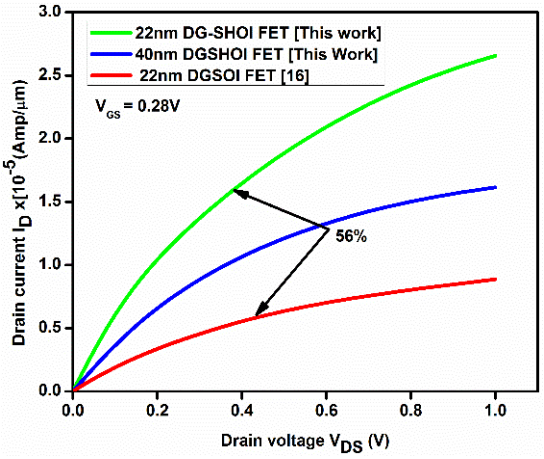


Fig. 6 – I_D-V_{DS} output characteristics of DG-SHOI FET compared with DGSOI FET for drain current, showing 56 % enhancement in device performance

The mobility of charge carries in a strained channel is increased, as well as the drive current which is inversely proportional to the channel length so that the transconductance of DG-SHOI FET increases, while reducing the channel length to 22 nm using the same gate bias (V_{GS}) as on 50 nm HOI MOSFET. As the channel length is reduced to 22 nm, the potential barrier from source to drain is also reduced, so that the threshold voltage of the novel device gets decreased,

minimizing the V_{th} roll off leading to velocity overshoot condition. The change in the threshold voltage at high drain bias (V_{DS}) is measured in terms of DIBL. This clearly indicates low subthreshold leakage and DIBL, thereby contributing to an increase in drain current of the device. The potential barrier of electrons in the depletion region is maintained by the additional gate and minimizes the barrier lowering effect in the device; accordingly subsidizes the reduction in current leakage of the device in comparison to HOI MOSFET.

Hence, the 22 nm DG-SHOI FET proves to be the most beneficial device as it is able to reduce leakage by providing enhanced drain current, as exhibited in Fig. 6, which is directly attributed to the effect of the carrier quantum confinement in a nano regime quantum well-barrier structure developed by the narrow-width channel of the tri-layered channel system, while creating the biaxial strain in the device, thus instigating for improved mobility with velocity overshoot condition, leading to ballistic transport of carriers in a shorter channel.

4. CONCLUSIONS

A novel DG-SHOI FET with 22 nm channel length is developed here for the first time with a nanometer scale channel width of 100 nm. The characteristics of DG-SHOI FET are compared with 22 nm double gate SOI FET (DG SOI FET) and with previously developed 50 nm HOI MOSFET. The device performance is observed to have enriched extensively for drive current by 56 % with an acceptable leakage current of ~ 2 nA. The increased band gap due to strain augments mobility of electrons in the channel region, and a strong inversion layer is developed by placing an additional back-gate, while forming this vertical double-gate structure. Carrier scattering is suppressed by maintaining the equipotential on the two gates and instigating nanoscale ballistic transport. The decline in DIBL, high transconductance (87.6 %), high electron mobility and drift velocity are evidently observed, which enhances the strength of drive current at a threshold voltage of 0.218 V and a minimal threshold voltage roll-off with carrier quantum confinement in a well-barrier channel system of the DG-SHOI FET. This double gate SHOI FET thus has the ability to meet the requirement of minimal leakage due to short channel effects on 22 nm channel length with 100 nm channel width and provides a fast-operating device.

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Моделювання та реалізація *n*-канального польового транзистора з подвійним затвором та тришаровою системою каналів із спроектованою деформацією для збагаченого струму стоку

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Технологія напруженого кремнію з FET є домінуючою технологією, що забезпечує збагачення швидкості носіїв в нанорозмірних пристроях шляхом проектування розташування зонної структури. Зменшення витоку при одночасному збільшенні струму стоку є ще однією важливою метою, тому розглядається розробка FET з подвійним затвором у нанорежимі та з напруженим каналом. Таким чином, основним є реалізація двозатворної напруженої гетероструктури на ізоляторі (DG-SHOI) FET із тришаровим каналом (s-Si/s-SiGe/s-Si). Фізика двовісної деформації вивчається і генерується в каналі шляхом впровадження трьох шарів оптимальної товщини, тоді як вузькі області виснаження каналу суворо контролюються еквіпотенційними затворами. Отже, максимальна кількість носіїв заряду на-

копичується в каналі через квантове утримання носіїв, викликаючи балістичний транспорт через пристрій з довжиною каналу 22 нм, що призводить до зменшення міждолинного розсіювання. У порівнянні з існуючим 22-нм DGSOI FET спостерігається збільшення струму стоку на 56 % і посилення крутості на 87,6 %, у той час як DIBL зменшений для цього нещодавно розробленого та реалізованого DG-SHOI FET, що свідчить про прогрес у технології мікроелектроніки.

Ключові слова: Деформований кремній, Квантове утримання носіїв, Балістичний транспорт, Наноінженерія, DG-SHOI FET пристрої.