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# CMOS Cascode Low Noise Amplifier (CCLNA) Design for Nanosensor Applications

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A design of Cascode Low Noise Amplifier (CCLNA) circuit is proposed using standard 0.18 μm millimeter wave (mmW) CMOS technology. The proposed CMOS CCLNA circuit has achieved a maximum conversion gain of 17.4 dB, NF of dB and a power of 22.3 mW at mmW $K_a$ band. The input and output reflection coefficients are well matched with less than – 10 dB at the $K_a$ band frequency with good Voltage Standing Wave Ratio (VSWR). The reverse transmission coefficient $S_{12}$ is less than – 12 dB, indicating that the LNA has improved isolation between input and output, the stability factor is greater than one for the amplifier realization. The SoC-based CCLNA design for circuit level examination with analytical equations also proved that the simulation outcomes were prone to the design suitable for nanoelectronic applications for an output power of 2 dBm, transition frequency ($f_T$) of 64 GHz and maximum operation frequency ($f_{max}$) of 96 GHz, which significantly shows the efficiency of the proposed method suitable for nanosensor applications. The justification of Radio Detection and Ranging (RADAR) front end simulation performance validates that the receiver designed with proposed LNA is suitable for the receiver design at high mmW frequencies.

**Keywords:** CCLNA, VSWR, RADAR, Conversion gain, CMOS design, Nanosensing, Nanomaterials.

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## 1. INTRODUCTION

Complementary Metal Oxide Semiconductor technology (CMOS) is the most succeed technologies utilized for the execution of Radio Frequency Integrated Circuits (RFICs) because of its inexpensive and its similarity with silicon-based System on Chip (SOC) [1]. LNA include great wide band matching then appear worse noise figure for stated LNA topologies have several noise cancelling techniques [2] issued and proposed the implementation of a fully integrated 2.4 GHz CMOS LNA and its simulation using TSMC factors for 0.18 μm mixed signal improving the impedance matching, improving the reverse isolation and frequency improvement. Ultra-Wide Band (UWB) LNA has been proceeded towards to overwhelm the huge bandwidth. The distributed amplifier delivers wideband-width features, great linearity, and adequate in/output matching conditions [3]. K-band has developed to be very essential to both industry and academe for short-range greater data-rate wireless communications and anti-collision radars [4].

Device and circuit techniques are obtainable which control the limited speed of the transistors while attains the high gain performance with low NF [5], with the illustration of section II the proposed CCLNA topology, section III represents simulation results and discussion. At last Section IV concludes the work. Cadence full analog suite and ADS upgraded version are used for improved accuracy.

## 2. PROPOSED METHODOLOGY AND MATERIALS USED

CCLNA circuit topology is one of the major topologies because of its wide bandwidth and great reverse isolation. A generic amplifier design includes many trades-offs between the performance parameters of gain, NF, linearity etc. The highlights of circuit design techniques and comparison with travelling wave tube amplifier are presented here. Electrical properties are very well enhanced with respect to the Duroid and FR4 material properties which are used in this design with a good aspect ratio of the device emphasized. Thermal properties are very well understood with the conductivity property of silicon-based CMOS devices. The design layout has been showcased in this work.

**Table 1** – Dielectric material characteristics

| Dielectric material | Frequency | Return loss with impedance | Gain with efficiency |
|---|---|---|---|
| FR4 | 20-30 GHz | – 32 dB, 55 Ω | > 10 dB, 61 % |
| RT-duroid | > 30 GHz | – 22 dB, 52 Ω | > 10 dB, 74 % |

Even though, duroid possess good characteristics than FR4, according to the above Table 1 cost is less in FR4. Hence FR4 is suitably chosen for the proposed design, enhancing the performance characteristics.

### 2.1 Circuit Design

The cascode topology is general configurations for LNA design and it was shown in Fig. 1. Its fundamental design is to deliver gain whereas conserve the input signal to noise ratio at output, Cascode LNA core consists of two NMOS transistors $M_1$, $M_2$ with feedback resistor $R_f$ resistive feedback with wideband of 2 GHz is achieved due to $R_f$ and $C_2$in the feedback path, $R_g$ is used in the bias path of $V_{G1}$. The CMOS Cascode LNA topology at the same time NF and input impedance matched, in order to enhance the presentation of a

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Cascode LNA shows improved isolation, enhanced BW and high gain level at milli-meter wave (mmW) frequencies. Therefore, the resistor shunt feedback inclines to be a few hundred ohms that match the low signal source resistance of characteristically 50 Ω, leads to remarkable NF degradation.

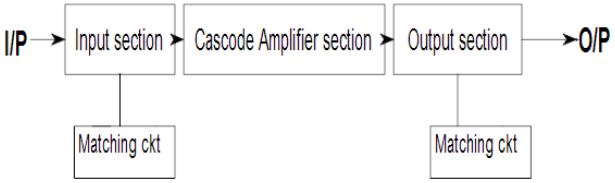


**Fig. 1** – Block description of the proposed CCLNA model

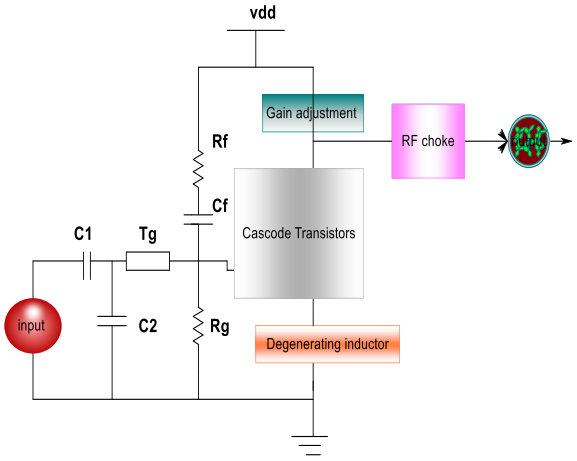


**Fig. 2** – Schematic design of the proposed CCLNA

### 2.2 Design Methodology and Its Implementation

In addition, the power gain starts to roll-off 3 GHz from circuit which confirms that the series inductive peaking method is valuable for increasing BW of the resistive feedback [6]. The expression for input impedance while consider at the gate of $M_1$ was given in Eq. (1). The simplified equation of input impedance is expressed by,

$$Z_{in} = \frac{g_m}{C_{gs}} L , \tag{1}$$

where $g_m$, $C_{gs}$ and $L$ represent the trans-conductance, gate-to-source capacitance, inductance of the $M_1$, respectively.

$$S = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\varepsilon|^2}{2|S_{12}S_{21}|}, \tag{2}$$

where $|\varepsilon| = |S_{11}S_{22} - S_{12}S_{21}|^2$. (3)

For an unreserved stability, the two conditions viz. $K > 1$ and $\varepsilon < 1$, should be satisfied. $K > 1$ and $\varepsilon < 1$ over the required frequency range. To assess the performance of LNAs for their high gain, less NF, low DC power consumption and cut-off frequency. Figure of Merit (FOM) [7] is given by Eq. 5, as shown below,

$$FOM = \frac{S21 \times BW}{(NF - 1) \times Pdc \times ft}. \tag{4}$$

## 3. ARTICLE STRUCTURE AND THE CORRESPONDING STYLES

The proposed Cascode Low noise amplifier is designed and analyzed utilizing Cadence Specter in 180 nm CMOS technology at 28 GHz. The schematic diagram of CMOS Cascode LNA topology was shown in Fig. 1. The simulation setup was shown in Fig. 2. Cascode LNA techniques should keep noise figure, gain and input matching while consuming least power and die area. Proposed CCLNA has been done at millimeter wave (28 GHz) frequency with a low NF. Reverse isolation of LNA is assessment of isolation of intermediate frequency elements entering back into LNA by any feedback network.

**Noise figure and power analysis.** In LNA, the least NF [5] and higher gain are basic execution parameters and low power consumption [6] is also particularly important in portable applications i.e., the lower the value of the noise figures it gives the great performance.

NF is given as

$$NF = 1 + \frac{\left(A_s^2 + \omega^2 C_g^2\right)\gamma g_{d0} R_s}{g_m^2}, \tag{5}$$

where source admittance ($A_s$), source resistance ($R_s$), Technology dependent noise parameter ($\gamma$), gate capacitance ($C_g$), drain-source conductance ($g_d$) at zero $V_{ds}$ and trans-conductance of NMOS transistor ($g_m$). The NF of a system is basically, the noise factor (F) assessed in dB:

$$F_{noise} = \frac{4KTr_g + |B + DR_S|^2 \, 4KT\gamma g_{d0}}{4KTR_S} = \frac{r_g}{R_s} + |B + DR_s|^2 \frac{\gamma g_{d0}}{R_s}, \tag{6a}$$

$$NF = 10\log(F)dB. \tag{6b}$$

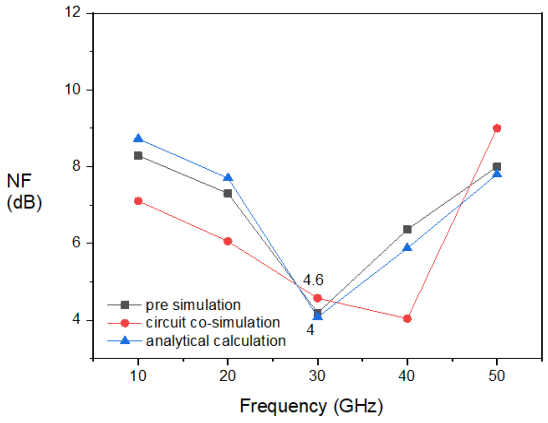


**Fig. 3** – Noise figure analysis

The analysis of NF determines that, as the frequency of operation decreased, the noise figure decreased, and low power consumption obtained the results of NF of 4 dB and power of 22.3 mW was presented in Fig. 3

and Fig. 4 which proves that the proposed circuit has great result with low noise figure with its output voltage compared with earlier reports. Millimeter Wave technology signifies the progress and compensation to the spectrum blockage in the low frequency signals and also provides satisfactory improvement and requirement for higher data rate transmission. New innovative idea with Millimeter Wave Cascode LNA Circuit design is described in this work, while fabricating the design only, manufacturing effects have to be considered. Capacitive cross coupling [8], resistive feed through [9] and transconductance boosted CG topology [10] can be applied to improve the noise reduction techniques.

It is urged in TSMC 90nm standard CMOS process achieves greater than 10dB conversion gain and a 4.0 dB minimum noise figure. The proposed CMOS Cascode mmW LNA circuit and test bench operating at a band of frequencies starting from 24 GHz to 70 GHz is show in Fig. 8. If LNA were not steady, it would turn into ineffective since a main property which includes bandwidth, noise, gain, impedance matching, linearity and low power consumption can be significantly degraded. Conversion gain of Cascode LNA should be more sufficient to decrease the noise offering of successive phases. In addition, the choice of gain leads to a trade-off amongst NF and linearity, as higher gain may saturate successive devices. In LNA, voltage gain ($A_v$) can be expressed by transconductance and resistive factors.

$$|A_v| \sim g_m \times (R_L || R_F), \quad (7)$$

where $g_m$ is the trans-conductance of transistor $M$, load resistances ($R_L$) and feedback shunt resistances ($R_F$) respectively. A 20 GHz low noise amplifier with low DC power consumption and an average output power is forged in a TSMC 0.18 μm standard CMOS process achieves a 9.3 dB conversion gain with 4.4 dB minimum noise figure.

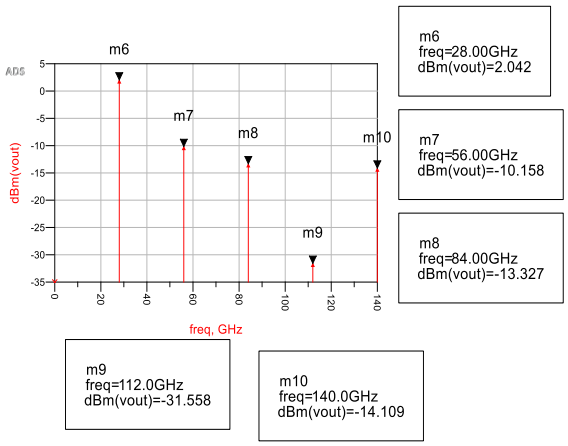


**Fig. 4** – Output voltage

The proposed CCLNA implementation with the analytical versus simulation results are shown in Table 2 and the designed CCLNA concise and differentiation to other CMOS LNAs was listed in Table 3. Fabrication is too costly, for designs implemented at milli-meter Wave frequency hence the analytical and simulation results were compared in this work.

**Table 2** – Analytical versus simulation results of CCLNA

| Proposed CCLNA operating at 28 GHz, $f_T$ (64 GHz) and $f_{Max}$ (90 GHz) | | |
|---|---|---|
| **Parameters** | **Analytical** | **Simulation** |
| Input reflection coefficient $S_{11}$ (dB) | – 11 | – 9 |
| Isolation or Return loss $S_{12}$ (dB) | – 10 | – 0.05 |
| Output reflection coefficient $S_{22}$ (dB) | – 14 | – 10 |
| Stability (dB) | 1 | 1.24 |
| NF (dB) | 3.8 | 4.0 |
| Conversion gain (dB) | 18.4 | 17.4 |

**Table 3** – Analytical versus simulation results of CCLNA

| **Freq. (GHz)** | **Gain (dB)** | **NF (dB)** | **Power (mW)** | **$S_{11}$ (dB)** | **Tech.** | **Ref.** |
|---|---|---|---|---|---|---|
| 49.5-67 | 16.4 | 6.8-9 | 33.6 | < – 10 | 65 nm CMOS | Wu. (2017) |
| DC-50 GHz | 0 | NA | 8 | < – 16 | 180 nm CMOS | Huynh & Nguyen (2016) |
| 22 | 15 | 6 | 24 | < – 12 | 180 nm CMOS | Shin, C. (2005) |
| 20 | 9.3 | 4.4 | NA | < – 12.2 | 130 nm CMOS | Liu et al. (2009) |
| 23 | 9 | 4.5 | 8.7 | < – 12 | 180 nm CMOS | El-Nozahi (2010) |
| **28** | **17.4** | **4** | **22.3** | **< – 12.2** | **180 nm CMOS** | **Proposed CCLNA** |

**Radar front-end simulation.** For the Radio Frequency Front end design of the Radar Receiver, the link budget analysis [11-15] is performed with various blocks like Band Pass Filter, Low Noise Amplifier, and Mixer. In a cascade form, the different blocks were connected. The millimeter Wave Low Noise Amplifier operating at 28 GHz, designed with a gain of greater than 10 dB and Noise figure of 4 dB is tied across the test-bench set up. The system output power is 10.904 dBm with respect to the block diagram illustrating, the budget analysis as shown in Fig. 5. Application of mmW CMOS Low Noise Amplifier to mono-pulse Radar system with respect to system power and gain are justified with the link budget performed with the receiver setup.

The eye diagram of the RADAR receiver is shown in Fig. 6, which is the significance of the amount of signal received without distortions at the higher frequency, pertaining to the amplification process.

**Nanosensor design applications.** The key aspects of the micro/nano satellites are to fulfil the telecommunication transceiver design with the aspect of CCLNA to promise the challenges in gain, noise figure, power consumption and area (dimensions smaller). The novel design approach involved in this design is based on the technology shift to higher frequency bands, with CMOS technology. The designed CCLNA, cater the requirements of small dimensions and power consumption with the power amplifier can be combined for nano sensor for satellite application at the $K_a$ band communication subsystem design. The CCLNA is validated

further by link budget and eye diagram for the aforementioned nano application, with the justification in the output.

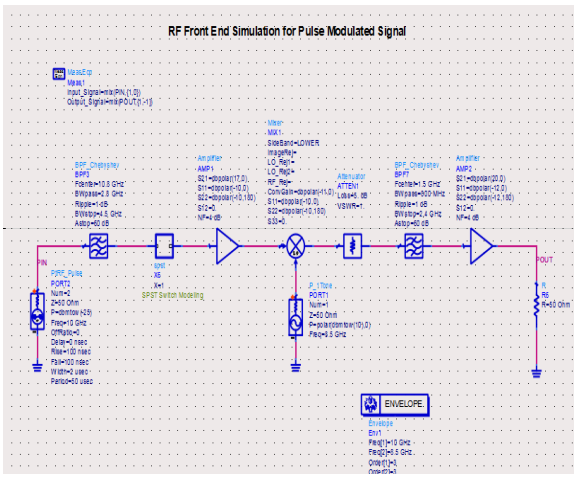


**Fig. 5** – Radar front-end simulation

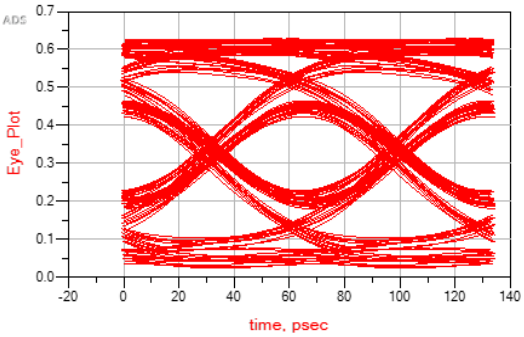


**Fig. 6** – Eye diagram (radar receiver)

The material used in the design is FR4 as a substrate for the PCB layout, which performs well at GHz frequency with its conducting and bonding arrangement are considered. Also, the top and bottom view layout were obtained for the layout of the circuit designed is shown in Fig. 7 and Fig. 8 below. The area of the design is optimized to 0.4 mm$^2$, which is the good enhancement for nanosensor province in the near future for all the holistic applications behind.

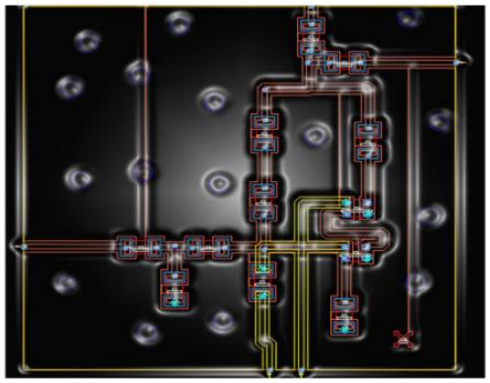

**Fig. 7** – Top view (layout)

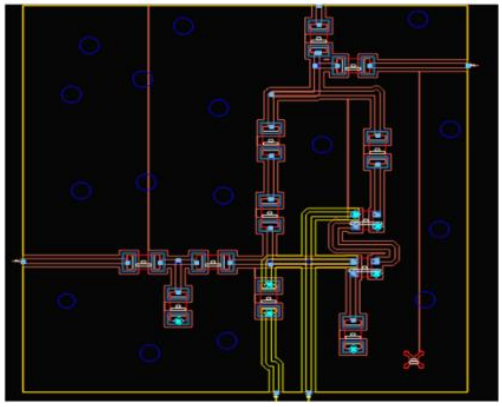

**Fig. 8** – Bottom view (layout)

## 4. CONCLUSIONS

In this paper, the proposed design of CCLNA using a 0.18 μm CMOS technology at millimeter Wave frequency. The proposed Cascode LNA provides greatest results attained higher gain and low NF at millimeter frequency. Nano-scale electronics and sensors with amplifier design for RADAR can be attained with increased robustness with post layout verification and the proposed design finds its suitability for RADAR front-end simulation.

Reconfigurable LNAs at two different frequencies to optimize the trade-off among performance metrics and extract the measurement results.

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# Конструкція підсилювача з низьким рівнем шуму CMOS Cascode Low Noise Amplifier (CCLNA) для наносенсорних додатків

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Запропоновано схему підсилювача з низьким рівнем шуму Cascode Low Noise Amplifier (CCLNA) із використанням стандартної технології CMOS 0,18 мкм міліметрової хвилі (мм·Вт). Пропонована схема CMOS CCLNA досягла максимального підсилення перетворення 17,4 дБ, NF в дБ і потужності 22,3 мВт в діапазоні mmW $K_a$. Вхідні та вихідні коефіцієнти відбиття добре узгоджені з менш ніж – 10 дБ на частоті діапазону $K_a$ з гарним коефіцієнтом стоячої хвилі за напругою (VSWR). Коефіцієнт зворотної передачі $S_{12}$ менше – 12 дБ, що вказує на те, що підсилювач LNA має покращену ізоляцію між входом і виходом, коефіцієнт стабільності більше одиниці для реалізації підсилювача. Конструкція CCLNA на основі SoC для дослідження рівня схеми з аналітичними рівняннями також довела, що результати моделювання схожі зі схемою, придатною для додатків наноелектроніки з вихідною потужністю 2 дБм, частотою переходу ($f_T$) 64 ГГц і максимальною робочою частотою ($f_{max}$) 96 ГГц, що свідчить про ефективність запропонованого методу, придатного для наносенсорних додатків. Обґрунтування ефективності моделювання RADAR (Radio Detection and Ranging) підтверджує, що приймач, розроблений із запропонованим підсилювачем LNA, підходить для конструкції приймача на високих mmW частотах.

**Ключові слова:** CCLNA, VSWR, RADAR, Підсилення перетворення, CMOS-дизайн, Наносенсор, Наноматеріали.