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An Analytical Model for the Depletion Region Width and Threshold Voltage of a Parallel Gated Junctionless Field Effect Transistor

A.K. Raibaruah*, K.C.D. Sarma

Central Institute of Technology Kokrajhar, Department of Instrumentation Engineering, 783370, India

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This paper reports on the modeling of the depletion region width and threshold voltage of a parallel gated junctionless field effect transistor. The depletion region width is obtained by resolving 1D Poisson equation along the channel of the device in the *y*-direction. The central potential through the channel region of the device is also considered. With the help of the depletion region width and device central potential model, the threshold voltage of the device is obtained. Exploration has been made for different variations of the depletion width depending on the gate to source voltage, gate oxide thickness, and different gate dielectric materials. For a 0.6 V gate bias, a 4 nm depletion width is achieved. The threshold voltage variation is obtained and analyzed by considering different drain voltages, doping concentrations, temperatures, and work functions. The device at 10^{19} cm^{-3} doping concentration, 300 K temperature, and 5.4 eV work function with a drain voltage of 1 V allows a threshold voltage of 0.47 V.

Keywords: Junctionless, Field effect, Depletion width, Threshold voltage.

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1. INTRODUCTION

During the modern era of the semiconductor industry, scaling down of devices and consequently storage in semiconductor memory is a primary concern with better performance enhancement of semiconductor devices. Semiconductor devices such as Field Effect Transistors (FETs) have *p-n* junctions. However, at the nano range, devices show challenges in terms of complexity in fabrication due to doping concentration gradient. On the other hand, devices such as Junctionless Field Effect Transistors (JLFETs) [1-14] have constant doping in the source length, channel, and drain length region, reducing fabrication complexity. A junctionless transistor was first reported in 2009 by J.P. Collinge [15]. It mainly works through the resultant field generated due to the difference between the gate work function and the body material of the device. This high work function difference generates an internal electric field which causes the formation of a depletion layer under the gate region. When there is a complete depletion layer in the channel region, then the current cannot flow through the device and the device is in the OFF state. On the other hand, when the gate voltage is applied, the effect of the internal electric field reduces, and the depletion layer starts diminishing slowly and current starts flowing through the channel region. This is known as the ON state of the device. Therefore, a depletion layer has a major role in the current conduction through the channel region of the device. Also, the applied gate voltage, at which the depletion width starts reducing and the flow of current begins, is called the threshold voltage of the device.

Junctionless transistors are a robust contender for memory devices. They help increase the speed of the memory chip by increasing the density of the chip. In addition, it can store information via flash memory [16]. Digital devices like computers, cameras, and GPS use flash memory technology to store data. The use of junctionless transistors helps in the reduction of mobility degradation which tends the junctionless transistor application to the flash memory. It has now become a rising device in the non-volatile memory market.

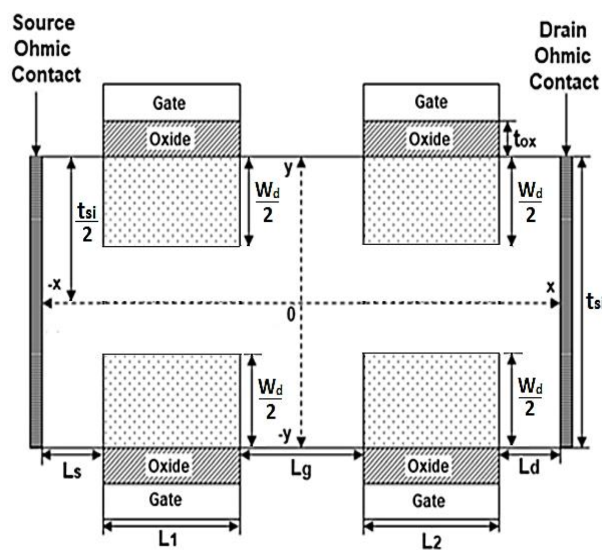

Fig. 1 – Cross-section view of PGJLFET

In this work, we are going to carry out the modeling of the depletion layer and threshold voltage of the Parallel Gated Junctionless FET (PGJLFET) [17, 18]. PGJLFET works better during the ON state as compared to conventional Junctionless Transistors [17]. The cross-sectional view of the PGJLFET is shown in Fig. 1. PGJLFET has two gate lengths L_1 and L_2. L_g is the gap length between two gate lengths. L_s and L_d are the source length and the drain length of the device, respectively. The device is 30 nm in length. With this very small node technology, the proposed device can be used in NAND flash memory with a high chip integration density.

* ak.raibaruah@cit.ac.in

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PGJLFET can be used as a fundamental element for computer circuitry as it can act as a binary switch (ON/OFF). It can be a promising device for memory cells. The flow of current through the channel of the PGJLFET device depends on the depletion region width which can be controlled by gate bias. Complete depletion blocks the current flow, and the device act as OFF, while reduction of the depletion region turns the device ON. At the threshold voltage, current will start flowing through PGJLFET. Therefore, it is very important to model the depletion width and the threshold voltage of the PGJLFET device. As the device is in the nano range, it becomes possible to accommodate billions of PGJLFETs to design a processor.

2. ANALYTICAL MODEL

The Poisson equation (1D) along the n-channel within the y-direction of the device is given by [6]:

$$\frac{d^2\phi(y)}{dy^2} = -q\frac{N_d}{\varepsilon_{si}}, \quad (1)$$

where $\phi(y)$ is the electrostatic potential, q is the electron charge, N_d is the donor concentration, and ε_{si} is the semiconductor permittivity.

Using the parabolic trial function method, one solution of equation (1) is given as [6]:

$$\phi(y) = C_0 + C_1(y) + C_2 y^2 . \quad (2)$$

At $y = \frac{t_{si} - W_d}{2}$, where W_d is the depletion region width and t_{si} is the channel thickness, the potential $\phi(y)$ can be written as

$$\phi(y) = \phi_0 = C_0 + C_1\left(\frac{t_{si} - W_d}{2}\right) + C_2\left(\frac{t_{si} - W_d}{2}\right)^2, \quad (3)$$

$$\frac{d\phi(y)}{dy} = 0 = C_1 + C_2(t_{si} - W_d) . \quad (4)$$

At $y = \frac{t_{si}}{2}$,

$$\frac{d\phi(y)}{dy} = C_1 + C_2 t_{si} = \frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}}\left(\phi_{gs} - \phi_s\right). \quad (5)$$

Substituting the value of C_1 from equation (5) into equation (4), we obtain

$$C_2 = \frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}W_d}\left(\phi_{gs} - \phi_s\right), \quad (6)$$

where ϕ_s is the potential at the surface, ε_{ox} is the gate oxide permittivity, t_{ox} is the thickness of the gate oxide and

$$\phi_{gs} = V_{gs} - V_{fb} ,$$

where, V_{gs} is the gate to source voltage, and V_{fb} is the flat band voltage.
Substituting the C_2 value into equation (4), we get

$$C_1 = -\frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}W_d}\left(t_{si} - W_d\right)\left(\phi_{gs} - \phi_s\right) . \quad (7)$$

Substituting the values of C_1 and C_2 into equation (3), we get

$$C_0 = \phi_0 + \frac{\varepsilon_{ox}}{4t_{ox}\varepsilon_{si}W_d}\left(\phi_{gs} - \phi_s\right)\left(t_{si} - W_d\right)^2 . \quad (8)$$

Now substituting the values of C_0, C_1 and C_2 into equation (2), we get

$$\phi(y) = \begin{bmatrix} \phi_0 + \frac{\varepsilon_{ox}}{4t_{ox}\varepsilon_{si}W_d}(t_{si} - W_d)^2\left(\phi_{gs} - \phi_s\right) \\ -\frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}W_d}(t_{si} - W_d)\ \left(\phi_{gs} - \phi_s\right)y \\ +\frac{\varepsilon_{ox}}{t_{ox}\varepsilon_{si}W_d}\ \left(\phi_{gs} - \phi_s\right)y^2 \end{bmatrix} \quad (9)$$

At $y = \frac{t_{si}}{2}$,

$$\phi_s = \begin{bmatrix} \phi_0 + \frac{\varepsilon_{ox}}{4t_{ox}\varepsilon_{si}W_d}(t_{si} - W_d)^2\left(\phi_{gs} - \phi_s\right) \\ -\frac{\varepsilon_{ox}}{2t_{ox}\varepsilon_{si}W_d}(t_{si} - W_d)\ \left(\phi_{gs} - \phi_s\right)t_{si} \\ +\frac{\varepsilon_{ox}}{4t_{ox}\varepsilon_{si}W_d}\ \left(\phi_{gs} - \phi_s\right){t_{si}}^2 \end{bmatrix} \quad (10)$$

From equations (9), (10) and (1) we obtain

$$\varepsilon_{ox}qN_dW_d^{\,2} + 4t_{ox}\varepsilon_{si}qN_dW_d + 8\varepsilon_{ox}\varepsilon_{si}\left(\phi_{gs} - \phi_0\right) = 0 , \quad (11)$$

$$W_d = \frac{-4t_{ox}\varepsilon_{si}qN_d + \sqrt{(4t_{ox}\varepsilon_{si}qN_d)^2 - 32{\varepsilon_{ox}}^2\varepsilon_{si}\left(\phi_{gs} - \phi_0\right)}}{2\varepsilon_{ox}qN_d} . \quad (12)$$

Equation (12) represents the depletion width of the n-channel PGJLFET device.

The central potential through the channel length region is given by [18]

$$\phi_0(x) = \left(\left[\frac{(V_{ds} + C\lambda^2).e^{\frac{(L_2 + \frac{L_g}{2})}{\lambda}} - \frac{C\lambda^2}{e^{\frac{L_1 + \frac{L_g}{2}}{\lambda}}}}{(e^{\frac{2(L_2 + \frac{L_g}{2})}{\lambda}} - e^{\frac{-2(L_1 + \frac{L_g}{2})}{\lambda}})} e^{\frac{x}{\lambda}} \right] - \left[\frac{(V_{ds} + C\lambda^2).e^{\frac{(L_2 - 2L_1 - \frac{L_g}{2})}{\lambda}} - C\lambda^2 e^{\frac{-3(L_1 + \frac{L_g}{2})}{\lambda}}}{(e^{\frac{2(L_2 + \frac{L_g}{2})}{\lambda}} - e^{\frac{-2(L_1 + \frac{L_g}{2})}{\lambda}})} - \frac{C\lambda^2}{e^{\frac{L_1 + \frac{L_g}{2}}{\lambda}}} \right] e^{\frac{-x}{\lambda}} \right) - C\lambda^2 \quad (13)$$

Solving equation (12), we obtain

$$2\varepsilon_{ox}qN_dt_{si} = \left[\begin{array}{l} -4t_{ox}\varepsilon_{si}qN_d \\ +\sqrt{(4t_{ox}\varepsilon_{si}qN_d)^2 - 32\varepsilon_{ox}{}^2\varepsilon_{si}\left(\phi'_{gs}-\phi'_0\right)} \end{array} \right]. \quad (14)$$

From equations (13) and (14) we get

$$V_{th} = \left[\begin{array}{l} \left(\left[\dfrac{(V_{ds}+C\lambda^2).e^{\frac{(L_2+\frac{L_g}{2})}{\lambda}} - \dfrac{C\lambda^2}{e^{\frac{L_1+\frac{L_g}{2}}{\lambda}}}}{\left(e^{\frac{2(L_2+\frac{L_g}{2})}{\lambda}} - e^{\frac{-2(L_1+\frac{L_g}{2})}{\lambda}}\right)} e^{\frac{x}{\lambda}} \right] - \left[\begin{array}{l} \dfrac{(V_{ds}+C\lambda^2).e^{\frac{(L_2-2L_1-\frac{L_g}{2})}{\lambda}} - C\lambda^2 e^{\frac{-3(L_1+\frac{L_g}{2})}{\lambda}}}{\left(e^{\frac{2(L_2+\frac{L_g}{2})}{\lambda}} - e^{\frac{-2(L_1+\frac{L_g}{2})}{\lambda}}\right)} \\ -\dfrac{C\lambda^2}{e^{\frac{L_1+\frac{L_g}{2}}{\lambda}}} \end{array} \right] e^{\frac{-x}{\lambda}} \right) - C\lambda^2 \\ +V_{fb} + \dfrac{\left[\begin{array}{l} (2\varepsilon_{ox}qN_dt_{si}) \\ +(4t_{ox}\varepsilon_{si}qN_d) \end{array} \right]^2 - (4t_{ox}\varepsilon_{si}qN_d)^2}{32\varepsilon_{ox}{}^2\varepsilon_{si}} \end{array} \right] \quad (15)$$

Equation (15) is the threshold voltage of PGJLFET.

3. RESULTS AND DISCUSSION

Fig. 2 shows a depletion width variation for different gate bias. The figure shows that the depletion width for the device decreases as we increase the gate to source voltage because of the reduction in an internal electric field, which is generated due to the gate electric field and work function difference between metal and semiconductor devices.

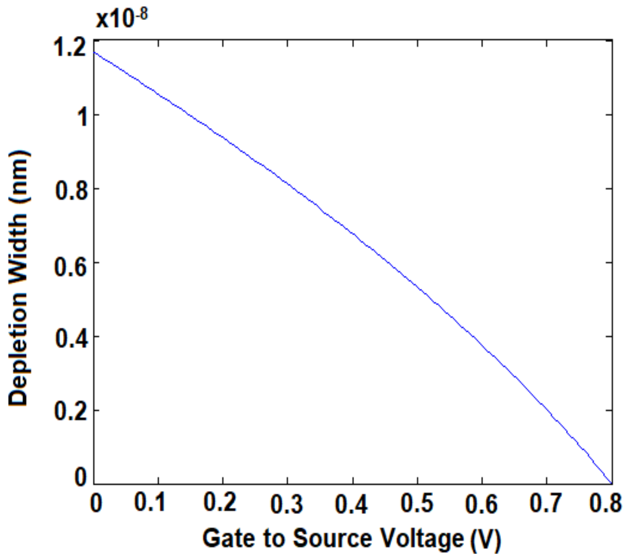

Fig. 2 – Depletion width versus gate to source voltage

Fig. 3 shows the depletion width variation for different values of the gate oxide thickness. As gate capacitive coupling is higher for thinner oxide thicknesses, a larger depletion width can be seen from the figure.

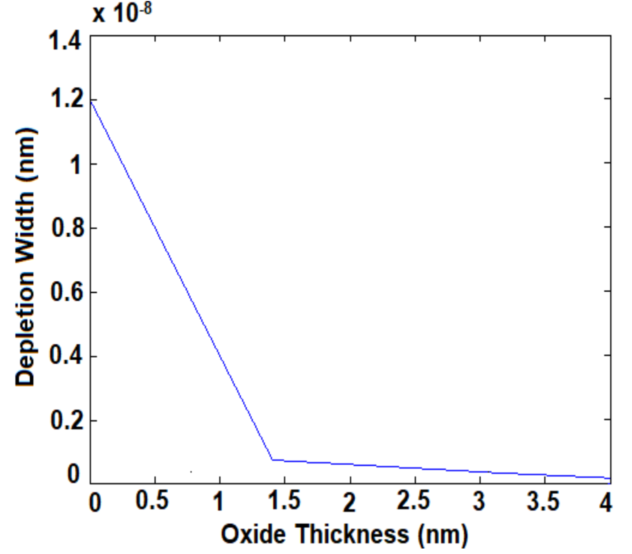

Fig. 3 – Depletion width versus oxide thickness

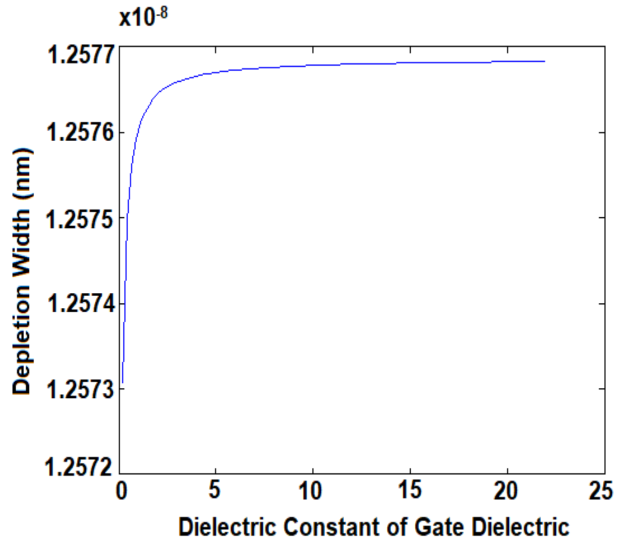

Fig. 4 – Depletion width versus dielectric constant of the gate dielectric

Table 1 – Threshold voltages for different drain to source voltages

Sl. No	Drain voltage (V)	Threshold voltage (V)
1	0.2	0.26
2	0.4	0.31
3	0.6	0.37
4	0.8	0.42
5	1	0.47

Table 2 – Threshold voltages for different doping concentrations

Sl. No	Doping concentration (cm^{-3})	Threshold voltage (V)
1	10^{18}	0.03
2	$5x10^{18}$	0.22
3	10^{19}	0.47

Fig. 4 depicts the depletion width variation for different values of the gate dielectric constants. From the figure, it can be observed that as the gate dielectric constant value increases, the depletion width of the

device also increases. This is because the capacitive coupling between the gate and the channel is also high for a higher gate dielectric constant.

Table 3 – Threshold voltages for different temperatures

Sl. No	Temperature (K)	Threshold voltage (V)
1	300	0.47
2	400	0.03
3	500	0.02

Table 4 – Threshold voltages for different work functions

Sl. No	Work function (eV)	Threshold voltage (V)
1	5	0.02
2	5.2	0.03
3	5.4	0.47

Tables 1, 2, 3, and 4 indicate the threshold voltages for different values of drain voltage, doping concentration, temperature, and work function. From Table 1, it is apparent that as the drain voltage increases, the threshold voltage also increases. The threshold voltage of the device is mainly guided by the applied gate bias, whereas a higher drain to source voltage turns down the drain-induced barrier lowering (DIBL) effect. From Table 2, we can see that at high doping a high threshold voltage is obtained. At a moderate doping level, the device seems to be in the ON state due to a very small threshold voltage. Table 3 indicates that the threshold voltage is higher at low temperatures. When we increase the temperature, the threshold voltage value is very low as the density of molecules becomes small and the device acts as the ON state. From Table 4, it can be seen that at lower work functions, the threshold voltage is very small, and the device is already in the ON state. At a work function of 5.4 eV, the threshold voltage obtained is 0.47 V.

4. CONCLUSIONS

This paper presents a mathematical model for the depletion width and threshold voltage of a parallel-gated junctionless field-effect transistor (PGJLFET) using the 1D Poisson equation. The change in the depletion width for various values of the applied gate bias, oxide thickness, and gate dielectric constants is studied. In addition, the threshold voltage is also obtained and analyzed for different values of drain voltage, doping concentration, temperature, and work function. Compact analytical modeling is suitable for future applications as logic and storage in the memory device.

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Аналітична модель ширини збідненої зони та порогової напруги безперехідного польового транзистора з паралельним затвором

A.K. Raibaruah, K.C.D. Sarma

Central Institute of Technology Kokrajhar, Department of Instrumentation Engineering, 783370, India

У роботі повідомляється про моделювання ширини збідненої зони та порогової напруги безперехідного польового транзистора з паралельним затвором. Ширина збідненої зони отримується розв'язуванням одновимірного рівняння Пуассона вздовж каналу пристрою в напрямку y. Також враховується центральний потенціал через область каналу пристрою. За допомогою моделі ширини збідненої зони та центрального потенціалу пристрою отримують порогову напругу пристрою. Були прове-

дені дослідження для різних варіацій ширини збідненої зони залежно від напруги між затвором і джерелом, товщини оксиду затвора та різних діелектричних матеріалів затвора. Для напруги зміщення на затворі 0,6 В ширина збідненої зони складає 4 нм. Зміну порогової напруги отримують і аналізують, враховуючи різні напруги стоку, концентрації легування, температури та роботи виходу. Пристрій допускає порогову напругу 0,47 В при концентрації легування 10^{19} см$^{-3}$, температурі 300 К, роботі виходу 5,4 еВ і напрузі стоку 1 В.

Ключові слова: Безперехідний, Польовий ефект, Ширина збідненої зони, Порогова напруга.