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The Study of Hetero Dielectric Buried Oxide and Heterojunction Dual Material TFET

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This study aims to enhance the ambipolar behavior and low-ON current of hetero dielectric BOX and heterojunction dual material TFETs. Tunnel FETs (TFETs), which work on tunnelling phenomenon, can circumvent MOSFET limitations owing to device scalability. Subthreshold current, drain-induced barrier lowering, and hot electron effects are among MOSFET restrictions owing to device scaling. TFET does not fulfil the ITRS requirement for a high ON current, which is compatible with MOSFET-based circuits. Different structures, channel materials, gate oxide materials, and appropriate gate work-functions can be used to improve the low ON current of TFETs. We propose and develop a heterojunction dual material TFET in this study. Heterojunction double gate TFET has been studied previously. The ON-state current is improved and the ambipolar current is reduced compared to the standard TFET, increasing the ON-state current lowers the subthreshold slope. Also, the dual gate TFET has higher performance than conventional TFET. The addition of heterojunction to the device aids in the reduction of the band gap at the source channel junction, and the gate oxide and junction work together to increase drain current (I_D) capacity while lowering parasitic strength. The concept of hetero buried oxide along with heterojunction dual material is integrated together for better outcomes. Initially the surface potential is derived using Poison's equation divided equally for regions of buried oxide as SiO_2 and HfO_2. Lateral and vertical electric fields are implemented using the surface potential and the potential along the *Y*-axis. The source material is InGaAs, the target material is InP and SiO_2/high-*k* hetero dielectric is used as the gate oxide material. Simulation is done with SILVACO TCAD.

Keywords: Heterojunction, Dual material, Tunnel FET, Drain current.

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1. INTRODUCTION

Higher chip density and lower power requirements are necessary in today's FET industry. Because they are exempt to scaling effects, TFETs are one of the most promising MOS alternatives for low-power applications. Low power with a moderate operating frequency is a key concern in numerous applications such as SRAM design, digital watches, and medical devices, thanks to recent technological breakthroughs. The energy required for switching is reduced as the supply voltage is increased, which enhances device performance. When the transistor runs in the subthreshold zone, the device's transconductance gain improves, and the gate input capacitance is reduced, resulting in more perfect results. This can be defined as a specific change in gate voltage required to raise the drain rate by an order of magnitude. TFETs are similar to gated PIN diodes in that they work on the basis of quantum-mechanical band-to-band tunnelling (BTBT) rather than thermal charge carrier injection as in ordinary MOSFETs [1, 2].

TFETs can easily solve the fundamental issue of lowering SS beneath 60 mV/dec at normal temperature. Because of their low leakage current, TFETs have a superior I_{ON}/I_{OFF} ratio than MOSFETs. However, due to the BTBT process, so at source channel intersection, their ON current is also minimal [3-7]. To address this issue, various researchers offered various geometrical variants of TFETs to enhance I_{ON} and SS, with nanowires being the most advantageous TFET geometrical [9-14]. Nanowires are employed to create a channel in the device, which increases the likelihood of tunnelling. The manufacturing has been in demand with a more efficient energy and speedier technology, which has resulted in MOSFETs being scaled down [15, 16]. However, there have been significant drawbacks to this scalability. Due to these constraints, tunnel field effect transistors (TFETs) were developed, which differ from MOSFETs in their essential carrier injection method [17]. The source, drain, and dielectric materials used in the proposed project differ from silicon. A heterojunction dual material TFET performance will be investigated and assessed.

2. STRUCTURE AND PARAMETERS

The proposed structure of buried oxide layer is separated by two different dielectrics: SiO_2 and high-*k* gate oxide HfO_2 with a *k* value of 25 shown in Fig. 1. Thus, the structure is hetero dielectric buried oxide (HDBOX). The dual materials M1 and M2 are aluminum and nickel with a work function of 4.08 eV and 5.01 eV, respectively. The only difference compared to

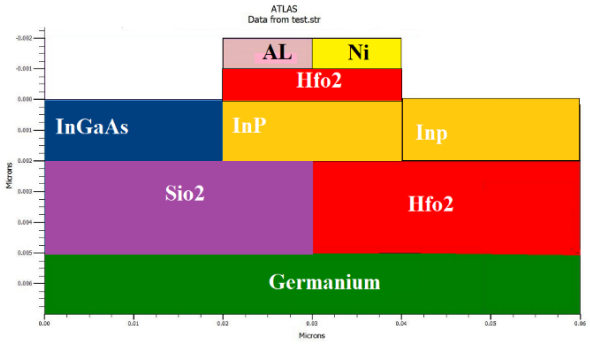

Fig. 1 – TCAD simulated structure

the conventional structure is that the high-k dielectric heterodielectric box is located directly below the drain.

Various parameters used in the proposed study are doping concentration, oxide thickness, Kane parameter in TCAD. The Kane parameter values used in implementing TCAD are $A_k = 4 \times 10^{19}$, $B_k = 4 \times 10^{16}$. The parameters designed to generate the drain current tunneling rate using the surface potential approach are shown in Table 1.

Table 1 – Parameter values for the proposed structure

S.no	Parameters	Symbol	Value
1.	Source doping concentration	*Ns*	10^{19} cm^{-3}
2.	Channel doping concentration	*Nc*	10^{19} cm^{-3}
3.	Drain doping concentration	*Nd*	5×10^{19} cm^{-3}
4.	Oxide thickness	*Tox*	3 nm
5.	Length of source, channel, drain	*Ls*, *Lc*, *Ld*	20 nm, 20 nm, 20 nm
6.	Permittivity of SiO_2 and HfO_2	ε_{SiO2}, ε_{HfO2}	$3.9\varepsilon_0$, $23\varepsilon_0$

3. SIMULATED RESULTS

The proposed structure is implemented in Silvaco TCAD with dimensions, concentration, doping information included in the deck build. The structure is the output of each material implemented in the deck build of the Silvaco TCAD tool. ATLAS input data must have five groups of instructions in the correct order. These are the following groups.

1. An explanation of the structure. The model structure can be defined by this set of assertions. This section contains statements that define meshes, region, electrode, materials, doping, and so on.
2. Specifications for materials and models. The material properties and physical models that will be used in the simulations are specified in this collection of statements. This section contains statements that define material, models, contact qualities, interface charges, and so on.
3. The definition of a numerical method. This statement describes numerical methods that will be utilized to solve the simulation's set of equations.
4. Specification of the solution. The biased parameters whereby the simulations must be run are specified in this collection of statements. It contains assertions indicating that simulators should solve for the provided bias conditions, log the result, and store the solution as a solution file.
5. Analyze the outcomes. This set of lines includes commands for opening and analyzing a solution stored in a solutions file.

Fig. 2 is the result of mesh structure; mesh selection implies a trade-off between precision and numerical efficiency. For precision, a hybrid approach is needed that can address all of the method's main properties. A crude mesh that aims at minimizing set of reference points is required for numerical efficiency. Triangular meshes are used in ATLAS.

The variance associated with a grid could be studied systematically by running computation with a sequence of finer meshes. This takes a long time and is rarely carried out. The common strategy is to use the initial or base mesh to sufficiently resolve structural elements, such as doping, and then add nodes as needed to resolve the output's essential features. Regridding is the method of assigning more nodes to an existing structure.

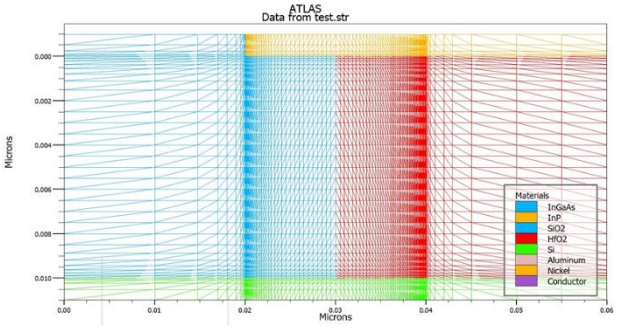

Fig. 2 – Mesh structure from Silvaco TCAD

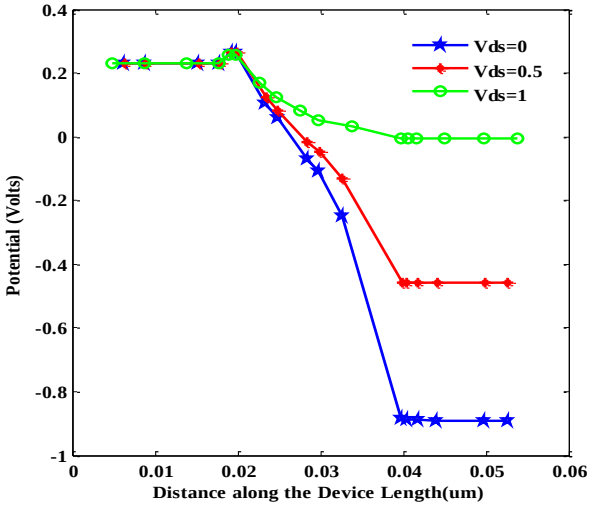

Fig. 3 – Surface potential with varying voltage (*Vds*)

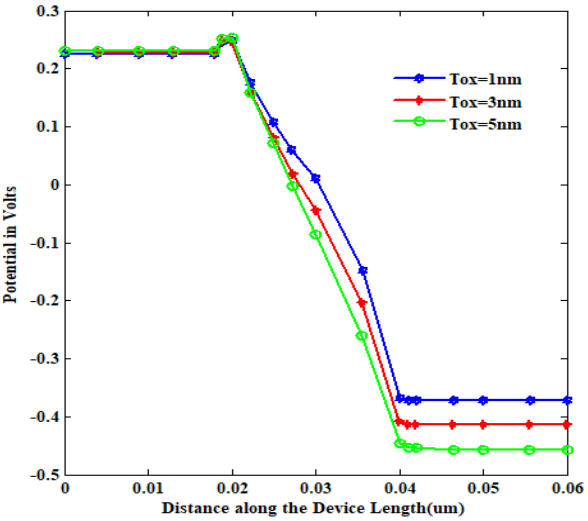

Fig. 4 – Surface potential with varied thickness (*Tox*)

Fig. 3 is the result on the *X*-axis with the distance along the device length and on the *Y*-axis with potential. Potential along the device length decreases with an increase in the distance along the channel. The voltage at the drain source junction (*Vds*) is equal to 0, 0.5, and 1 V. With an increase in the voltage (*Vds*), the potential along the channel length increases. Fig. 4 shows the result on the *X*-axis with the distance along the device length and on the *Y*-axis with potential. Potential along the device length decreases with an increase in the distance along the channel. The oxide thickness is equal to 1, 3, and 5 nm. With an increase in the oxide thickness, the potential along the channel length decreases.

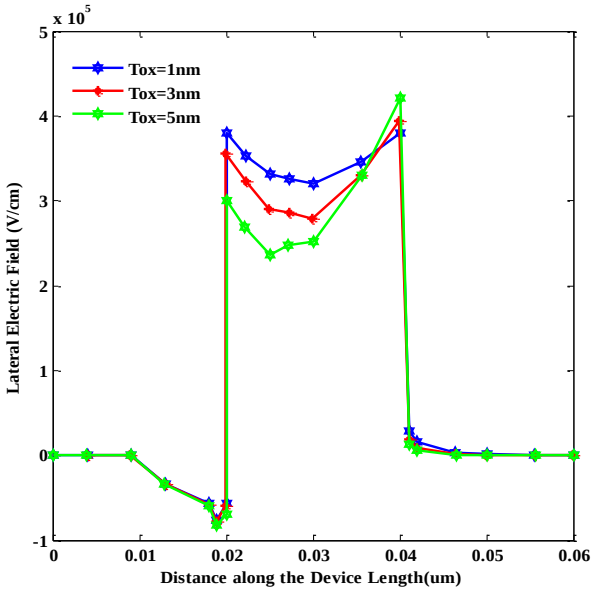

Fig. 5 – Lateral electric field with varied thickness (*Tox*)

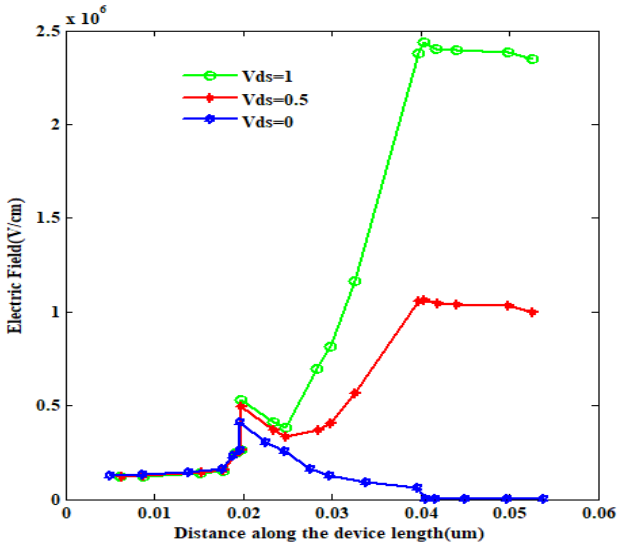

Fig. 6 – Electric field with varying voltage (*Vds*)

The plot shown in Fig. 5 is the result on the *X*-axis with the distance along the device length and on the *Y*-axis with lateral electric field. The lateral electric field along the device length decreases with an increase in the distance along the channel for buried oxide SiO_2. But for buried oxide HfO_2, the lateral electric field along the device length increases with an increase in the distance along the channel. With an increase in the channel thickness, the electric field decreases. Fig. 6 shows the result on the *X*-axis with the distance along the device length and on the *Y*-axis with electric field. The electric field along the device length increases with an increase in the distance along the channel with HfO_2 as buried oxide. The electric field increases with an increase in voltage applied at the drain source junction. Also, a peak is observed in the source channel region.

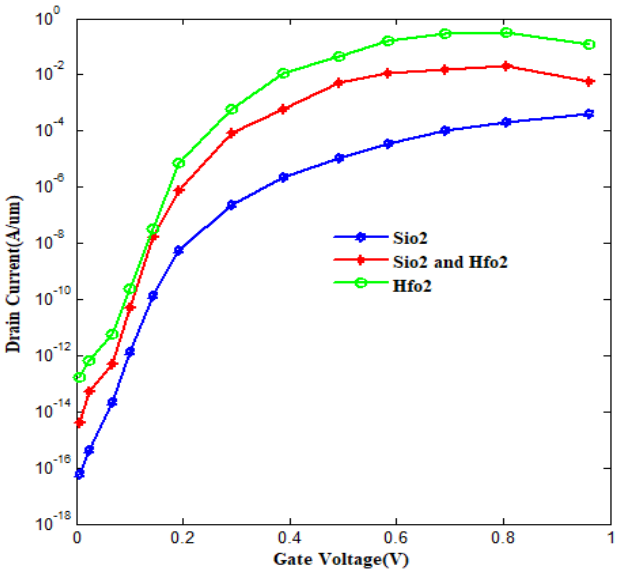

Fig. 7 – Drain current with gate voltage

Fig. 7 is the result on the *X*-axis with the gate voltage varied from 0 to 1 V and on the *Y*-axis with drain current. Drain current increases with an increase in the applied gate voltage *Vgs*. The buried oxide with HfO_2 has improved ON current compared to SiO_2 and buried oxide with both SiO_2 and HfO_2.

4. CONCLUSIONS

In current technology, TFETs are used in many applications to overcome the limitations of MOSFETs. TFETs have advantages. The proposed structure is developed with a combination of hetero dielectric and a junction dual material. The simulated TCAD structure results in an improvement compared to normal structure. The potential along the channel increases with increasing voltage applied at the drain source junction. Also, the potential decreases with increasing the thickness of buried oxide. The electric field along the channel increases with increasing voltage applied at the drain source junction. The lateral electric field increases with decreasing the thickness of buried oxide. In conventional TFETs, buried oxide is SiO_2. With an increase in *k*-value, the ambipolar nature of the permittivity increases, but with HfO_2 as buried oxide, the lateral electric field is improved compared to SiO_2.

REFERENCES

1. P. Vimala, T.S. Arun Samuel, *Silicon* **13**, 3899 (2021).
2. M. Sathishkumar, T.S. Arun Samuel, P. Vimala, *International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE)*, 1-5 (2020).
3. F. Obite, G. Ijeomah, J.S. Bassi, *IJCA* **41** No 2, 149 (2018).
4. P. Vimala, N.B. Balamurugan, *J. Semicond.* **33** No 3, 034001 (2012).
5. C. Usha, P. Vimala, T.S.A. Samuel, et al., *J. Comput. Electron.* **19**, 1144 (2020).
6. P. Vimala, K. Maheshwari, *J. Nanotech. Nano- Eng.* **5** No 2, 19 (2019).
7. G. Navya Shree, U. Priyadarshini, M. Keerthana, P. Vimala, *2020 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE)*, 1-5 (2020).
8. P. Vimala, N.B. Balamurugan, *Int. J. Comput. Math. Elec. Electron. Eng.* **33** No 1-2, 630 (2014).
9. R.A. Patel, R.A. Thakker, *IJAR* **5** No 1, 41 (2015).
10. P. Vimala, N.B. Balamurugan, *J. Semicond.* **35** No 3, 034001 (2014).
11. M. Mehrad, E.S. Ghadi, *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, 164 (Greece: IEEE: 2017).
12. P. Vimala, T.S.A. Samuel, *J. Nano Res.* **60**, 113 (2019).
13. P. Banerjee, S.K. Sarkar, *J. Comp. Electron.* **16** No 3, 631 (2017).
14. C. Usha, P. Vimala, *Indian J. Phys.* **95**, 1365 (2021).
15. N. Chowdhury, G. Iannaccone, G. Fiori, D.A. Antoniadis, T. Palacios, *IEEE Electron Dev. Lett.* **38** No 7, 859 (2017).
16. Eatemadi, H. Daraee, K. Hamzeh, M. Kouhi, N. Zarghami, Akbarzadeh, M. Abasi, Y. Hanifehpour, S.W. Joo, *Nanoscale Res. Lett.* **9**, 393 (2014).
17. N. Dhurandhar, P. Dwivedi, *Res. J. Eng. Technol.* **8** No 1, 56 (2019).

Дослідження гетеродіелектричного заглибленого оксиду та TFETs з гетеропереходом із подвійним матеріалом

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Дослідження спрямоване на покращення амбіполярної поведінки та низького струму увімкнення гетеродіелектричних BOX та TFETs з гетеропереходом із подвійним матеріалом. Тунельні польові транзистори (TFETs), які працюють на явищі тунелювання, можуть обійти обмеження MOSFETs завдяки масштабованості пристрою. Допороговий струм, індуковане стоком зниження бар'єру і ефекти гарячих електронів належать до обмежень MOSFETs через масштабування пристрою. TFET не відповідає вимогам ITRS щодо високого струму увімкнення, що сумісно зі схемами на основі MOSFETs. Для покращення низького струму TFETs можна використовувати різні структури, матеріали каналу, оксидні матеріали затвора та відповідні роботи виходу затвора. У дослідженні ми пропонуємо та розробляємо гетеропереходний двоматеріальний TFET. Гетеропереходний TFET з подвійним затвором вивчався раніше. Струм увімкненого стану покращено, а амбіполярний струм зменшено порівняно зі стандартним TFET, збільшення струму увімкненого стану зменшує підпорогову крутизну. Крім того, TFET з подвійним затвором має вищу продуктивність, ніж звичайний TFET. Додавання гетеропереходу до пристрою сприяє зменшенню забороненої зони на переході між джерелом та каналом, а оксид затвора та перехід працюють разом, щоб збільшити струму стоку (I_D), одночасно знижуючи паразитну силу. Концепція гетеро заглибленого оксиду разом із подвійним матеріалом гетеропереходу інтегрована для кращих результатів. Спочатку поверхневий потенціал виводиться за допомогою рівняння Пуассона, розділеного порівну на області заглибленого оксиду SiO_2 і HfO_2. Бічні та вертикальні електричні поля реалізуються за допомогою поверхневого потенціалу та потенціалу вздовж осі *Y*. Вихідним матеріалом є InGaAs, цільовим матеріалом є InP, а гетеродіелектрик SiO_2/high-*k* використовується як оксидний матеріал затвора. Моделювання виконується за допомогою SILVACO TCAD.

Ключові слова: Гетероперехід, Подвійний матеріал, Тунельний польовий транзистор, Струм стоку.