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Formation of Dislocations During Phosphorus Doping in the Technology of Silicon *p-i-n* Photodiodes and their Influence on Dark Currents

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In the manufacture of *p*-type silicon-based *p*-i-*n* photodiodes (PDs), it was found that when the time of phosphorus diffusion increases, the yield of fit products significantly decreases. Up to 10 % are the rejects as to external appearance, the rest – as to the spread of dark current levels of PD responsive elements (REs), since the double spread of dark currents is considered a defect. Probably, the above occurrence might be caused by non-uniform distribution of defects across REs because of the increase in phosphorus impurity. An additional investigation was required to find out the cause of non-uniform distribution of dark currents and to establish the optimal concentration of impurities, which would provide for a low dark current with minimum spread. To study the effect of the surface resistance of the n^+-layer on the concentration of dislocations and their distribution, PDs were made with different duration of the predeposition, accordingly, with different values of the surface resistance. To reveal the nature of the distribution of dark currents on REs, defective crystals were studied using selective etching. It was established that conditions for the occurrence of structural defects within one ingot may be different due to the spread of specific resistance. The dependence of the dislocation density on the surface resistance after phosphorus diffusion was studied. It was noted that REs of a high level of dark currents were characterized by an increased concentration of dislocations as compared to the characteristic density for good crystals at a given surface resistance. The actual reasons for the dislocations distribution non-uniformity are the irregular distribution of point defects generated during oxidation and the presence of microdefects formed during mechanical or chemical-dynamic polishing. When locally increased numbers of growth defects and point defects acquired during the mechanical, chemical or thermal operations are superimposed, critical faults and spread of dark currents with maximum values are observed.

Keywords: Photodiode, Surface resistance, Dark current, Dislocation.

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1. INTRODUCTION

In the manufacture of electronic components of micron and submicron sizes, the most stringent requirements to structural perfection of both the source semiconductor material and the use production procedures and techniques for making finished products, minimizing the formation of structural defects, are specified.

Silicon, due to its electrophysical, mechanical and technological properties, remains the main material for the production of the element base of modern electronics. The ever-increasing requirements for the reliability of the parameters of silicon structures call for the use of not only new technologies, but also further experimental and theoretical study of defect formation processes. Such studies are needed, in particular, to increase the reliability and stability of the parameters of silicon photodetectors.

P-i-*n* photodiodes (PDs) are the most widely used silicon photodetectors. The specific nature of the study of defect formation processes and their influence on PD parameters as compared with conventional PDs, is the presence of the high-impedance *i*-region, in which processes of recombination-generation of charge carriers take place. On the one hand, the presence of the *i*-region leads to an improvement in the injection coefficient in the *p*-i-*n*-structure, on the other hand, the presence of increased defect concentration in the *i*-region encourages the occurrence of additional recombination-generation centers, thus photoelectric parameters are changed and degraded. Also, the need to create a shallow *p*-*n* junction in the *p*-i-*n* photosystem gives rise to the problem of doping a very thin near-surface layer of silicon, which can generate high mechanical stresses or high density of defects [1]. Accordingly, due to the presence of a defective structure in the form of clusters of structural defects or dislocations, both in the *i*-region and surface n^+- or p^+-layers, deep levels appear in the band gap of silicon, which causes an increase in dark currents [2].

In the manufacture of silicon-based *p*-i-*n* PDs, it was found that when there is an increase in the concentration of phosphorus in the n^+-layer, the yield of fit products significantly decreases. About 90 % of PD defects were caused by the increase in the levels or the spread of dark currents I_d of the responsive elements (REs) of one PD, as far as the double spread of I_d is considered a defect. The rest is the lack of proper appearance. One of the reasons for the spread of I_d may be the non-uniformity of the resistance of the interconnection between the REs and the guard ring (GR). This parameter characterizes the resistance between the active elements of the PD, a decrease in which level often leads to an increase in I_d. When measuring the resistance of the interconnection, no scatter was detected. Also, no visual defects that could affect dark currents were observed on the surface of PD crystals. Probably, the above occurrence might be caused by non-uniform distribution of defects across the RE be-

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cause of the increase in phosphorus impurity. An additional investigation was required to find out the cause of non-uniform I_d distribution, and to establish the optimal concentration of impurities, which would provide for a low dark current with minimum spread.

In technical literature and scientific publications, the matter of the influence of phosphorus concentration on the parameters of *p-i-n* PDs has not been studied, and most of the works are devoted to solar cells. Thus, [3] showed that the diffusion of phosphorus of a high concentration into silicon made by the Czochralski method leads to an increase in oxygen precipitates, which in turn cause the non-uniform distribution of microdefects and minority charge carrier lifetime (τ). In [4], the dependence of values and uniformity of the distribution of τ in silicon on the surface resistance of the phosphorus diffusion layer was investigated, and no-dependence in boron diffusion was shown.

Based on the above, the purpose of this article is to study the effect of phosphorus concentration (surface resistance) in the n^+-layer of a silicon *p-i-n* PD on the formation of structural defects and their contribution to the non-uniformity of dark current values.

2. EXPERIMENTAL

The research was carried out in the manufacture of silicon four-element *p-i-n* PDs with a GR for operation at supply voltage $U_{op} = 120$ V and operating wavelength $\lambda_{op} = 1.064$ μm. PDs were made on the basis of single-crystal dislocation-free *p*-type silicon with resistivity $\rho \approx 18$ kOhm·cm, minority charge carrier lifetime $\tau \approx 2$ ms and [111] orientation by diffusion-planar technology. The method of two-stage diffusion from planar phosphorus sources was used to create REs and a n^+-GR. Initially, the predeposition was carried out, i.e., a short diffusion from an unlimited source at $T = 1323$ K in a nitrogen atmosphere, obtaining a thin diffusion layer up to 1 μm in thickness in the substrate. Next, a drive-in was performed at $T = 1423$ K in an oxygen atmosphere, while the diffusion layer was already a source of a limited concentration of impurities. After each of these operations, the surface resistance R_S was monitored by the four-probe method [5]. For convenience, it is the surface resistance of the obtained samples to be indicated in the description of the research, because this parameter is most often used in practice.

To study the effect of the surface resistance of the n^+-layer on the concentration of dislocations and their distribution, PDs with different duration of the predeposition, accordingly, different values of R_S were made.

Table 1 – Surface resistance values of PDs obtained at different predeposition durations

Predeposition duration *t*, min	R_S, Ohm/□ (after predeposition)	R_S, Ohm/□ (after drive-in)
60	3.1	1.9
50	3.3	2.1
40	3.7	2.4
30	4.1	2.7
20	5.4	3.3
10	8.4	5.0
5	12.7	8.1

The R_S values of the obtained samples are given in Table 1.

It should be noted that the dependence of surface resistance on the duration of the predeposition is not constant, as it may vary depending on the depletion of planar sources, saturation of quartz reactors with phosphorosilicate glass, carrier gas consumption and other factors.

Dark currents I_d at the supply voltage $U_{op} = 120$ V were monitored. The current density J_d in nA/cm^2, which was calculated by formula (1), will be indicated.

$$J_d = \frac{I_d}{A_{RE}}, \quad (1)$$

where A_{RE} is the area of the RE.

To study the surface of crystals, selective etching was performed in Sirtl's etchant of HF – 100 cm^3, CrO_3 – 50 g, H_2O – 120 cm^3 composition [6]. The duration of the etching was 5 min. After the etching, the surface was examined with optical microscopes at different magnifications.

3. RESULTS OF THE RESEARCH AND THEIR DISCUSSION

3.1 Influence of the Substrate Material on the Formation of Dislocations during Thermal Operations

It is known that silicon doping is one of the main causes of structural defects, dislocations, in particular [7]. It is the diameter of the introduced atoms different from the diameter of the atoms of the substrate, being responsible for the defects. In particular, the diameter of a silicon atom is $d_{Si} = 1.32 \cdot 10^{-10}$ m, while in phosphorus it is $d_P = 1.28 \cdot 10^{-10}$ m [8]. Accordingly, when a foreign atom of a smaller diameter (as compared to the atoms of the matrix) is introduced, mechanical stresses occur in the substrate, giving rise to compression deformations, which, in turn, contribute to the formation of dislocations.

It should also be noted that the density of dislocations in silicon wafers, formed as a result of the same technological modes and operations (including the same R_S after phosphorus diffusion), depends on the source material: concentration of point defects, oxygen precipitates, resistivity. Point defects and precipitates, in particular, become the centers of formation of dislocation loops during heat treatment [7, 9]. Besides, with decreasing resistivity of the substrate material, mechanical stresses in it increased, caused by the introduction of impurities during the growth of the ingot. These stresses cause compression or expansion deformations.

In this case, when the acceptor impurity is boron with an atomic radius $d_B = 0.87 \cdot 10^{-10}$ m, *p*-type Si is used [8]. Given that $d_B < d_{Si}$, compression deformations ε are formed in the silicon lattice, which can be represented by the following formula [7]:

$$\varepsilon = -\beta N_A, \quad (2)$$

where the "–" sign means that the deformation is compression; β is the compression coefficient associated with the solubility of the impurity in the lattice, defined as a change in the silicon lattice constant by 1 % of the introduced impurity; N_A is the impurity concentration.

Silicon ingots usually have a spread in resistivity $\Delta\rho$ at different ends [10]. Often this spread reaches 7-8 kOhm·cm, in the best case – $\Delta\rho$ = 1-2 kOhm·cm. In this case, the wafers obtained from an ingot of ρ = 16-20 kOhm·cm were used. From the formula of electrical conductivity [11], according to (3), it is possible to obtain limiting concentrations $N_A = 7.8\cdot10^{11}$ cm^{-3} and $N_A = 6.3\ 10^{11}$ cm^{-3} for *p*-type material (with provision for all acceptors are ionized at room temperature):

$$\sigma = 1/\rho = ep\mu_p \,, \qquad (3)$$

where σ is the electrical conductivity; μ_p is the mobility of holes; *e* is the electron charge; and *p* is the concentration of holes.

Given that the compression strains in Si are directly proportional to the impurity concentrations, it can be seen that even within a single ingot, the conditions for the occurrence of structural defects are different.

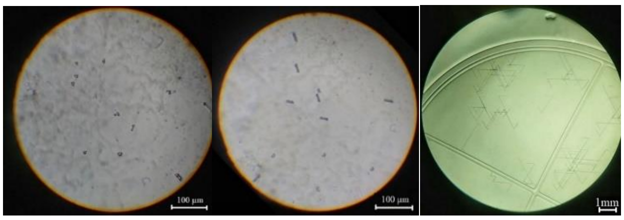
3.2 Influence of Phosphorus Diffusion on the Formation of Structural Defects

Since structural defects affect dark currents, it was decided to investigate the effect of the level of phosphorus doping on defect formation, in particular, dislocations. The surface of the PD was treated with a selective etchant and examined with optical microscopes (see Fig. 1).

It was noted that when impurity concentration decreases (surface resistance diminishes), the number of dislocations increases. Samples of R_S = 8.1 Ohm/□ and R_S = 5.0 Ohm/□, in particular, were characterized by single or double dislocations. In this case, the density of dislocations was $N_{dis}^{8.1}$ = 70-90 cm^{-2} and = $N_{dis}^{5.1}$ $1.2\cdot10^2$-$1.4\cdot10^2$ cm^{-2}. Note that for the source wafers, this parameter was N_{dis}^{Si} = 5-15 cm^{-2}.

Samples with R_S = 3.3 Ohm/□ were characterized by clusters of 2-3 dislocations and the formation of dislocation lines (DLs), which contained 2-4 dislocations (Fig. 1a). The concentration of dislocations in this case was $N_{dis}^{3.3}$ = $2.5\cdot10^2$-$3\cdot10^2$ cm^{-2}.

Fig. 1b shows the PD surface with R_S = 2.7 Ohm/□ after selective etching. The figure shows the structure of "short" dislocation lines, which consist of 2-5 structural defects. In this case, $N_{dis}^{2.7}$ = $2.4\cdot10^3$-$2.6\cdot10^3$ cm^{-2}. For samples with R_S = 2.4 Ohm/□, there was an increase in the lengths of dislocation lines and the formation of defective structures, which were a combination of DLs with mutual placement at an angle of 60°, which is typical for the [111] orientation. The density of dislocations was $N_{dis}^{2.4}$ = $0.9\cdot10^4$-$1.4\cdot10^4$ cm^{-2}.



a b c

Fig. 1 – Image of the PD surface after selective etching: a) R_S = 3.3 Ohm/□; b) R_S = 2.7 Ohm/□); c) R_S =1.9 - 2.1 Ohm/□

With a further increase in the concentration of phosphorus, there was an increase in dislocation structures and the formation of clusters of DLs, which were local dislocation networks (Fig. 1c). N_{dis} values reached $N_{dis}^{2.1}$ = $4\cdot10^4$ -$5\cdot10^4$ cm^{-2} and $N_{dis}^{1.9}$ = $6\cdot10^4$-$7\cdot10^4$ cm^{-2}.

According to the obtained values of the surface density of dislocations, a graph of $N_{dis} = f(R_S)$ dependence was made (Fig. 2).

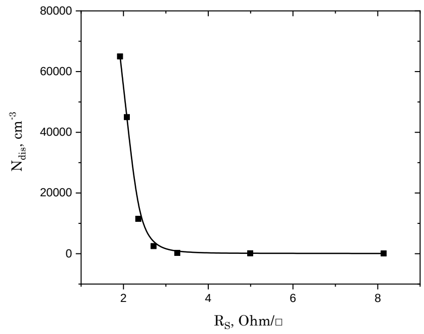


Fig. 2 – Graph of the concentration dependence of dislocations on the surface resistance

3.3 Contribution of Dislocations to the Level of Dark Current FDs

The presence of dislocations that are generation-recombination centers (GRC) affects the generation component of the dark current I_d^G [7]:

$$I_g^G = e\frac{n_i}{2\langle\tau\rangle}W_i A_{RE} \,, \qquad (5)$$

where *e* is the electron charge; n_i is the intrinsic concentration of charge carriers in the substrate; $<\tau>$ is the average value of the lifetime of charge carriers; W_i is the width of the space charge region (SCR); A_{RE} is the RE area.

In the manufacture of PDs, monocrystalline *p*-type silicon with resistivity $\rho \approx 18$ kOhm·cm was used, which corresponds to the concentration of charge carriers in the substrate $n_i \approx 7{,}7\cdot10^{11}$ cm^{-3}.

The width of the SCR can be determined by the formula [12]:

$$W_i = \left(\frac{2\varepsilon\varepsilon_0\left(\varphi_c - U_{bias}\right)}{eN_A}\right)^{\frac{1}{2}} , \qquad (6)$$

where ε and ε_0 are dielectric constants for silicon and vacuum, respectively; φ_c is the contact potential difference; U_{bias} is the bias voltage; N_A is the concentration of acceptors in the substrate (assuming that at room temperature all impurities are ionized, then $n_i = N_A$).

At U_{bias} = 120 V, $W_i \approx 490$ µm. But in this case, substrates with a thickness of about 440 µm were used, so taking into account the width of n^+-*p*- and p^+-*p*-layers, $W_i \approx 430$ µm.

With increasing generation and recombination centers, <τ> decreases, the value of which can be estimated by the following formula [13]:

$$\langle \tau \rangle = \frac{3}{8R_0 N_{Dis} \upsilon}, \qquad (7)$$

where R_0 is the radius of the SCR of the dislocation; υ is the average relative (relative to the center of recombination) velocity of thermal charge carriers, which is equal to $\upsilon = 1.56 \cdot 10^5$ m/s.

The radius of the SCR of the dislocation according to [7] is defined as:

$$R_0 = \left(\frac{f_0}{\pi c (N_D - N_A)} \right)^{\frac{1}{2}}, \qquad (8)$$

where f_0 is the Fermi distribution function; π is the mathematical constant; c is the distance between the broken valence bonds ($c = 3.34 \cdot 10^{-10}$ m for edge dislocations in silicon [7]).

The function f_0 can be determined from equation [7]:

$$f_0 = \frac{1}{1 + \exp\left(\frac{E_D - E_F}{kT} \right)}, \qquad (9)$$

where E_D is the energy level of the dislocation; E_F is the Fermi level; k is the Boltzmann constant; T is the temperature.

If we calculate <τ> for the level $E_D = (E_v + 0.6)$ eV [14] at the studied R_S and according to N_{dis}, we can see that at $N_{dis} \leq 3 \cdot 10^2$ cm^{-2} reduction of the lifetime of minority charge carriers does not occur, and the dislocation density reaches the initial value before heat treatment. To estimate <τ> for different N_{dis}, a calculated graph of the dependence <τ>(N_{dis}) is obtained (Fig. 3).

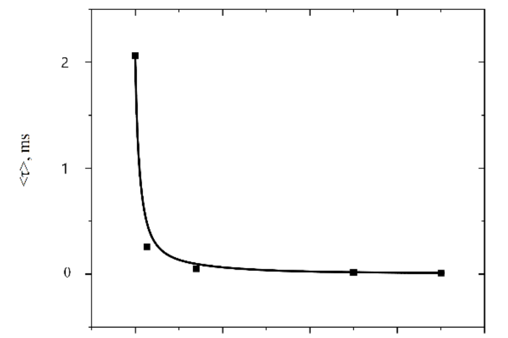


Fig. 3 – The calculated graph of the <τ> dependence on N_{dis}

The graph of the I_d^G dependence on N_{dis} is also obtained (Fig. 4). When calculating the generation component of the dark current, it was seen that at $N_{dis} = 2.6 \cdot 10^3$ cm^{-2}, which corresponds to $R_S = 2.7$ Ohm/□, $I_d^G = 0.42$ nA, and at $N_{dis} = 1.4 \cdot 10^4$ cm^{-2} ($R_S = 2.4$ Ohm/□), the contribution to the I_d^G reaches about 2 nA. Accordingly, when $N_{dis} \geq 10^4$ cm^{-2}, the contribution of dislocations to the level of the generation component of the dark current becomes significant.

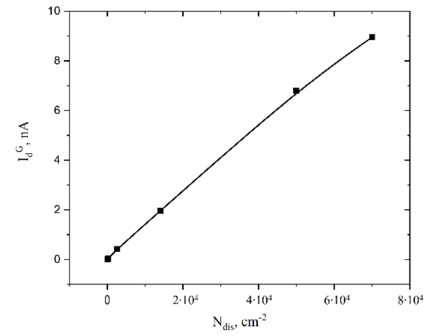


Fig. 4 – The calculated graph of the I_d^G dependence on N_{dis}

Note that the calculations described above were performed in the approximation that the dislocations are uniformly located in the high-impedance region, and not only in the n^+-layer. In real crystals, structural defects caused by the diffusion of impurities are located in the doped or adjacent areas. Although we studied the depth of dislocations by layer-by-layer etching of plates with subsequent selective treatment, we found the presence of dislocations at a depth of 20-30 μm and a thickness of the diffusion layer of phosphorus of 4-5 μm (further etching was not performed).

The presence of dislocations also affects the surface generation component of the dark current I_d^{surf} [12]:

$$I_d^{surf} = \frac{e N_{ss} \upsilon_{drift} \sigma_{ss} A_{p-n}}{2}, \qquad (10)$$

where σ_{ss} is the capture cross-sectional area, $\sigma_{ss} = 10^{-15}$ cm^2; N_{ss} is the density of surface states; A_{p-n} is the area that contributes to the surface component of the dark current, $A_{p-n} = 1.225 \cdot 10^{-3}$ cm^2.

If, according to (4), we calculate the contribution of the dislocation component at $N_{ss} = N_{dis}$, we see that at $N_{dis}^{1.9} = 6 \cdot 10^4$ -$7 \cdot 10^4$ cm^{-2}, $I_d^{surf} \approx 1 \cdot 10^{-25}$ A. Accordingly, the contribution of dislocations to the surface component of the dark current is much smaller than to the generation component. But on the surface of real plates there are not only dislocations, but also other generation and recombination centers, in particular point defects, the density of which can vary between 10^{10}-10^{13} cm^{-2} [7].

3.4 Spread of Dark Current Levels Across the RE and Dislocations

Depending on the obtained dark current and responsivity values, the level of surface resistance $R_S \approx$ 2-3.5 Ohm/□ is usually employed in technology of silicon p-i-n PDs (to visualize, formation of dislocations at $R_S = 8.1/5.0$ Ohm/□ is given [12]).

In commercial production of p-i-n PDs, it was observed that when the surface resistance decreased from $R_S \approx$ 3-3.5 Ohm/□ to $R_S \approx$ 2.2-2.4 Ohm/□, the percentage of good-to-bad responsive crystals yield dropped significantly: from ~ 70 % to ~ 55 %. Moreover, as it was mentioned above, about 10 % was the reject in external appearance, all the rest – in the spread of dark current levels of a PD RE. The above phenomenon was observed with no evident spread of interconnection resistance of the responsive areas and the GR or given the visual defects, which could be the cause of these faults.

The total level of dark currents decreased about 1.5 times, and the spread of levels in good products reached 10-20 % as compared to 50-70 % for PDs with $R_S \approx$ 3-3.5 Ohm/□. After conducting experimental batches with R_S = 1.9-2.4 Ohm/□, it was noticed that the I_d levels in these cases do not differ, but when R_S decreases, the percentage of defects in the failure of one area grows and is more pronounced (spread of I_d values by 20-30 times) (Table 2).

In samples with R_S = 2.7 Ohm/□, with a slight increase in I_d levels relative to PDs with R_S = 1.9-2.4 Ohm/□, the incidence of a RE rejected is much lower (percentage of good-to-bad crystals yield ~ 65 %) and is characterized mainly by 2-3 times spread in REs.

To determine the nature of this type of defects, faulty crystals were examined using selective etching. It was noted that REs of a high level of I_d were characterized by an increased concentration of dislocations as compared to the characteristic density for good crystals at a given R_S.

The first admissible reason for the spread of dark currents or the distribution of dislocations is non-uniform diffusion from planar sources of phosphorus. To determine the uniformity of distribution of the surface resistance, a control process is carried out before the introduction of the sources. Fig. 5 represents the characteristic result of the process. It can be seen that R_S non-uniformity is minimal.

Table 2 – Characteristic values of J_d of defective samples due to failure of one RE

R_S, Ohm/□	J_d, nA/cm^2			
2.7	106.8	109.6	123.3	274.0
	268.5	120.5	93.2	106.8
2.4	79.5	90.4	383.6	84.9
	882.2	90.4	87.7	87.7
2.1	90.4	82.2	2082.2	79.5
	90.4	87.7	821.9	95.9
1.9	3013.7	93.2	90.4	84.9
	76.7	90.4	6027.4	87.7

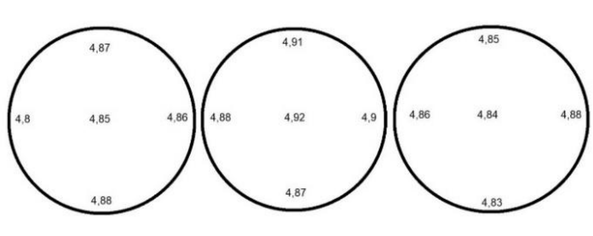


Fig. 5 – Distribution of surface resistance across silicon wafers after phosphorus predeposition

The actual reasons for dislocations distribution non-uniformity may be the irregular distribution of point defects generated during oxidation and the presence of microdefects formed during mechanical or chemical-dynamic polishing (Fig. 6). Accordingly, these phenomena are manifested to a greater extent at high impurity concentrations and contribute to the increase in dark currents by decorating dislocations with impurities or creating additional energy levels in the band gap.

An increase in the probability of the occurrence and nature of I_d spread may be caused by growth in the capture cross-sectional area of the dislocation when phosphorus concentration increases. That is, as the impurity concentration increases, not only N_{dis}, but also σ_{ss} grows. After all, the physical content of σ_{ss} is the outer area of the cylindrical SCR formed around the dislocation, the length of which grows with an increase in the impurity concentration due to the gain in the amount of mechanical stresses.

The non-uniformity of I_d disribution across the RE may be also caused by point defects disposition in the bulk of the ingot, and, accordingly, in the bulk of the wafer, created in the process of growth (growth defects). The location of these defects is often a spiral – the so-called swirl-distribution (Fig. 7). Colonies of point defects with a swirl distribution can cross the entire ingot [7]. These defects may be the centers of dislocations origin.

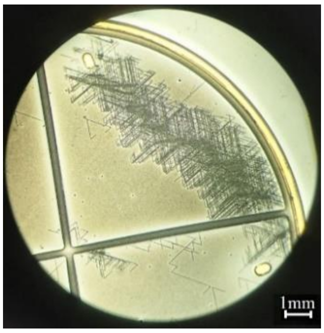


Fig. 6 – REs of defective crystals with non-uniform distribution of defects

Fig. 7 – Complexes of swirl defects

Probably, when locally increased numbers of growth defects and point defects acquired during mechanical, chemical or thermal operations are superimposed, critical faults and spread of dark currents with maximum values are observed.

4. CONCLUSIONS

1. Silicon quadrant p-i-n PDs with different concentrations of diffused phosphorus in the n^+-layer were fabricated, and the formation of dislocations at different concentrations and their effect on dark currents were studied.

2. The density of dislocations in silicon wafers, formed as a result of the same technological modes and operations (the same R_S after phosphorus diffusion, in particular), depends on the source material: the concentration of point defects, the presence of oxygen precipitates, resistivity.

3. Due to the discrepancy of the resistivity along the length of the ingot, the conditions of structural defects are different.

4. When phosphorus concentration increases, the number of edge dislocations grows.

5. When calculating the generation component of the dark current, it was seen that at $N_{dis} = 2.6 \cdot 10^3$ cm^{-2}, which corresponds to R_S = 2.7 Ohm/□, I_d^G = 0.42 nA, and at $N_{dis} = 1.4 \cdot 10^4$ cm^{-2} (R_S = 2.4 Ohm/□), the contribution to the I_d^G reaches about 2 nA. Accordingly, when $N_{dis} \geq 10^4$ cm^{-2}, the contribution of dislocations to the

level of the generation component of the dark current becomes significant.

6. The contribution of dislocations to the surface component of the dark current is calculated, and it is shown that the contribution of dislocations formed in good crystals due to phosphorus diffusion even at $R_S = 1.9$ Ohm/□ ($N_{dis}^{1.9} = 6 \cdot 10^4$-$7 \cdot 10^4$) is negligible and reaches the order of 10^{-25} A.

7. It is shown that the reason for a significant spread in the dark current levels is the non-uniform distribution of dislocations over the wafer.

8. The reasons of non-uniform distribution of dislocations are non-uniform distribution of point defects generated by oxidation and the presence of microdefects formed during mechanical or chemical-dynamic polishing, as well as the heterogeneity of point defects in the bulk of the ingot (respectively in the bulk of the wafer).

9. The nature and probability of manifestation of the homogeneity of structural defects distribution and their impact on dark currents increases with increasing impurity concentration.

10. It is assumed that when superimposing growth defects and point defects caused by mechanical, chemical or thermal operations, critical faults and spread of dark currents with maximum values are observed.

11. To minimize the manifestation of critical spread of dark currents, it is recommended to obtain the value of the surface resistance $R_S \approx 2.7$ Ohm/□ by diffusion, which, at relatively low levels of I_d, is characterized by a low probability of non-uniform distribution of edge dislocations.

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Утворення дислокацій при легуванні фосфором в технології кремнієвих *p*-i-*n* фотодіодів та їх вплив на темнові струми

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При виготовленні *p-i-n* фотодіодів (ФД) на основі кремнію *p*-типу провідності встановлено, що при збільшенні часу дифузії фосфору суттєво знижується відсоток виходу придатних виробів. До 10 % складає брак по зовнішньому вигляду, решта – по розкиду рівнів темнових струмів фоточутливих елементів (ФЧЕ) одного ФД. Імовірною причиною описаного міг бути нерівномірний розподіл дефектів по ФЧЕ, спричинений збільшенням концентрації домішки фосфору. Даний факт потребував додаткового дослідження для визначення причини появи нерівномірного розподілу темнових струмів та встановлення оптимальної концентрації домішки, яка б забезпечувала низький темновий струм при мінімальному розкиді. Для дослідження впливу поверхневого опору n^+-шару на концентрацію дислокацій та їх розподіл було виготовлено ФД із різною тривалістю дифузії фосфору, відповідно із різним значенням поверхневого опору. Для виявлення природи розкиду темнових струмів по фоточутливих елементах, браковані кристали досліджувались із застосуванням селективного травлення. Встановлено, що умови виникнення структурних дефектів в межах одного злитка можуть бути неоднакові за рахунок розкиду питомого опору. Досліджено залежність густини дислокацій від поверхневого опору після дифузії фосфору. Аналітично вирахувано внесок дислокацій в генераційну та поверхневу складові темнового струму Побачено, що ФЧЕ, які володіли підвищеним рівнем темнового струму, була притаманна підвищена концентрація дислокацій порівняно із характерною густиною для придатних кристалів при даному поверхневому опорі. Фактичними причинами нерівномірності розподілу дислокацій є нерівномірність розподілу точкових дефектів, згенерованих при окисленні та наявність мікродефектів утворених під час механічного чи хіміко-динамічного полірування. При накладанні локально підвищеної кількості «ростових» дефектів та точкових дефектів, набутих у процесі механічних, хімічних чи термічних операцій, спостерігаються критичні несправності та розкиди темнових струмів з максимальними значеннями.

Ключові слова: Фотодіод, Поверхневий опір, Темновий струм, Дислокація.