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Implementation and Analysis of an L-Shaped Tunnel Field Effect Transistor by Incorporating Gate and Oxide Engineering

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In this paper, an L-shaped tunnel FET (TFET) with the dominant tunneling current along the gate region with gate and oxide engineering is proposed and its electrical characteristics are investigated using TCAD simulations. The band-to-band tunneling (BTBT) takes place near the gate region and the L-shaped structure is to suppress corner tunneling. A triple material (TM) gate structure is formed with three different work functions (WFs) and the drain current performance is simulated and compared with single material (SM) gate L-shaped TFET. The structure is simulated and compared with different dielectric oxides. The subthreshold slope is determined for various voltages, and it gives 40 mV/dec. The analysis is done by the slotboom model for considering impact of doping concentration on energy bandgap narrowing in source/drain regions. The main objective is to minimize the subthreshold swing (SS), reduce leakage current and increase the ON to OFF current ratio by varying the parameters and simulating using Sentaurus Technology Computer Aided Design (TCAD) tool. A new structure is formed with oxide and gate engineering. The existing parameters are varied, and the performance is improved with less subthreshold slope, less leakage current and increase in the I_{ON} to I_{OFF} current ratio.

Keywords: Triple material (TM) gate, Band-to-band tunneling (BTBT), L-shaped tunnel FET (TFET), Work function (WF), Electric potential, Corner tunneling, Subthreshold swing (SS).

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1. INTRODUCTION

In real time, metal-oxide-semiconductor field-effect transistors (MOSFETs) have been widely used for many applications because of their symmetric structure as the source and drain are interchangeable. [1]. There are short channel effects such as threshold voltage roll-off, drain induced barrier lowering (DIBL) and hot carrier effect due to transistor scaling. MOSFETs produce subthreshold swing (SS) greater than 60 mV/dec at room temperature and high ON-to-OFF current ratio as the operating voltage is scaled down [2]. In order to reduce the SS less than 60 mV/dec, various novel devices have been found such as impact-ionization MOS devices [3, 4], nano-electro-mechanical FETs [5] and tunnel FETs (TFETs) [6-8]. TFET is considered as one of the promising candidates for the ultra-low power application due to scalability in complementary MOS devices [9]. The recently proposed dual material gate MOSFET shows high suppression of short channel effects and leakage current without sacrificing driving ability. There are different dielectrics with high k values. To reduce the leakage current, high-k dielectric materials having high permittivity are normally used.

Gate engineering is efficient by altering the pattern of electric field and surface potential along the channel [10]. Dielectric-based TFET is proposed to overcome the drawback of normal TFET. Dielectric based TFET is dielectric barrier tunneling based which reduces ambipolar effects in the OFF stage. The drain current is reduced multiple times in dielectric based TFET because of extra barrier formation between source and drain. The fabrication process flow is also described [11]. The dual material gate with different work functions (WFs) gives better performance due to potential step at interface which reduces short channel effects. WFs are given in order of maximum value near the source and minimum value near the drain for an n-channel transistor [12, 13]. Higher WF near the source leads to better acceleration of carriers in the channel, and lower WF near the drain is for reducing electric field near the drain, which in turn reduces hot carrier effect. For dual gate material engineering, WF of the first metal gate should be greater than that of the second metal gate in an n-channel MOSFET, and WF of the second metal gate should be greater than that of the first metal gate in a p-channel MOSFET.

The advantage of triple material (TM) gate engineering is done to enhance the performance of the existing single material (SM) gate in an L-shaped TFET. The proposed structure is of three material based electrode of different WFs which allows better gate control of the channel and increases the drain resistance, thus improving the transport efficiency of the gate. The following sections are discussed in this paper: (2) Device Structure, (3) Results and Discussion, (4) Conclusions.

2. DEVICE STRUCTURE

Fig. 1 illustrates the schematic view of the existing SM L-shaped TFET formed using TCAD simulation tool. In the present work, the switching characteristics of the L-shaped TFET are discussed with doping engineering, and the process integration is also given for fabrication feasibility [14].

In Fig. 2, SM gate is replaced with TM gate. The parameters of the proposed device are: 20 nm gate length, 1 nm oxide thickness, 4 nm channel thickness, 80 nm source height, 30 nm source length, 30 nm drain length, 10 nm body thickness, 20 nm pocket height, 24 nm pocket length, 1×10^{15} cm^{-3} source doping,

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1×10^{18} cm^{-3} drain doping, 2.5×10^{15} cm^{-3} pocket doping and 5×10^{17} cm^{-3} body doping. From the structure, it is seen that the gate electrode is of three different WFs (φ) based materials M1, M2 and M3 that are deposited in the height H1, H2 and H3. WFs for the first, second and third gates are $\varphi1$, $\varphi2$ and $\varphi3$ for a *p*-channel transistor. The total height is 96 nm which is split into three equal heights. The gate material near the source with the lowest WF is termed as control gate. The material with the next higher function in between the source and drain is the first screen gate, and the third material with the highest work function near the drain is the second screen gate. The device is composed three WFs: the first WF WK1 is 4.4 eV (Ti), the second WF WK2 is 4.6 eV (Mo), and the third WF WK3 is 4.8 eV (Au) [15]. In the Synopsys Sentaurus TCAD, the device has been analyzed by employing various physical models, for example, drift diffusion (DD) model. The effects of doping concentration and electric field are studied by the mobility model (MM). The carrier lifetime is predicted by the band gap narrowing model (BNM) and Shockley-Read-Hall (SRH) recombination model [16, 17]. The fabrication flow of SM L-shaped TFET has been explained [14].

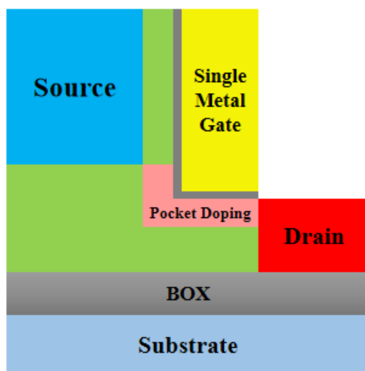

Fig. 1 – Schematic view of existing L-shaped TFET

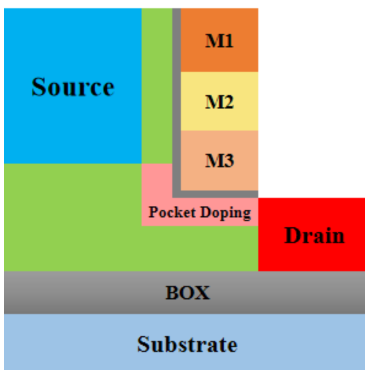

Fig. 2 – Schematic view of the proposed TM L-shaped TFET

3. RESULTS AND DISCUSSION

The transfer characteristics of the experimental L-shaped TFET and simulated TCAD results are shown in Fig. 3. It is seen that the experimental results and TCAD simulated results are same.

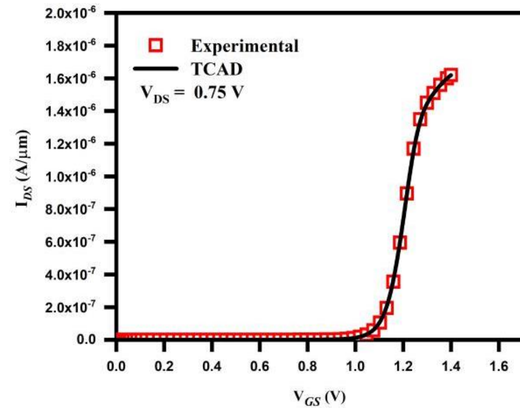

Fig. 3 – Experimental L-shaped TFET and simulated TCAD results

3.1. Electric Potential

Fig. 4 shows the comparison of electric potentials for SM gate and TM gate. The values are $V_D = 1.3$ V and $V_D = 1.4$ V, respectively. In the SM gate, it is seen that the electric potential monotonically increments from the source to the drain, while there is a sudden change in different gate materials in the TM gate. It is seen that there are two downsides in the SM model. In the first place, the I_{OFF} current increases due to a low negative potential, causing leakage current in the drain region. Second, as electrons move from the source to the drain, there is a decrease in the carrier velocity and mobility due to electric potential increment.

In the event of TM gate, a low electric potential is observed in the M1 region. This shows less influence of the drain current after saturation with respect to V_D. This assists with reducing the channel conductance and subsequently the effect of DIBL. In the saturation region, M3 assimilates extra V_D, and M1 is subsequently screened from potential variations in the drain, where M2 and M3 act as screening gates. Because of differing electric potentials, there is a decrease in the effect of high velocity moving electrons. Hence, hot carrier effects decrease and carrier transport efficiency increases.

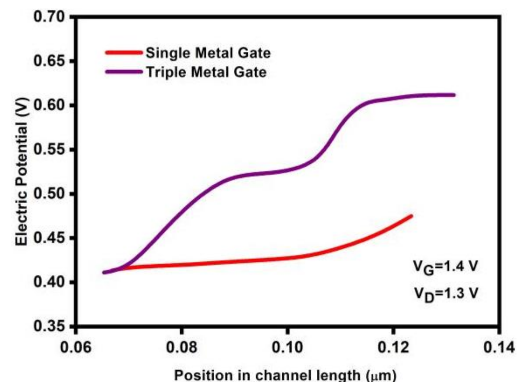

Fig. 4 – Electric potential variation of the proposed TM and SM L-shaped TFETs

3.2. Drain Current

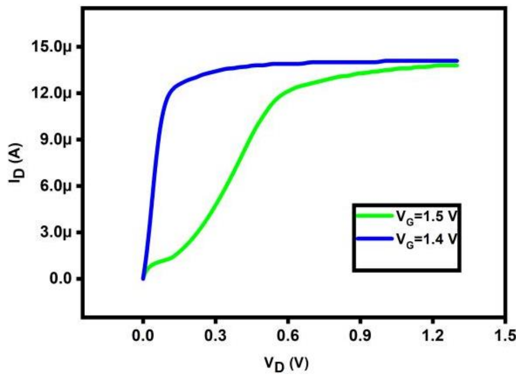

Fig. 5 – Output characteristics of TM L-shaped TFET by varying gate voltage

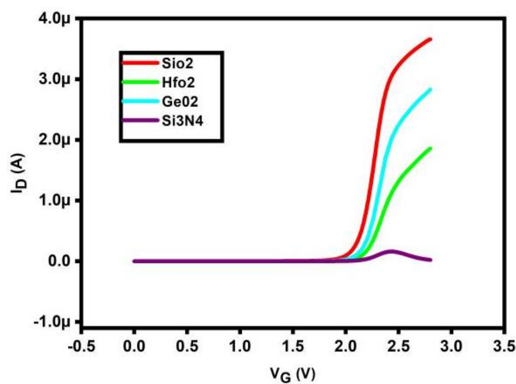

Fig. 6 – Transfer characteristics of SM L-shaped TFET for various dielectric materials

Fig. 5 shows the output characteristics of the proposed TM gate L-shaped TFET. The WFs are the following: WK1 = 4.4 eV, WK2 = 4.6 eV, WK3 = 4.8 eV. A voltage of 1.4 V and 1.5 V is applied to the gate terminal to on-current of the transistor. It is observed a better current performance with the above WFs.

Fig. 6 shows the transfer characteristics of the proposed structure simulated and compared with various dielectric oxides such as silicon dioxide (SiO_2), hafnium oxide (HfO_2), germanium dioxide (GeO_2) and silicon nitride (Si_3N_4). It is seen that silicon dioxide gives better performance when compared to other oxide materials.

Fig. 7 shows the subthreshold swing (SS) plot for different gate voltages with SS = 40 mV/dec for V_G = 1.1 V, which is less than the ideal SS value. Therefore, this can be used for low power applications.

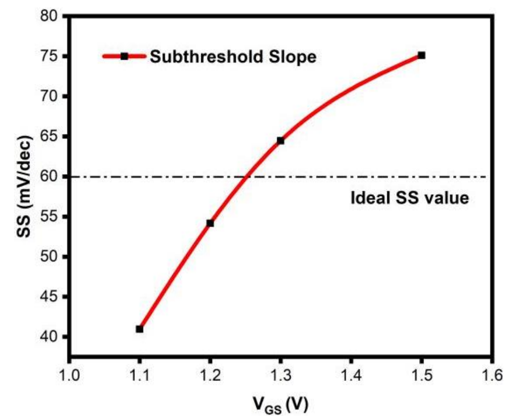

Fig. 7 – Subthreshold slope for different gate voltages

4. CONCLUSIONS

In this paper, implementation and performance analysis of TM gate L-shaped TFET with respect to the electric potential has been carried, and it shows better performance when compared with SM gate L-shaped TFET. The transfer characteristics of SM gate L-shaped TFET are simulated with various oxide materials and compared. The subthreshold slope less than the ideal value is observed. This study proves that TM gate has better I_{ON}/I_{OFF} ratio and lower SS, which makes it suitable for low power applications. This paper can be further improved by implementing inverter circuit.

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Реалізація та аналіз L-подібного тунельного польового транзистора з використанням затвора та оксидної інженерії

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У статті пропонується L-подібний тунельний польовий транзистор (TFET) з переважним тунельним струмом вздовж області затвора з використанням затвору та оксидної інженерії, а електричні характеристики транзистора досліджуються з використанням моделювання TCAD. Міжзонне тунелювання (BTBT) відбувається поблизу області затвора, а L-подібна структура призначена для придушення кутового тунелювання. Структура затвора із потрійним матеріалом (TM) сформована з трьома різними роботами виходу (WFs), а характеристики струму стоку змодельовані та порівняні з L-подібним TFET із затвором з одного матеріалу (SM). Структура моделюється та порівнюється з використанням різних діелектричних оксидів. Підпороговий нахил визначено для різних напруг і складає 40 mV/dec. Аналіз виконано за допомогою моделі slotboom для визначення впливу концентрації легуючої домішки на звуження забороненої зони в областях витоку/стоку. Основна мета роботи полягає в тому, щоб звести до мінімуму підпорогове коливання (SS), зменшити струм витоку та збільшити відношення струмів I_{ON}/I_{OFF} шляхом зміни параметрів та моделювання за допомогою інструменту автоматизованого проектування Sentaurus TCAD. Нова структура формується із застосуванням затвора та оксидної інженерії. Існуючі параметри змінюються, а продуктивність покращується за рахунок меншого підпорогового нахилу, меншого струму витоку та більшого відношення струмів I_{ON}/I_{OFF}.

Ключові слова: Затвор із потрійним матеріалом (TM), Міжзонне тунелювання (BTBT), L-подібний тунельний польовий транзистор (TFET), Робота виходу, Електричний потенціал, Кутове тунелювання, Підпорогове коливання (SS).