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High Temperature Effects on the Static Performance of 14 nm TG SOI N FinFET

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The persistent scaling of feature sizes of metal–oxide–semiconductor field- effect transistors (MOSFETs) is described by Moore's law which lead to the development of sophisticated electronic component technologies. Due to the difficulties in planar CMOS transistor scaling with the hope to preserve a good and acceptable channel control, FinFET devices have been introduced to overcome the different problems such as the increase of the leakage current, the decrease of the ON current and therefore the degradation of the performance ratio. FinFET devices have other important advantages over planar transistor such as reduced random doping fluctuation and the increase the threshold voltage. The BSIM Group continues to develop models for complementary metal–oxide–semiconductor technology by introducing device geometry-dependent, material-independent compact models which is essential for electronics designs. In this paper we investigate the effects of temperature variations from 77 to 377 K on the input and output characteristics of TG SOI N FinFET 14 nm. The aim of the study is to find out how temperature affects the threshold voltage, the ON and OFF currents, the Subthreshold Swing (SS), the Drain Induced Barrier Lowering and the leakage current. The Berkeley PTM (Predictive Technology Model) is used in SPICE and TCAD Atlas tools. While increasing the temperature from 77 to 377 K, the degradation of the performance ratio I_{ON}/I_{OFF} is observed.

Keywords: CMOS, Quantum effect, Leakage current, FinFET, Temperature effect.

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1. INTRODUCTION

MOSFETs have served the electronic industry in the past 50 years and to improve its performance, engineers have managed to change its structure. FinFET is the alternative new device after the emergence of the MOSFET deterioration of its performance at scales below 22 nm [18].

The FinFET structure requires a new design to improve its performance and to address the different problems namely the gate and subthreshold leakage currents, the increase of threshold voltage and the control of the SCE (Short Channel Effects) [17].

Nowadays, the new structure is TG (tri gate) SOI (semi-conductor on insulator) N FinFET, it has shown high reliability and technological manufacturability for Nano scale devices.

In this paper, the temperature effects in TG SOI N FinFET 14 nm are investigated with Silvaco TCAD Atlas tools and SPICE. The thermal characterization is crucial in evaluating its performance, reliability and the impact of the SCE on the device. We used in this simulation Hafnium Dioxide and the Berkeley PTM (Predictive Technology Model) parameters

2. DEVICE STRCTURE

The TG SOI N FinFET 14 nm is represented by different parameters like gate length (L_G), channel length (L), fin width (W), fin height (H_{fin}) and oxide thickness (t_{ox}). The aluminum gate work function used in this simulation is $\Phi_M = 4.85$ eV [1].

Hafnium Dioxide is used in this simulation to reduce the leakage current from the gate to the channel.

Table 1 displays the different geometric parameters used in this simulation, Silvaco TCAD atlas tools and SPICE have been used in the modeling of the structure of the device. Spice is used to simulate its output and transfer electrical characteristics. The numerical simulation of the device requires a good choice of the parameters. SRH (Shockley Read Hall) theory is used to account for the generation of charge carriers in the channel [6].

Table 1 – The geometric parameters [7]

Parameter	L	t_{ox}	V_{dd}
Value	14 nm	1.3 nm	0.8 V

Where L is the channel length, t_{ox} is the oxide thickness, V_{dd} is the supply voltage.

Table 2 – The operating parameters [7]

Parameter	Affinity (Si)	Affinity (HfO_2)	κ(HfO_2)
Value	4.05 eV	1.0 eV	24

3. DEVICE SIMULATION

The threshold voltage expression can be represented by the following equation [2]:

$$V_{TH} = \Phi_{ms} + 2\Phi_f + \frac{Q_D}{C_{ox}} + \frac{Q_{ss}}{C_{ox}} + V_{in}, \quad (1)$$

where Φ_{ms} is the work functions difference between gate and F_{in}, Q_{SS} is the charge in the gate dielectric, C_{OX} is the oxide capacitance, Q_D is the depletion charge, Φ_f is the Fermi potential, V_{in} is the input voltage

The variation of the transconductance is defined by the following equation [4]:

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$$g_m = \frac{dI_D}{dV_{GS}}, \tag{2}$$

One of the critical electrical parameters such as subthreshold swing is represented by the following equation: (2-4).

$$SS(mV/dec) = \frac{dV_{GS}}{d(\log_{10} I_{DS})}, \tag{3}$$

$$SS = \eta V_T \ln(10), \tag{4}$$

$$SS = \left(1 + \frac{C_d}{C_{ox}}\right)\left(\frac{k_B T}{q}\right)\ln(10), \tag{5}$$

where $\eta = \left(1 + C_d/C_{ox}\right)$ represents the body coefficient.

C_d is depletion capacitance, V_T is thermal voltage, k_B is Boltzmann constant, q is electron charge.

The DIBL is represented by the following equation*:*

$$DIBL\left(mV/V\right) = \frac{dV_{TH}}{dV_{DS}}, \tag{6}$$

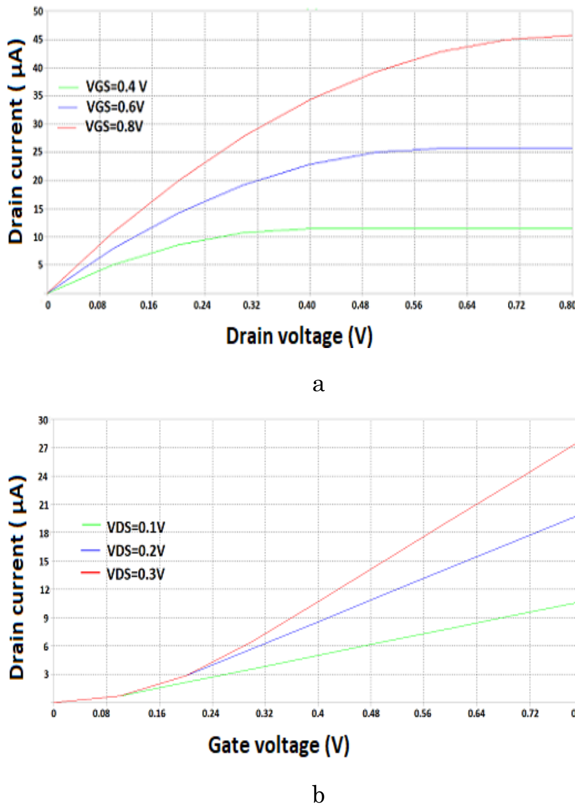

Fig. 1 – Output characteristic for TG SOI N FinFET (a), Transfer characteristic for TG SOI N FinFET (b)

Fig. 1 (a) illustrates the output characteristics for TG SOI N FinFET 14 nm when the gate voltage is swept from 0 to 0.8 V for V_{GS} = 0.4 V, V_{GS} = 0.6 V and V_{GS} = 0.8 V using Spice.

The drain current saturation V_{DSAT} is the maximum value of drain current when V_{DS} = V_{DD}. We notice that the drain current saturation increases with the increase of the gate voltage. The maximum value of drain current saturation in this simulation is 46 μA.

The increase of V_{GS} will result in higher channel conductivity, and hence lower channel resistivity. It can be easily observed from Fig. 2 that the current flattens up with increasing gate length.

The current level depends on the gate length and gate voltage, which determine the number of charge carrier velocity. However, the transit time of the charge carrier from source to drain is improved with shorter gate length which gives faster transistor switching [19].

Fig. 1 (b) illustrates the transfer characteristics for TG SOI N FinFET 14 nm when the gate voltage is swept from 0 to 0.8 V for V_{DS} = 0.1 V, 0.2 V and 0.3 V using Spice.

The On-current shows the driving capability of the device. It is defined as drain to source current when V_{GS} = V_{DD} = 0.8 V.

We notice that the increase of V_{DS} increases the inversion charge density which itself increases the threshold voltage and the ON current.

DIBL (Drain Induced Barrier Lowering) is one of the harmful parameters for the device, it represents the variation of the threshold voltage as a function of drain voltage at V_{DS} = 0.05 V and V_{DS} = 1 V.

The DIBL value of the device at room temperature is 36.4 mV / V. As transistor dimensions are scaled down to reduce power consumption, to minimize parasitic capacitances, to reduce the subthreshold slope (SS) in the device and consequently improve circuit speed. The value of subthreshold slope in this simulation at room temperature is 62.77 mV / dec.

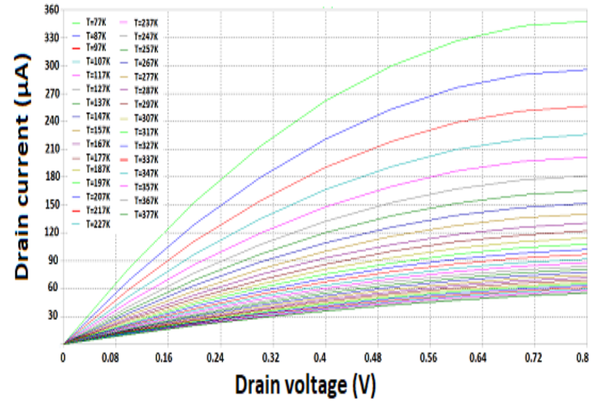

Fig. 2 – Output characteristics for TG SOI N FinFET 14 nm for different temperatures

Fig. 2 illustrates the output characteristics for TG SOI N FinFET 14 nm when the gate voltage is swept from 0 to 0.8 V for different values for temperature using Spice software.

The temperature is swept from 77 K to 377 K. We notice that the drain current saturation is from 345 × 10 − 6 A at T = 77 K to 50 × 10 − 6 A at T = 377 K.

Fig. 3 illustrates the variation of the saturation drain current when the temperature is swept from 77 K to 377 K. at V_{DS} = 0.8 V and V_{GS} = 1 V.

We notice that the drain current saturation decreases when the temperature increases and the maximum value is 350 × 10 − 6 A.

The increase of temperature results in lower channel conductivity and hence a higher channel resistivity. The drain current saturation decreases [21].

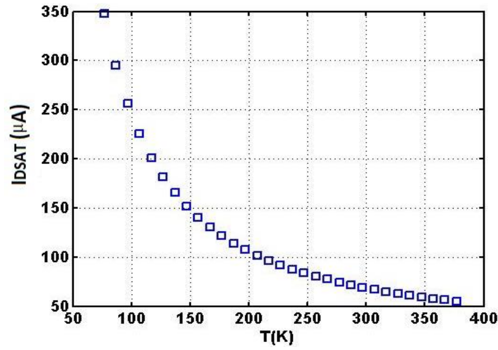

Fig. 3 – Drain current saturation variation with temperature

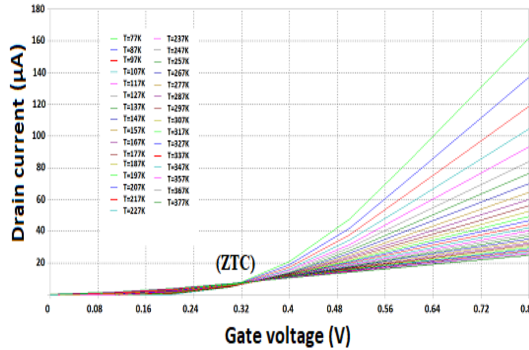

Fig. 4 – Transfer characteristics for different temperatures [12]

Fig. 4 illustrates the transfer characteristics for TG SOI N FinFET 14 nm when the gate voltage is swept from 0 to 0.8 V for different values for temperature using Spice.

We notice that the drain current increases when the gate voltage is swept from 0 to 0.8 V and the ZTC (Zero Temperature Change) for the device is 0.32 V.

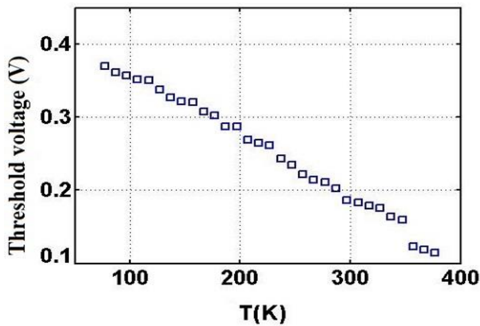

Fig. 5 – Threshold voltage variation with temperature

Fig. 5 illustrates the variation of threshold voltage with temperature, we notice that the threshold voltage decreases with the increase of temperature.

The threshold voltage is a critical parameter for FinFET operation, it influences the static and dynamic operating modes.

The decrease of the threshold voltage V_{TH} is due to the decrease of the Fermi level Φ_f in equation (1). Quantum confinement of the electrons within the sub-bands [10-13].

Fig. 6 illustrates the variation of the subthreshold slope with temperature, we notice that the subthreshold slope decreases down to room temperature, and then it starts increasing with temperature [14].

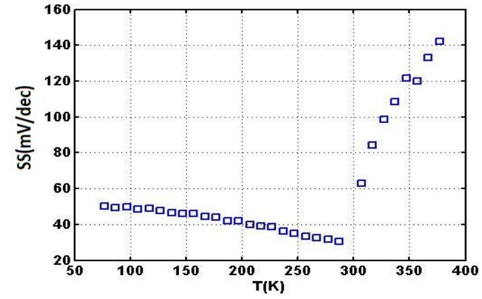

Fig. 6 – Subthreshold slope variation with temperatures

High temperature values tend to increase the capacitance which ultimately decreases the direct leakage current which correspondingly improves Subthreshold Slope [20].

Low temperature decreases the capacitance which decreases the Subthreshold Slope [15].

The Subthreshold Slope (SS) at room temperature is better than calculated by Ajay Kumar [15]

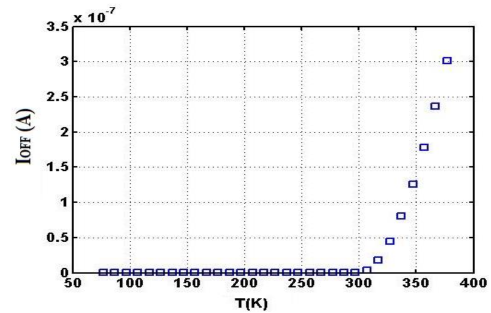

Fig. 7 – Leakage current variation with temperature

Fig. 7 illustrates the variation of the leakage current for different temperatures, we notice that the leakage current increases with the increase of temperature [5].

This can be explained by the fact that the energy gap E_g decreases when the temperature increases, so that Band Bending at the Oxide interface becomes equal or greater than the energy gap E_g of the drain material, hence Band-to-Band tunneling will take place and is activated in the simulation, this shows a contribution to the drain current intensity [8].

The electrons in the valence band of the n-type drain will tunnel through the thinned band gap into the conduction band, and they will be collected at the drain contact and form part of the drain current, whereas the remaining holes will be collected at the source contact and will contribute to the source leakage current [8-13].

Consequently, we have an increase of leakage current in the device with temperature.

The TAT (Trap Assisted Tunneling) current through the gate oxide materials is caused by defects in the high k dielectric material [11].

The result shows TAT is dominant over that direct tunneling until 300 K, then as T increases, direct tunneling will be dominant and it generates a big leakage current, hence its increase. [11].

Fig. 8 illustrates the variation of the performance ratio I_{ON}/I_{OFF} when the temperature varies from 77 K to 377 K. We notice that the performance of the device decreases with the increase of temperature.

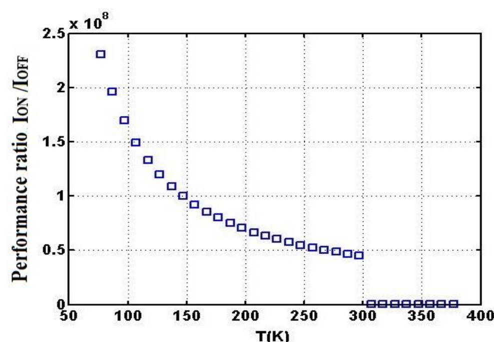

Fig. 8– Ratio I_{ON} / I_{OFF} performance

The decrease of the performance I_{ON} / I_{OFF} ratio is linked to the increase of the tunneling currents (Band to Band Tunneling and Trap Assisted Tunneling).

The tunneling current increase is due to the choice of the geometric parameters like oxide thickness which leads to the raising of the conduction band, so we have more leakage current between the gate and the channel.

The higher performance ratio for this simulation is $2.4 \times 10^8 > 10^6$ which shows that the device operation is good at $T = 77$ K [3-9].

We note that the performance ratio I_{ON} / I_{OFF} at room temperature is better than that calculated by Bourahla et al [16].

4. CONCLUSION

In this paper, we have analyzed the performance of TG SOI N FinFET 14 nm with SPICE and Silvaco TCAD Atlas tools, the new structure exhibits a good performance using Hafnium Dioxide and silicon used in the channel. The temperature effects on the electrical parameters such as threshold voltage, subthreshold slope, leakage current, ON current and transconductance are extracted and studied. The device was studied in the temperature range: 77 K to 377 K. As expected, temperature rise decreases the performance of the device and we think the best operating temperature of any circuit made from this device should be equal or below 300 K.

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Вивчення впливу високої температури на статичні характеристики 14 нм TG SOI N FinFET

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Постійне масштабування розмірів польових транзисторів метал-оксид-напівпровідник (MOSFET) описується законом Мура, що призводить до розробки складних технологій електронних компонентів. Через труднощі масштабування планарного CMOS-транзистора з надією на збереження ефективногокерування каналом, пристрої FinFET були представлені для подолання різних проблем, таких як збільшення струму витоку, зменшення струму ввімкнення та погіршення коефіцієнта продуктивності. Пристрої FinFET мають інші важливі переваги перед планарними транзисторами, такі як зменшення випа-

дкових флуктуацій легування та підвищення порогової напруги. Група BSIM продовжує розробляти моделі для комплементарної технології метал-оксид-напівпровідник, представляючи компактні моделі, що залежать від геометрії пристрою та не залежать від матеріалу, що є важливим для проектування електроніки. У даній роботі був досліджений вплив зміни температури від 77 до 377 К на вхідні та вихідні характеристики TG SOI N FinFET 14 нм. Мета дослідження полягає в аналізі впливу температури на порогову напругу, струми увімкнення та вимкнення, підпорогове коливання, зниження бар'єру, викликане стоком, та струм витоку. Berkeley PTM (Predictive Technology Model) використовується в інструментах SPICE і TCAD Atlas. При підвищенні температури від 77 до 377 К спостерігається погіршення співвідношення продуктивності I_{ON}/I_{OFF}.

Ключові слова: CMOS, Квантовий ефект, Струм витоку, FinFET, Температурний ефект.