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REGULAR ARTICLE

Resistance Based Drain Current Model of Surrounded Channel Junction Less Field Effect Transistor

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A resistance based analytical model for drain current of a Junction less field effect transistor with surrounded channel (SCJLFET) is reported in this paper. Surrounded channel junction less field effect transistor (SCJLFET) exhibits the merits of both double and single gate Junction less field effect transistor. This paper illustrated the uses of resistance of the channel to obtain the drain current. The model is based on the concept that channel of a JLFET is comprised of either a space charge layer or a neutral layer or an accumulation layer or combination of any two of these layers. The model development starts with the formulation of resistances of these three types of layers followed by determination of total channel resistance in the four modes of operation of a JLFET. In the sub threshold mode only depletion layer is present while in bulk current mode total resistance is obtained by parallel combination of neutral semiconductor and depletion resistances. In flat band mode only neutral semiconductor layer is present while in accumulation mode total resistance is obtained by parallel combination of accumulation and depletion resistances. The drain current model in four modes is obtained by dividing the potential difference across the channel with the corresponding resistances of the modes. It is simplified model based on resistance of the body of the device. The model developed is fully analytical in nature which reduces the computation time in designing. The model is full range model applicable in all the operation modes of surrounded channel Junction less field effect transistor (SCJLFET). The potential expression also obtained using Poisson's equation. The analytical drain current model has been verified with the help of TCAD numerical simulation results by comparing the transfer and output characteristics of the device obtained from TCAD and the drain current model.

Keywords: Drain current Model, Double gate, JLFET, Surrounded channel, SCJLFET, TCAD.

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1. INTRODUCTION

Junction less field effect transistor (JLFET) exhibits superior characteristics compared to other MOSFET structure [1-4]. However, JLFET suffers from few serious drawbacks regarding switching [5-17]. As a consequence, the minimum number for gate requirement for JLFET is two. Monogate JLFET has some advantages regarding on characteristics as well simpler configuration. Therefore, a novel structure namely surrounded channel JLFET incorporating advantages of both double and single gate structure along with another advantage of higher packing density compared to both the structure has been reported in [18]. For any MOS based device the most important parameter is the current through it. Therefore, model for current flowing through the JLFET is developed and presented here. In a JLFET, the variation of gate voltage causes variation of depletion width leading to variation in the channel resistance. When the gate voltage is below the threshold voltage, the channel is devoid of carriers resulting in a very high channel resistance [18-20]. Due to this ideally no current can flow through the device. At gate voltage exceeding the threshold value causes depletion width shrinking. As a consequence, channel resistance decreases which results in a decrease in the channel potential barrier to initiate the flow of current through the channel [20]. Further increase in the gate voltage reduces the depletion width until the condition of zero depletion width arises.

When the depletion width becomes zero the channel resistance drops to a very small value resulting in a large current. Drain current rise beyond the flat band value may also occur due to accumulation of charges near the oxide semiconductor boundary.

However, the current due to accumulated charges is negligible compared to the bulk current which dominates on-state characteristics of JLFET. Thus, the drain current in a JLFET is directly related to the channel resistance which varies with the depletion region thickness.

The model for a modified version of a JLFET with channel wrapped around the gate (SCJLFET) is presented. The model for all the modes of the device- sub threshold, bulk current, flat band and accumulation are obtained. The width of the depletion layer decides the mode of operation of the device. The model development starts with the determination of resistances of the three layers-depletion, neutral and accumulation which is followed by total resistance determination of the channel in the four modes. Finally, the current expression is obtained by dividing the channel potential difference with the total resistance. The model verification is done at simulation level with the help of results obtained from TCAD simulations.

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2. METHODOLOGY

The paper uses resistance of the channel to obtain the drain current. The method used to determine the resistance is based on the charge density in the various parts of the channel as the channel consists of neutral semiconductor, depletion or accumulation or their combinations in different modes of operation. The potential expression also obtained using Poisson's equation.

2.1 Model Derivation

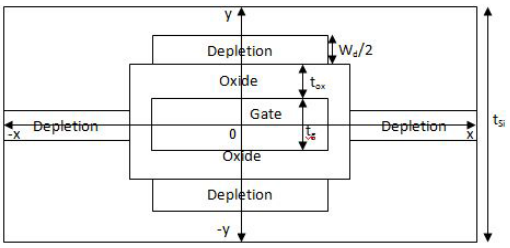

Fig. 1 – Surrounded channel of JLFET [18]

Fig. 1 indicates the schematic diagram. The body of the device is divided into three regions- drain, source and channel. The resistances of the regions are determined separately and finally equivalent resistance of the entire body has been determined. Each region consists of

i) Depletion resistance R_d (x, y, V_{gs}, V_{ds}) (Sub threshold) or
ii) Flat band resistance R_{nd} (x, y, V_{gs}, V_{ds}) (Flat band) or
iii) Combination of both neutral semiconductor region and depletion region (Bulk current) or
iv) A combination of neutral semiconductor and an accumulation resistance R_{acc} (x, y, V_{gs}, V_{ds}) (Accumulation)

The resistance equivalent circuit for the device for different modes of operation is shown in Fig. 2 (a), (b), (c) & (d).

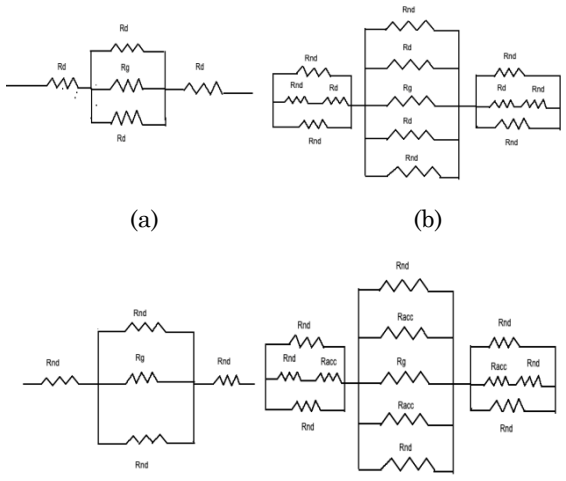

Fig. 2 – Sub threshold mode (a), bulk current mode (b), flat band mode (c), accumulation mode (d)

The current flowing through SCJLFET is,

$$I_D = \frac{\phi(L_D + \frac{L_G}{2}) - \phi(-L_S - \frac{L_G}{2})}{R_{eq}}$$

where $\phi(x = L_D + \frac{L_G}{2})$ and $\phi(x = -L_S - \frac{L_G}{2})$ are the potentials at the drain and source terminals which can be given as [18-20],

$$\Phi_0(x) = \left[\frac{V_{DS} + C\lambda^2 - \frac{C\lambda^2 e^{\frac{-(L_D+\frac{L_G}{2})}{\lambda}}}{e^{\frac{-(L_s-\frac{L_G}{2})}{\lambda}}}}{e^{\frac{(L_D+\frac{L_G}{2})}{\lambda}} - e^{\frac{-2(L_s-\frac{L_G}{2})}{\lambda}} e^{\frac{-(L_D+\frac{L_G}{2})}{\lambda}}} e^{\frac{x}{2}} \right] -$$

$$\left[\left\{ \frac{V_{DS} + C\lambda^2 - \frac{C\lambda^2 e^{\frac{-(L_D+\frac{L_G}{2})}{\lambda}}}{e^{\frac{-(L_s-\frac{L_G}{2})}{\lambda}}}}{e^{\frac{(L_D+\frac{L_G}{2})}{\lambda}} - e^{\frac{-2(L_s-\frac{L_G}{2})}{\lambda}} e^{\frac{-(L_D+\frac{L_G}{2})}{\lambda}}} \right\} \left\{ e^{\frac{-2(L_s-\frac{L_G}{2})}{\lambda}} - \frac{C\lambda^2}{e^{\frac{-(L_s-\frac{L_G}{2})}{\lambda}}} \right\} e^{\frac{-x}{\lambda}} \right] - C\lambda^2$$

and

$$R_{eq} = R_1 + \frac{R_2}{2} + R_3$$

In case of Sub threshold mode:

$$R_1 = \frac{R_{nd1}}{2} \| R_{d1}$$

$$R_2 = R_{d2}$$

$$R_3 = \frac{R_{nd3}}{2} \| R_{d3}$$

In case of Bulk current mode:

$$R_1 = \frac{R_{nd1}}{2} \| (R_{d1} + R_{nd4})$$

$$R_2 = R_{nd2} \| R_{d2}$$

$$R_3 = \frac{R_{nd3}}{2} \| (R_{d3} + R_{nd5})$$

In case of Flat band mode:

$$R_1 = R_{nd1}$$

$$R_2 = R_{nd2}$$

$$R_3 = R_{nd3}$$

In case of accumulation mode:

$$R_1 = \frac{R_{nd1}}{2} \| (R_{nd6} + R_{acc1})$$

$$R_2 = R_{nd2} \| R_{acc2}$$

$$R_3 = \frac{R_{nd3}}{2} \| (R_{nd7} + R_{acc3})$$

The channel potential equation for SCJLFET is given by [18-20],

$$j(x,y) = j_s = j_o(x) - \frac{\hat{I}_{ox}(\frac{t_{si}}{2}+t_{ox}+\frac{t_g}{2})^2}{2\hat{I}_{si}t_{ox}(t_{ox}+\frac{t_g}{2})}(j_{gs}-j_s) + \frac{\hat{I}_{ox}(t_{ox}+\frac{t_g}{2})}{2\hat{I}_{si}t_{ox}}(j_{gs}-j_s$$

Therefore the equation for the surface potential ϕ_s of SCJLFET is given by [18],

$$j_s = j_o(x) - \frac{\hat{I}_{ox}(\frac{t_{si}}{2}+t_{ox}+\frac{t_g}{2})^2}{2\hat{I}_{si}t_{ox}(t_{ox}+\frac{t_g}{2})}j_{gs} + \frac{\hat{I}_{ox}(\frac{t_{si}}{2}+t_{ox}+\frac{t_g}{2})^2}{2\hat{I}_{si}t_{ox}(t_{ox}+\frac{t_g}{2})}j_s + \frac{\hat{I}_{ox}(t_{ox}+\frac{t_g}{2})}{2\hat{I}_{si}t_{ox}}j_{gs} - \frac{\hat{I}_{ox}(t_{ox}+\frac{t_g}{2})}{2\hat{I}_{si}t_{ox}}j_s$$

3. RESULTS AND DISCUSSION

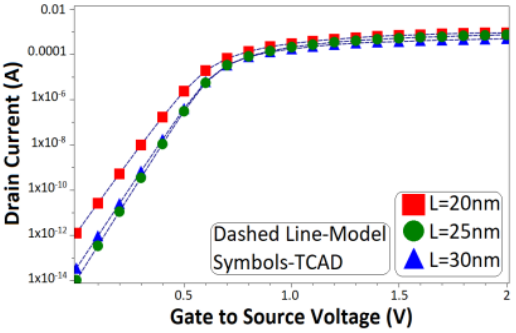

Fig. 3 – Transfer characteristics for various gate length

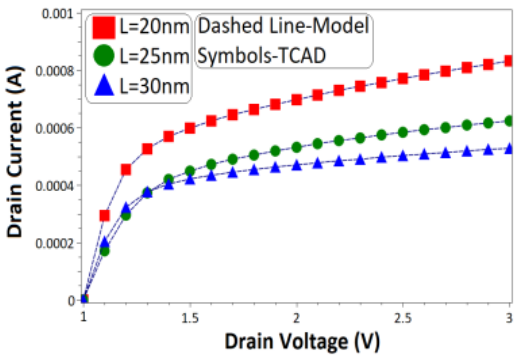

Fig. 4 – Output characteristics for various gate length

Fig. 3 shows transfer characteristics and Fig. 4 shows output characteristics for gate lengths (L = 20 nm, 25 nm, 30 nm). A device with very short gate lengths allows larger on current as well as sub threshold current due to lower channel resistances and higher DIBL.

Fig. 5 shows transfer characteristics and Fig. 6 indicates output characteristics for gate oxide thickness values (t_{ox} = 2 nm, 3 nm, 4 nm). Thicker gate dielectric layer generates higher capacitance between gate and the channel. This enhances the control of channel potential by the gate. This effect results in higher conduction current and lower sub threshold current due to enhanced coupling of gate and channel.

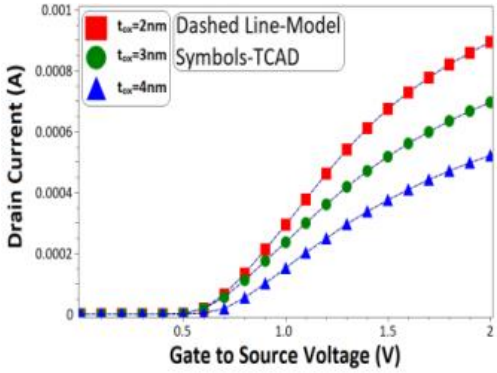

Fig. 5 – Transfer characteristics for various Gate dielectric thickness

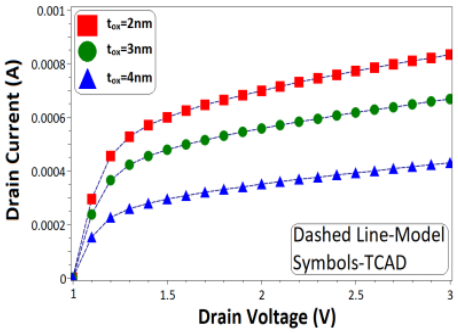

Fig. 6 – Output characteristics for different value of Gate oxide thickness

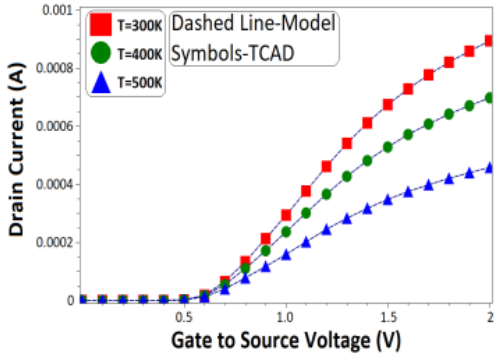

Fig. 7 – Transfer characteristics for different value of channel thickness

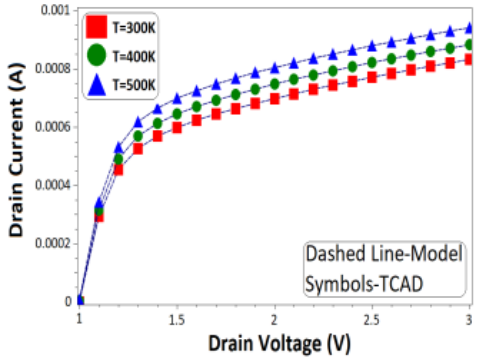

Fig. 8 – Output characteristics for different value of channel thickness

Fig. 7 shows transfer characteristics and Fig. 8 shows output characteristics for Temperatures (300 K, 400 K and 500 K). With rise in temperature the carrier mobility decreases which in turn causes lower drain current.

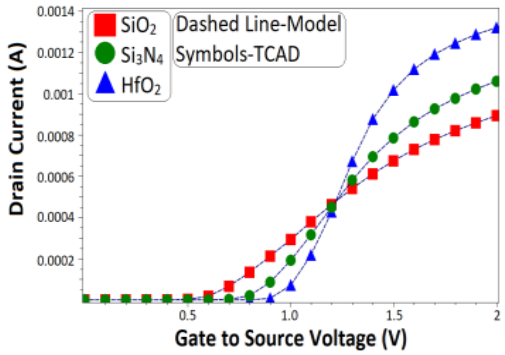

Fig. 9 – Transfer characteristics for different value of gate dielectric

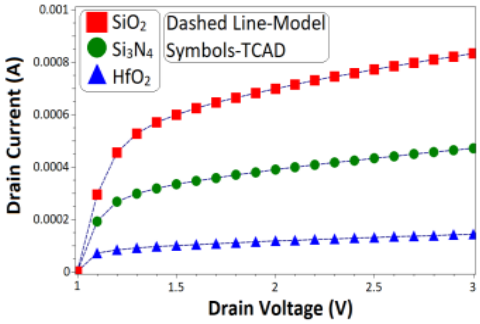

Fig. 10 – Output characteristics for different value of gate dielectric

Fig. 9 shows the transfer characteristics and Fig. 10 shows the output characteristics for different values of gate dielectric (e_{ox} = 3.9, 6.9, 22). Higher permittivity of gate dielectric also enhances the gate and channel coupling by capacitive effect resulting in reduced sub threshold and increased on current.

Table 1 – compares the I_{on}/I_{off} ratio, threshold voltage (V_{th}) and sub threshold swing (SS).

	Conventional JLFET	Surrounded Channel JLFET
I_{on}	1.7858	0.835
V_{th}	0.36	0.67
SS	75	60

4. CONCLUSION

The surrounded channel structure exhibits much better characteristics compared to other structure. The model developed is fully analytical in nature which reduces the computation time in designing. The model is full range model applicable in all the operation modes of SCJLFET. It is simplified model based on resistance of the body of the device. The validity of the model has been verified on a device simulation platform. The software used here is Cogenda Visual TCAD 1.8.0.

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Модель струму стоку на основі опору оточеного каналу польового транзистора

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У цій статті розглянута аналітична модель на основі опору для струму стоку польового транзистора з оточеним каналом (SCJLFET), який демонструє переваги транзисторів з подвійним та одинарним затворами. Ця стаття проілюструвала використання опору каналу для отримання струму стоку. Модель заснована на концепції, згідно з якою канал JLFET складається з шару просторового заряду, нейтрального шару, шару накопичення, або з комбінації будь-яких двох із цих шарів. Розробка моделі починається з формулювання опорів цих трьох типів шарів з подальшим визначенням загального опору каналу в чотирьох режимах роботи JLFET. У підпороговому режимі присутній лише виснажуючий шар, тоді як у режимі об'ємного струму загальний опір виходить шляхом паралельної комбінації опорів нейтрального напівпровідника. У режимі плоскої зони присутній лише нейтральний напівпровідниковий шар, тоді як у режимі накопичення загальний опір виходить шляхом паралельної комбінації опорів накопичення та виснаження. Модель струму стоку в чотирьох модах отримується діленням різниці потенціалів по каналу на відповідні опори мод. Це спрощена модель, яка має повністю аналітичний характер, що скорочує час обчислень при проектуванні. Вираз потенціалу також отриманий за допомогою рівняння Пуассона. Аналітична модель струму стоку була перевірена за допомогою результатів чисельного моделювання TCAD шляхом порівняння характеристик передачі та виходу пристрою, отриманих з TCAD, і моделі струму стоку.

Ключові слова: Модель струму стоку, Подвійний затвор, JLFET, Оточений канал, SCJLFET, TCAD.