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High Power Analysis of Surrounded Channel Junction Less Field Effect Transistor

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This paper reports the high power analysis of a new type of technology namely Surrounded channel junction less field effect transistor (SCJLFET) which can be used as power semiconductor switches in various power electronics circuits. Mainly surrounded channel junction less field effect transistor (SCJLFET) is a semiconductor device without junction where the gate is placed inside the body of the device or in other words the gate is surrounded by the channel region. Such type of surrounded channel junction less field effect transistor can be used as a power semiconductor switches in various power electronics circuit's applications. Surrounded channel junction less field effect transistor (SCJLFET) exhibits comparatively higher I_{on}/I_{off} ratio, lower sub threshold swing and higher threshold voltage with higher DIBL than a conventional JLFETwhich can be used easily in the numerous power electronics circuits. In this paper it is presented that a new device model as surrounded channel junction less field effect transistor (SCJLFET) has been introduced in the form of power MOSFET which can be used as power semiconductor switches in various power electronics devices in both off state and on state condition at high power, high voltage and high current. The surrounded channel JLFET show higher on current compared to conventional JLFET due to increased area of cross section. The on current and off current of the new structure have been determined for different values of drain voltages, gate oxide thickness, dielectric constant of gate dielectric, doping concentration and work function. The study of the characterization of SCJLFET at high power has been introduced in this paper. The high power characteristics of SCJLFET are compared with the other conventional junction less transistor using visual Cogenda TCAD 2D simulator.

Keywords: Junction less, Surrounded channel, High power, High voltage, High current, Off state, On state, TCAD.

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1. INTRODUCTION

Junction less Field effect Transistor (JLFET) has shown vast potential in the platform of VLSI due to its tremendous performance in very small dimensions[1-2]. The JLFET works on the principle of depletion width created by work function difference between the gate and body [1-20]. Although JLFET has many essential benefits it also suffers from some serious limitations. One major limitation of JLFET is the turn off condition. A JLFET requires a high work function gate and a thin channel to sufficiently suppress the off state current. It is almost impossible with a single gate JLFET structure to achieve proper off state as well saturation condition. Therefore the primary structure for JLFET is considered to be double gate structure. However the double gate structure also requires a thin channel for turning off the device. Moreover thin channel degrades carrier mobility resulting in degradation of on characteristics. It has been reported that few techniques are used for carrier mobility enhancement by placing two dielectrics diagonally and using gradual doping [18-20]. However, placing two dielectrics may have interfacing issues and using gradual doping at a very small dimension is challenging in terms of random dopant fluctuations. Therefore to overcome the previous issues a new structure is proposed to combine both the merits of single gate as well as double gate structure by placing the complete gate circuit inside the body as shown in fig1. The structure can be termed as surrounded channel as the gate is surrounded by the channel.

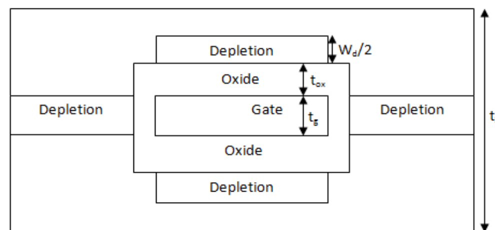

Fig. 1 – 2-D view of SCJLFET [20]

Such new model namely surrounded channel junction less field effect transistor (SCJLFET) is used as semiconductor switches in various power electronics

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circuit with high power in both off state and on state condition by applying different values of voltages and current. Capability of low power consumption becomes increasingly essential criterion for various power electronics circuits' technology. It is also necessary to decrease the size and bulkiness of various power circuits in the sense of increasing by introducing new technology changes. Power electronics is the method that controls the flow of current as well as voltage converting it to a form that is essential and suitable for output. The most reliable and desirable power electronics system is one whose efficiency is about 100 percent. The essential use of semiconductor switching devices in power electronics system is mainly based on their ability to manipulate and control very huge amounts of power from the input to the load with relatively very low power dissipation in the semiconductor switching device which results in a very high efficiency power electronics circuit and system. The power MOSFET is one of the most reliable and common power device due to fast switching speed, low power by gate drive and advanced capability of paralleling. Power semiconductor devices such as power MOSFET are found in systems which delivered as little as a few tens of milliwatts up to around a gigawatt in a high voltage direct current transmission results in high power ratings. It also enhances and control the flow of current and voltage drop across the load. Power MOSFET a type of MOSFET which is normally meant to handle high levels of power ratings. These exhibit and provide high speed and can also work much better in comparison with other normal MOSFETs in the case of low voltage and current levels. Power MOSFETs can sustain high voltage and high blocking current, making them reliable and suitable for low power switching applications. Due to the presence of P-N junctions the short channel effects devastates the performance of any device which are involved. It is necessary to reduce short channel effects along with channel reduction of the device. It is a huge challenge for fabrication world to fabricate such conventional MOSFET's at smaller scalability with very accurate and fine alignment of junctions. Therefore a new design has been introduced to reduce such complexity in which MOS transistor are made without junctions that results in the reduction of short channel effects and it is known as junction less technology. These types of power junction less MOSFET are used as semiconductor switchesin various power electronics circuits.

In this paper it is presented that a new device model as surrounded channel junction less field effect transistor (SCJLFET) has been introduced in the form of power MOSFET which can be used as semiconductor power switches in various power electronics devices in both off state and on state condition at high power, high voltage and high current. A study about characterization and analysis of high power of surrounded channel junction less field effect transistor (SCJLFET) as semiconductor power switches for both off state and on state condition is done using Visual Cogenda TCAD 2D simulator.

2. RESULT AND DISCUSSION

The surrounded channel JLFET has been simulated on TCAD 2D device simulator. The on current and off current of the structure have been determined for different values of drain voltages, gate oxide thickness, dielectric constant of gate dielectric, doping concentration and work function.

Table 1 – *On* current and *Off* current variation with drain voltage

Drain Voltage (V)	I_{ON} (A)			I_{OFF} (A)		
	SCJLFET	Conventional JLFET	DGMOSFET	SCJLFET	Conventional JLFET	DGMOSFET
5	11.1972	1.61	0.0012	0.8646×10^{-7}	0.775×10^{-6}	0.79×10^{-6}
10	11.6629	1.94	0.0046	0.9063×10^{-7}	0.785×10^{-6}	3.15×10^{-6}
15	11.8359	2.23	0.011	0.9304×10^{-7}	0.794×10^{-6}	7.1×10^{-6}
20	11.9686	2.45	0.019	0.9492×10^{-7}	0.801×10^{-6}	1.3×10^{-5}
25	12.0851	2.79	0.029	0.9652×10^{-7}	0.808×10^{-6}	2×10^{-5}
30	12.1959	3.08	0.042	0.9801×10^{-7}	0.814×10^{-6}	3×10^{-5}
35	12.3036	3.42	0.057	0.9942×10^{-7}	0.820×10^{-6}	3.9×10^{-5}
40	12.4092	3.84	0.075	1.0077×10^{-7}	0.826×10^{-6}	5×10^{-5}
45	12.5134	4.11	0.095	1.0208×10^{-7}	0.831×10^{-6}	6.4×10^{-5}
50	12.6163	4.35	0.117	1.0335×10^{-7}	0.835×10^{-6}	7.9×10^{-5}

Table 2 – *On* current and *Off* current variation with gate oxide thickness

Tox (nm)	I_{ON} (A)		I_{OFF} (A)	
	SCJLFET	Conventional JLFET	SCJLFET	Conventional JLFET
10	12.6163	4.35	1.0335×10^{-7}	0.835×10^{-6}
12	12.5723	3.91	1.1125×10^{-7}	3.28×10^{-6}
14	12.5291	3.31	1.2423×10^{-7}	8.23×10^{-6}
16	12.4678	2.47	1.3692×10^{-7}	1.483×10^{-7}
18	12.4153	1.58	1.4862×10^{-7}	2.224×10^{-7}
20	12.3542	0.66	1.6142×10^{-7}	3.123×10^{-7}

The on current as well as off current rises with drain voltage due to increased longitudinal field and drain induced barrier lowering (DIBL) as shown in the Table 1. With lower gate oxide thickness and higher gate dielectric constant the capacitive coupling of gate with channel rises. It results in higher on current and lower off current indicating enhanced control of gate over the channel as shown in the Table 2 and Table 3. The higher work function of gate results in stronger internal electric field creating depletion region in the channel. The applied gate electric field has to overcome the internal electric field to initiate current conduction. Therefore the on current and off current are lower for higher work function of gate as shown in the Table 4. Higher doping concentration implies higher carrier density. Therefore both on and off current are higher for higher doping concentration as shown in the Table 5.

It can be seen from the tables that the surrounded channel JLFET show higher on current compared to conventional JLFET due to increased area of cross-section. The SCJLFET structure shows almost equal off current to conventional DGJLFET as effective electric field creating the depletion is same for both cases.

Table 3 – *On* current and *Off* current variation with dielectric constant of gate dielectric

ϵ_{ox}	I_{ON} (A)		I_{OFF} (A)	
	SCJLFET	Conventional JLFET	SCJLFET	Conventional JLFET
3.9	12.6163	4.35	1.0335×10^{-7}	0.835×10^{-6}
6.9	12.7842	7.7	0.9892×10^{-7}	0.58×10^{-6}
22	14.2314	11.2	0.7345×10^{-7}	0.32×10^{-6}

Table 4 – *On* current and *Off* current variation with work function.

Work function (eV)	I_{ON} (A)		I_{OFF} (A)	
	SCJLFET	Conventional JLFET	SCJLFET	Conventional JLFET
5.2	12.6912	5.71	1.0971×10^{-7}	1.822×10^{-6}
5.3	12.6431	4.92	1.0632×10^{-7}	0.961×10^{-6}
5.4	12.6163	4.35	1.0335×10^{-7}	0.835×10^{-6}
5.5	12.5964	3.98	1.0311×10^{-7}	0.715×10^{-6}
5.6	12.5728	3.43	1.0287×10^{-7}	0.596×10^{-6}

Table 5 – *On* current and *Off* current variation with doping concentration.

Doping Concentration (/cm^3)	I_{ON}(A)		I_{OFF}(A)	
	SCJLFET	Conventional JLFET	SCJLFET	Conventional JLFET
10^{18}	12.4218	2.98	1.0164×10^{-7}	0.45×10^{-6}
2×10^{18}	12.4631	3.21	1.0178×10^{-7}	0.51×10^{-6}
4×10^{18}	12.5013	3.39	1.0196×10^{-7}	0.59×10^{-6}
6×10^{18}	12.5472	4.5	1.0212×10^{-7}	0.66×10^{-6}
8×10^{18}	12.5841	4.39	1.0248×10^{-7}	0.77×10^{-6}
10^{19}	12.6163	4.35	1.0335×10^{-7}	0.835×10^{-6}

This paper shows the work is innovative comparing the existing works as that the new device model as surrounded channel junction less field effect transistor (SCJLFET) has been introduced in the form of power MOSFET which can be used as semiconductor power switches in various power electronics devices in both the condition of off state and on state at high power, high voltage and high current. The surrounded channel JLFET show higher on current compared to conventional JLFET due to increased area of cross-section. The SCJLFET structure shows almost equal off current to conventional DGJLFET as effective electric field creating the depletion is same for both cases.

3. CONCLUSION

A study on the characteristics of a SCJLFET at high power has been performed and presented in this paper. The on and off current of the device have been compared with that of conventional JLFET at high power. The study showed that the SCJLFET exhibits higher on current and lower off current compared to that of conventional JLFET. Therefore the SCJLFET is suitable for high power applications with thinner channel and thinner gate oxide and with high K gate dielectric.

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Аналіз високої потужності транзистора без польового ефекту з оточеними каналами

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У статті проведений аналіз високої потужності нового типу технології, а саме транзистора без польового ефекту з оточеним канальним переходом (SCJLFET), який можна використовувати як силові напівпровідникові перемикачі в різних схемах силової електроніки. Транзистор без польового ефекту з переважно оточеним канальним переходом (SCJLFET) – це напівпровідниковий пристрій без переходу, де затвор розміщено всередині корпусу пристрою, іншими словами, затвор оточений областю каналу. Такий тип безпольового транзистора з оточеним канальним з'єднанням можна використовувати як силові напівпровідникові перемикачі в різних схемах силової електроніки. Транзистор без польового ефекту з оточеним канальним з'єднанням (SCJLFET) демонструє порівняно вищий коефіцієнт I_{on}/I_{off}, нижчий підпороговий коливання та вищу порогову напругу з вищим DIBL, ніж звичайний JLFET, який можна легко використовувати в численних схемах силової електроніки. У цій статті представлено нову модель пристрою, як транзистор без польового ефекту з оточеним канальним переходом (SCJLFET) у формі силового MOSFET, який можна використовувати як силові напівпровідникові перемикачі в різних пристроях силової електроніки як у вимкненому, так і у включеному стані. стан стану при високій потужності, високій напрузі та великому струмі. JLFET з оточеним каналом показує більший струм порівняно зі звичайним JLFET завдяки збільшеній площі поперечного перерізу. Струм увімкнення та вимкнення нової структури були визначені для різних значень напруги стоку, товщини оксиду затвора, діелектричної проникності діелектрика затвора, концентрації легування та роботи виходу. Дослідження характеристик SCJLFET при високій потужності було представлено в цій статті. Характеристики високої потужності SCJLFET порівнюються з іншими звичайними транзисторами без переходів за допомогою візуального симулятора Cogenda TCAD 2D.

Ключові слова: Оточений канал, Висока потужність, Висока напруга, Високий струм, Вимкнений стан, Увімкнений стан, TCAD.