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REGULAR ARTICLE

Design and Analysis of Charge Plasma-Based Heterogeneous *L*-Shaped Tunnel Field-Effect Transistor (TFET) for Low-Power Applications

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In this proposed work focuses to overcome the traditional doping challenges in *L*-shaped tunnel field transistors by using charge plasma (CP) concept and increase current conduction by forming heterogeneous junction (SiC-Si-SiC). Silicon carbide is used for the material for Source and Drain. The concept of charge plasma is implemented in the source and drain regions by implementing different work functions and to improve current conduction the source and drain regions is made of Silicon Carbide and the channel is made of Silicon which forms heterojunction which creates horizontal tensile strain and vertical compressive strain in the channel region which increases electron mobility mainly for low-power semiconductor applications. The performance of device parameters like the transfer characteristics subthreshold swing, output characteristics have been described. Analysis of Threshold Voltage, drain current and I_{ON}/I_{OFF} ratio have been carried for CP based *L*-TFET. Sentaurus Technology Computer Aided Design (TCAD) has been used to evaluate and analyze the device for the CP-based TFET. The device was simulated in the Sentaurus TCAD in which the certain parameters are evaluated in which certain models such as, Slotboom model is applied to consider the impact of doping concentrations on energy bandgap narrowing in the source/drain (S/D) regions. Also, Fermi statistics and Shockley-Read-Hall recombination models are used. The inclusion of charge plasma and SiC in the device improves the electron mobility and current conduction is improved with less leakage current and can be used for low power applications such as inverter, memory devices.

Keywords: Band to band tunneling, *L*-shaped TFET, Charge plasma, Work function, Silicon carbide (SiC).

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1. INTRODUCTION

The growing demand for increased performance and miniaturization in electronic devices has significantly reduced the use of conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). [1]. While MOSFETs remain essential for certain applications, their inherent limitations particularly a subthreshold swing (SS) greater than 60 mV/dec and a high ON-OFF current ratio (Ion) present significant challenges for low-power operation. To address these issues, researchers have explored various MOS devices, including nanoelectromechanical FETs and Tunnel FETs. Among these, Tunnel FETs show promise as candidates for low-power applications. [2]. Tunnel FETs operate based on electron band-to-band tunneling, allowing them to act as switches at lower voltages compared to MOSFETs. These devices offer reduced subthreshold swing, extremely low off-state current (I_{OFF}), and improved performance for low-power digital and memory applications. With their unique characteristics, Tunnel FETs can meet the requirements of efficient, low-power electronic circuits [3]. Device reduction to a few nanometer scale divisions, where traditional chemical doping techniques are used to dope semiconductor materials, has been a major advance for many edge-cutting devices. When the device size reduces to a few nanometers, the conventional doping procedures become less effective and more challenging [4].

This research work incorporates by implementing work function induced doping, charge plasma method. This method is an effective technique for introducing charge carriers of *n*-type and p-type into the intrinsic semiconductors. This method is effectively applied on the intricate devices such as Bipolar Junction Transistors, Junction less transistors and Tunnel Field Effect Transistors. [5, 6]. The use of homogeneous material (Si) results in a homojunction, where current conduction is reduced. To enhance current conduction, heterogenous material (SiC) is employed, forming a hetero-junction. SiC has been experimentally proven and introduced as a source and drain material. Incorporating SiC introduces both horizontal and vertical strain in the channel region. This strain alters the physical properties of the channel, particularly the electron mobility, leading to improved device performance. [7].

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The next phase of the paper has been split into subsequent sections: The proposed structure is explored in section 2 and analysis of outcomes are dealt with in section Three.

2. DEVICE STRUCTURE

Fig. 1 illustrates the schematic view of the existing L-shaped TFET, which was created in the TCAD simulation tool using the parameters mentioned in [2]. In this present work, as referenced in [2], the switching characteristics are discussed along with doping engineering, which also includes the process integration for the given fabrication.

In Fig. 2 the schematic diagram of the proposed work is depicted in which two different work function metal are introduced above the source and drain regions. The parameters of the proposed device are: 20 nm gate length, 1 nm oxide thickness,4nm channel thickness, 80 nm source height, 30 nm source length, 30 nm drain length, 10 nm body thickness, 24 nm pocket length, 1×10^{15} cm^{-3} source doping, 1×10^{20} cm^{-3} drain doping, 2.5×10^{19} cm^{-3} pocket doping and 5×10^{17} cm^{-3} body doping.

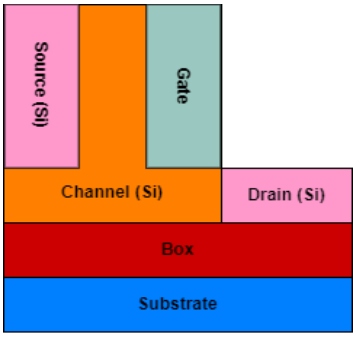

Fig. 1 – Schematic view of existing L-shaped TFET

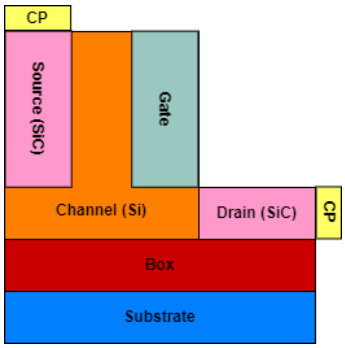

Fig. 2 – Schematic view of the proposed work

The p^+ channel area in the proposed structure is made utilizing the Charge Plasma (CP) method. In order to use this method into effect, two conditions must be fulfilled [8]:

(i) Given the inequality, the metallic contact work function in the channel should be higher than that of silicon.

$$\phi_m > \chi_{Si} + (E_G/2q) \quad (1)$$

Where q represents the charge of an electron, E_G is the bandgap of silicon, and χ_{Si} is the Electron Affinity of Silicon.

(ii) The channel thickness must also be shorter than the Debye length, which is defined as

$$L_D = (\varepsilon_{Si} V_T/q.N) \quad (2)$$

Where ε_{Si} is the silicon's dielectric constant, V_T is the thermal voltage, and N is the carrier concentration.

The proposed structure intends to improve device performance by generating carriers in the channel region without conventional doping by meeting these requirements mentioned above. The metal contact given in the channel is made of several materials, including Cobalt, Gold, Palladium, and Platinum, with corresponding work functions of 5 eV, 5.1 eV, 5.12 eV, and 5.65 eV, respectively, to satisfy the first condition, in which the contact should be above the silicon.

The proposed device shown in fig depicts the source terminal, channel and drain terminal in which the metal later is placed above the source and drain regions in which the carriers are introduced in the channel region without conventional doping in which there is a precise control over the doping concentration to achieve the electrical properties with a high efficiency. Additionally, Hetero-junction (SiC is used as a Source/Drain Material) has been formed by replacing with the Homo-junction structure (Si is used as a Source/Drain Material).

The device was simulated in the Sentaurus TCAD in which the certain parameters are evaluated in which certain models such as, Slotboom model is applied to consider the impact of doping concentrations on energy bandgap narrowing in the source/drain (S/D) regions. Also, Fermi statistics and Shockley-Read-Hall recombination models are used [2].

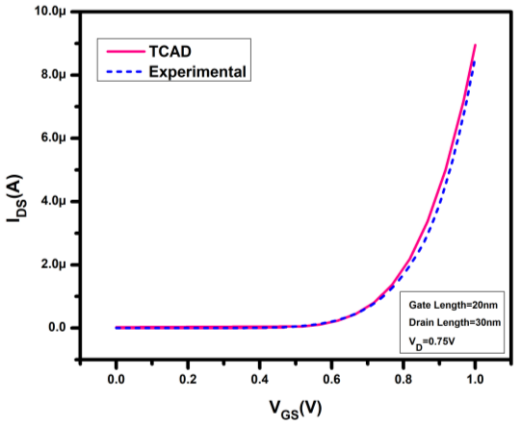

Fig. 3 – Simulation result validates with [4]

3. RESULT AND DISCUSSION

3.1 Hetero Junction

Hetero junction has been created by changing Si to SiC in source and drain of the L-TFET. The hetero-junction is given in Fig. 4. The bandgap of Si is 1.1 eV and SiC is 3.26 eV. As per the hetero-junction theory, the conduction

band of the source region is always higher than that of the channel region, and the band-offset ΔEC created from the hetero-junction increases the velocity of electrons from the source. The current drive has been increased based on that functionality. The source and drain (SiC) regions act as stressors to generate lateral tension and vertical compression in the channel, thereby increasing the mobility of elec-trons which increases output current drive.

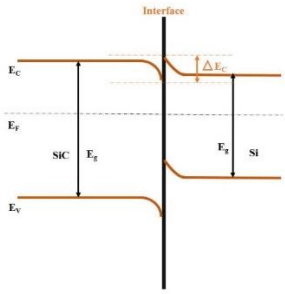

Fig. 4 – Hetero Junction Formation

3.2 IV Characteristics

The transfer characteristics for homo-junction device has been analyzed by keeping the V_D constant at 1 V and varying V_G from 0 to 1.2 V, and then varying the gate bias from 0 to 1 V by placing V_D constant at 50 mV. For the hetero-junction device, similar analysis is carried out as the homo-junction device, but the gate bias is varied from 0 to 1.5 V for V_D constant of 1 V. Moreover, hetero-junction has an added advantage of higher I_{on}/I_{off} ratio and output current than the homo-junction device due to increased carrier velocity. When $V_D = 50$ mV, both devices produce almost the same current, but in the case of $V_D = 1$ V, the L-TFET hetero-junction has 42% more drain current than L-TFET homo-junction, which produces a 75% drain current. Due to the increased velocity of carriers in the source–channel junction,

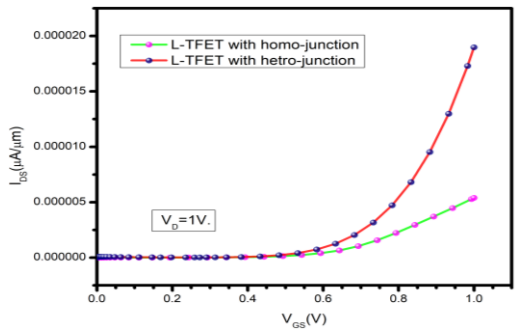

Fig. 5 – Comparison between Transfer Characteristics of both Homo-junction (Si) and Hetero-junction (SiC) in L- TFET

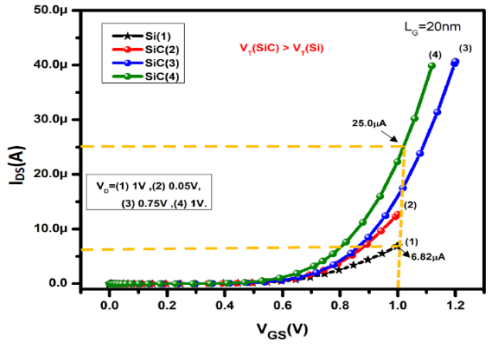

Fig. 6 – Comparison between Transfer Characteristics of both Homo-junction (Si) and Hetero-junction (SiC) in L- TFET for different values of V_d

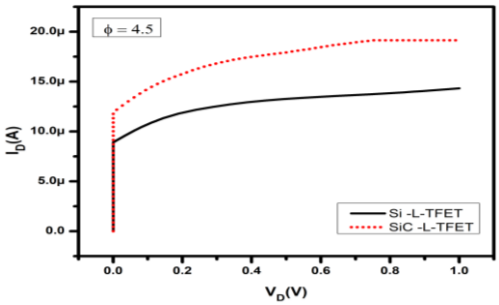

Fig. 7 – Comparison between Output Characteristics of both Homo-junction (Si) and Hetero-junction (SiC) in L-TFET when $V_g = 1$ V

conductance has been increased rap-idly even for small change in gate voltage. The hetero-junction feature will be more suitable for sub 5 nm devices since there is an acceleration of carriers for minimum change in voltage. The presence of hetero-junction helps the proposed structure to attain better I_{on}/I_{off} ratio compared to other works. The I_{on}/I_{off} value reached an approximate value of $10^6 – 10^7$. The Ideal value of SS is 60 mV/decade. The performance of the device is increased by using the UTB, charge plasma based doping, and the heterojunction.

4. CONCLUSION

Without changing the device structure, by using only materials strain has been created and carrier velocity has been increased Strain is created in the device using only the materials. The carrier velocity of the device has been increased, resulting in an enhanced device performance when compared with the conventional device [1]. The concept of Hetero-structure and charge plasma doping is implemented on source and drain region without conventional doping hence improves the performance. Almost 12 times better cur-rent drive than the conventional JL nanowire is produced under different strain levels.

REFERENCES

1. R. Dhanush, R.A. Kumar, S. Logisvary, *J. Nano- Electron. Phys.* 14 No 5, 05015 (2022).
2. H.W. Kim, D. Kwon, *IEEE J. Electron Dev. Soc.* **9**, 359 (2021).
3. G. Gupta, B. Rajasekharan, R.J. Hueting, *IEEE Trans. Electron Dev.* **64** No 8, 3044 (2017).
4. R.J. Hueting, B. Rajasekharan, C. Salm, J. Schmitz, *IEEE Electron Dev. Lett.* **29** No 12, 1367 (2008).
5. P.N. Chander, P. Raja, S.A. Kumar, R. Gayathri, *IETE Journal of Research* **70**, 6950 (2024).
6. S.A. Kumar, J.C. Pravin, *J. Nano- Electron. Phys.* **13** No 1, 01005 (2021).
7. Z. Yang, *IEEE Electron Dev. Lett.* **37** No 7, 839 (2016).
8. C. Sahu, J. Singh, *IEEE Electron Dev. Lett.* **35** No 3, 411 (2014).
9. S.S. Shin, J.H. Kim, S. Kim, *Jpn. Soc. Appl. Phys.* **58**, SDDE10 (2019).
10. K.M. Choi, W.Y. Choi, *IEEE Electron Dev. Lett.* **34** No 8, 942 (2013).
11. W.Y. Choi, W. Lee, *IEEE Trans. Electron Dev.* **57** No 9, 2317 (2010).
12. W.V. Devi, B. Bhowmick, P.D. Pukhrambam, *IEEE Trans. Electron Dev.* **67** No 5, 2133 (2020).
13. http://www.sentaurus.dsod.pl/manuals/data/sdevice_ug.pdf.

Розробка та аналіз гетерогенного *L*-подібного тунельного польового транзистора (TFET) на основі зарядової плазми для застосувань з низьким енергоспоживанням

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У цій пропонованій роботі фокусується на подоланні традиційних проблем легування в *L*-подібних тунельних польових транзисторах за допомогою концепції зарядової плазми (CP) і збільшення провідності струму шляхом формування гетерогенного переходу (SiC-Si-SiC). Карбід кремнію використовується як матеріал для джерела та витоку. Концепція зарядової плазми реалізована в областях витоку та стоку шляхом реалізації різних робочих функцій, а для покращення провідності струму області витоку та стоку виготовлені з карбіду кремнію, а канал виготовлений із кремнію, який утворює гетероперехід, який створює горизонтальну деформацію розтягування та вертикальну деформація стиснення в області каналу, що збільшує рухливість електронів, головним чином для малопотужних напівпровідникових застосувань. Описано продуктивність таких параметрів пристрою, як підпорогове коливання характеристик передачі, вихідні характеристики. Аналіз порогової напруги, струму витоку та співвідношення I_{ON}/I_{OFF} було проведено для *L*-TFET на основі CP. Технологія Sentaurus Computer Aided Design (TCAD) була використана для оцінки та аналізу пристрою для TFET на основі CP. Пристрій було змодельовано в Sentaurus TCAD, у якому оцінюються певні параметри, у яких певні моделі, такі як модель Slotboom, застосовуються для розгляду впливу концентрації допінгу на звуження забороненої зони енергії в областях джерела/витоку (S/D). Також використовуються статистика Фермі та рекомбінаційні моделі Шоклі-Ріда-Холла. Включення зарядової плазми та SiC у пристрій покращує рухливість електронів, а провідність струму покращується з меншим струмом витоку, і його можна використовувати для додатків з низьким енергоспоживанням, таких як інвертори, пристрої пам'яті.

Ключові слова: Смугове тунелювання, L-подібний TFET, Зарядна плазма, Функція виходу, Карбід кремнію (SiC).