




REGULAR ARTICLE

Performance Analysis of Vertical Gate-All-Around Multi-Bridge Channel Field Effect Transistor for Low-Power Applications

S.B. Lenin¹, S.A. Kumar^{2,*} , T. Sibbi¹, T. Kumaran¹, R. Pravin¹

¹ Department of ECE, Sri Manakula Vinayagar Engineering College, Madagadipet Puducherry, India

² Department of ECE, Karpagam Academy of Higher Education, India

(Received 03 July 2024; revised manuscript received 25 October 2024; published online 30 October 2024)

The study focuses on the Vertical Gate-All-Around Multi-Bridge-Channel Field-Effect Transistor (VGAA-MBCFET), which is a critical component in developing low-power applications. Several optimization strategies are being investigated to improve VGAA-MBCFET performance, with a particular focus on improving the on-off ratio, reducing leakage current, and fine-tuning I-V characteristics. The study emphasizes the distinctive vertical gate-all-around structure and scalability benefits that distinguish VGAA-MBCFETs from horizontal counterparts such as FinFETs and lateral GAAFETs. In-depth research on the scalability of VGAA-MBCFETs into smaller technological nodes is a significant priority, since it is recognized as crucial to influencing the future of sophisticated and compact integrated circuits. The paper acknowledges these innovations revolutionary impact on large-scale integration (LSI) improvements, as well as their influence on the trajectory of wearable technology within the larger context of integrated circuit miniaturization the issues provided by downsizing are openly discussed, with recognition of their complicated impact on wearable performance and functionality. As wearable technology aims to incorporate high-performance computing systems, this study addresses the constraints of traditional techniques and investigates whether VGAA-MBCFETs can be a transformative technology, allowing for compact yet powerful designs in energy-efficient electronic gadgets. The study uses robust modelling approaches to provide thorough insights into the capabilities and possible applications of VGAA-MBCFETs, providing a significant contribution to the ongoing progress of low-power electronic device technology.

Keywords: Large-scale integration (LSI), On-off ratio, Scalability, Vertical gate-all-around structure.

DOI: [10.21272/jnep.16\(5\).05028](https://doi.org/10.21272/jnep.16(5).05028)

PACS numbers: 85.30.De, 85.30.Tv, 73.40.Qv

1. INTRODUCTION

A major advancement in semiconductor research and device engineering has been made with the study of the Vertical Gate-All-Around Multi-Bridge-Channel Field-Effect Transistor (VGAA-MBCFET) for low-power applications. The goal of this state-of-the-art study is to gain a thorough understanding of the scalability, performance, and potential benefits of VGAA-MBCFETs in the context of electronic systems that use less energy. Because of their distinctive Multi-Bridge-channel architecture and vertical gate-all-around structure, VGAA-MBCFETs are seen as promising options for low-power applications [1]. This study's main goal is to thoroughly analyze and simulate these transistors in order to investigate their dependability, speed, power consumption, and efficiency in a range of operating scenarios [1].

To investigate important factors like I-V characteristics, leakage current reduction, and on-off ratio improvement, the study utilizes simulation techniques. VGAA-MBCFETs are a development from earlier generations of transistor designs in the history of

transistor technology [3]. FinFETs and lateral GAAFETs, two earlier iterations, have played a significant role in advancing semiconductor technology. FinFETs, for example, improved current flow control by introducing a three-dimensional fin-like structure. Even though these technologies have made a substantial contribution to the development of integrated circuits, VGAA-MBCFETs go one step further by utilizing a multi-bridge-channel design and a vertical orientation [2].

Especially when low-power applications are pursued [2]. FinFETs and lateral GAAFETs are two well-known transistor designs that had a big impact on semiconductor technology prior to the development of VGAA-MBCFETs. FinFETs solved issues with current flow control with their novel three-dimensional fin-like structure. This design offered better electrostatic control and lower leakage currents, marking a significant departure from conventional planar transistor architectures [5].

A significant step toward the creation of more potent and efficient integrated circuits was made with the introduction of FinFETs [7]. In a parallel development, the

* Correspondence e-mail: 6691ashok@gmail.com



implementation of gate-all-around structures by lateral GAAFETs furthered semiconductor technology, providing enhanced control over the channel to mitigate the negative effects of short-channel phenomena. While lateral GAAFETs represented a substantial advancement, the pursuit of more sophisticated transistor architectures persisted among engineers and researchers to meet the evolving demands of low-power applications [4].

Enter VGAA-MBCFETs, a state-of-the-art concept in transistor design. VGAA-MBCFETs stand out due to their vertical gate-all-around structure and unique Multi-Bridge-channel architecture, offering exclusive advantages that make them particularly promising for low-power applications. The innovation brought by VGAA-MBCFETs enables improved performance and scalability, addressing crucial issues in modern electronic systems [8].

The primary objective of the state-of-the-art study on VGAA-MBCFETs is the comprehensive analysis and simulation of their behavior in various operating scenarios. Parameters such as I-V characteristics, leakage current reduction, and on-off ratio improvement play a pivotal role in evaluating the dependability, speed, power consumption, and overall efficiency of VGAA-MBCFETs [7]. In this investigation, the utilization of analytical tools and simulation techniques is essential, providing crucial insights into the performance of these advanced transistor structures [8].

2. DEVICE STRUCTURE

The Vertical Gate-All-Around Field-Effect Transistor (VGAA-FET) is an advancement in semiconductor technology, with a sophisticated and distinct device structure targeted at improving overall performance. The semiconductor substrate, which is commonly made of silicon, provides the foundational support for the VGAA-FET. The device's effectiveness is high-lighted by vertically oriented nanowires that have been precisely constructed as active channels to permit efficient charge carrier transport [11].

The VGAA-FET is distinguished by its Gate-All-around (GAA) arrangement, in which the gate material surrounds the whole circumference of each nanowire [8]. This vertical GAA architecture gives the transistor extraordinary control over the channel, reducing leakage currents and improving overall performance. To ensure precision and prevent unwanted interactions, carefully placed dielectric materials operate as insulators, producing a clear separation between the nanowires and the gate material [10]. The source and drain areas at the nanowire terminations are critical to the VGAA-FET's operation. These regions serve an important role in orchestrating the flow of current, which is regulated by the electric field produced by the encompassing gate, resulting in controlled and efficient operation. Spacer materials can be carefully used to optimize nanowire spacing, ensuring.

Consistency and exact control over the transistor's electrical properties. Metal contacts and interconnects

complete the extensive network, allowing for seamless connections between the source, drain, and external circuitry. The gate dielectric layer plays an important function in maintaining the necessary separation between the gate and the channel, hence contributing to successful modulation of the transistor's operation [12].

The VGAA-FET structure's purposeful vertical orientation highlights its small footprint and excellent space utilization, making it especially desirable for applications that require size reduction [9]. The VGAA-FET's careful device structure combines sophisticated design approaches to address difficulties inherent in classic transistor layouts, providing greater control, decreased leakage, and potential scalability benefits within the area of semiconductor applications [11].

Field-effect transistors (FETs) with multi-bridge devices and structures represent a paradigm change in semiconductor design by offering creative ways to improve transistor performance. These multi-bridge structures, like dual-gate and triple-gate FETs, were developed in response to the shortcomings of conventional single-channel designs [10]. They distribute current across several bridges to provide increased flexibility and control. This development improves reliability and scalability by reducing short-channel effects, a recurring problem in conventional FETs. This idea is notably expanded upon by Vertical Gate-All-Around Multibrige-Channel FETs (VGAA-MBCFETs), which combine multiple bridge-like structures and a vertical orientation. The primary goals of this design are to maximize current flow, minimize power consumption, and improve efficiency all of which are important considerations for low-power applications [10].

Although multi-bridge structures present a promising avenue for advancement, there are obstacles to their adoption. One of the challenges that researchers are actively tackling is the complexity of fabrication processes and the possible financial ramifications. Furthermore, compatibility and system-level implications must be carefully considered when integrating these structures into current semiconductor technologies. Continuous research endeavors to enhance manufacturing methodologies to optimize fabrication and investigate strategies for seamless integration. Multi-Bridge FETs are at the forefront of innovation in the semiconductor industry, with the potential to redefine transistor technology and open the door to more effective, scalable, and adaptable electronic systems [12].

2.1 Gate-All-Around Field-Effect Transistor

The Gate-All-Around Field-Effect Transistor (GAAFET) is a semiconductor device with a three-dimensional gate structure surrounding the channel. This design provides better control over the flow of current compared to traditional transistors. By enveloping the channel with the gate, the GAAFET reduces gate-to-channel capacitance and improves gate control, resulting in improved performance and reduced

leakage currents, especially in low-power applications [15]. One of its significant advantages is scalability to smaller technology nodes. Traditional transistors face challenges like gate leakage and variability as they shrink in size. However, the GAAFET's gate-all-around configuration mitigates these issues by maintaining strong gate control even at nanoscale dimensions, enabling the development of smaller and more efficient devices for advanced integrated circuits [18].

The improved gate control of the GAAFET is one of its main advantages. Modulating the channel conductivity more effectively is made possible by the gate-all-around arrangement, which reduces the gate-to-channel capacitance. Better subthreshold swing and lower leakage currents are the outcomes of this, especially under off-state circumstances. Furthermore, the gate-all-around design of the GAAFET reduces the impact of short channels [14], allowing for improved performance at lower device dimensions.

Another significant advantage of the GAAFET is its scalability. Traditional planar transistors face difficulties such as rising gate leakage and unpredictability as semiconductor research continues to push towards lower feature sizes [16]. On the other hand, even at nanoscale dimensions, robust gate control is preserved thanks to the GAAFET's gate-all-around design. This scalability permits the construction of more compact and power-efficient integrated circuits by guaranteeing that GAAFET-based devices can maintain performance requirements as technology nodes shrink [17].

2.2 Multi Bridge Channel Field-Effect Transistor (MBCFET)

A unique transistor construction with numerous bridge-like channels inside the device is presented by the Multi Bridge Channel Field-Effect Transistor (MBCFET). This arrangement improves the speed and power handling of the transistor by increasing its ability to conduct current efficiently [19]. When compared to conventional transistors with single-channel designs, the MBCFET's architecture facilitates more efficient charge transport, allowing for better conductivity. Applications needing strong power handling capabilities and high-speed operation will find this capability especially helpful [14].

Furthermore, the multi-bridge channel design of the MBCFET overcomes scalability issues with conventional transistor architectures. Through the use of smaller bridge structures, the MBCFET is able to reduce the effects of short channels and preserve its performance even with a range of device sizes [18]. Because of their scalability, MBCFET-based devices may adjust to progressively smaller integrated circuits without compromising performance [16].

First off, improved current handling capabilities are provided by the multi-bridge channel design of the MBCFET. It is possible for the transistor to handle greater currents without experiencing localized hotspots or performance deterioration since the current flow is

spread across numerous bridge segments. Because of this, the MBCFET performs better overall and in terms of power handling, which makes it appropriate for high-power applications [12].

Second, short-channel effects are lessened by the MBCFET's segmented channel shape. Traditional transistors face difficulties with channel control and leakage currents when transistor size decrease [15]. But the segmented channel of the MBCFET shortens the effective channel length, reducing the impacts of short channels and providing greater control over device functioning, particularly in sub-100-nanometer technology nodes [18].

2.3 Vertical Field-Effect Transistor (VFET)

The Vertical Field-Effect Transistor (VFET) is a transistor arrangement that is different from traditional transistor layouts in that its channel is vertical. The gate electrode encircles the channel on all sides as it travels vertically through the semiconductor substrate in the VFET [9]. There are various technological advantages to this structural decision.

First off, because of its vertical channel design, the VFET has excellent gate control and low leakage current. This makes it easier for the gate and the channel to couple more effectively, which improves electrostatic control over transistor functioning [19]. As a result, leakage currents are reduced, especially in off-state situations, which makes the VFET an excellent choice for low-power applications where reducing power consumption is crucial [15].

Furthermore, the VFET's vertical channel layout makes it easier for smaller technology nodes to scale. As device dimensions' decrease, traditional planar transistors face issues such as short-channel effects and gate leakage. VFET's vertical channel architecture, on the other hand, helps to mitigate these problems by permitting transistor size to be scaled farther without compromising reliability and performance. Because of its scalability [15], VFET-based devices can fulfil the demands of increasingly shrunk integrated circuits and keep up with advances in semiconductor technology [18].

Moreover, the vertical channel structure of VFETs provides benefits in terms of integration and device density [3]. Engineers can achieve higher device densities and packing densities by stacking numerous VFETs vertically as opposed to planar transistor architectures. This makes it easier to create integrated circuits with improved functionality that are more compact and efficient [7].

3. PROPOSED WORK

New semiconductor technologies are being explored at a rapid pace due to the persistent demand for energy-efficient electronic equipment. Because of their distinctive structural design and potential benefits for low-power applications, the Vertical Gate-All-Around Multi-Bridge Channel Field-Effect Transistors (VGAA-MBCFETs) have emerged as one of the most promising options among

them. This study addresses the urgent need for energy-efficient semiconductor solutions by proposing an inquiry into the application of VGAA-MBCFETs.

The rise of battery-powered systems, IoT devices, and portable electronics highlights how crucial it is for semiconductor devices to have as little power consumption as possible. The optimal energy efficiency of conventional transistor architectures is limited by design, especially when operating speeds rise and device dimensions get smaller. With its unique vertical gate-all-around construction and multi-bridge channel design, the VGAA-MBCFETs present a strong substitute that promises better performance and energy efficiency. Examining VGAA-MBCFETs potential for low-power applications has important ramifications for improving semiconductor technology and satisfying the market's increasing need for environmentally friendly electronics.

3.1 Proposed Methodology

Vertical Gate-All-Around Multi-Bridge Channel Field-Effect Transistors (VGAA-MBCFETs) for low-power applications are being studied using a structured technique that includes simulation, analysis, and optimization.

The study's initial focus will be on creating thorough device models with sophisticated simulation software Sentaurus TCAD [20]. The complex structural characteristics of VGAA-MBCFETs, such as the multi-bridge channel layout and vertical gate-all-around design, will be included in these models. The electrical properties of VGAA-MBCFETs will be carefully examined by rigorous simulation under various operating situations, such as gate and drain voltages. From these simulations, important performance parameters such as leakage current, subthreshold swing, and on-off ratio will be taken out and used to evaluate if the device is suitable for low-power operation.

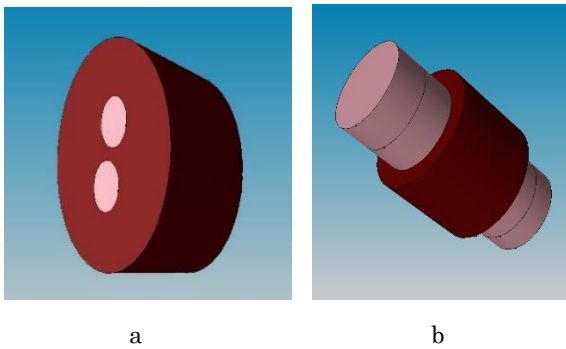


Fig. 1 – Structure of VGAA-MBCFET: (a) Internal structure of separated channel, (b) Structural simulation of VGAA-MBCFET

A sensitivity study will next be carried out to determine the crucial factors affecting the performance of the VGAA-MBCFET. To comprehend their influence on device behavior, variations in structural parameters such channel width, doping profile, gate oxide thickness, and material characteristics will be investigated. The ideal parameter values that optimize device efficiency while

minimizing power consumption will be determined with the help of this analysis.

To obtain a better understanding of the behavior of VGAA-MBCFET, graphical representations of the simulation findings, including I-V characteristics and transfer characteristics, will be created and examined. To verify the accuracy of the device models, these graphical representations will be compared with experimental data and theoretical predictions.

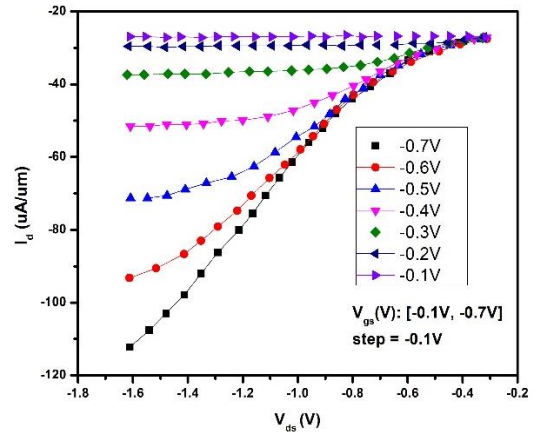


Fig. 2 – I-V Characteristics of VGAA-MBCFET

In order to improve the energy efficiency of VGAA-MBCFETs for low-power applications, more optimization techniques will be investigated. To reduce power consumption while maintaining device performance, strategies such structural alterations, gate engineering, and channel doping optimization will be looked into. To determine the efficacy of the optimized VGAA-MBCFET designs, simulated results will be compared to important performance criteria. In order to assess the variability and reliability of the device, statistical analysis will also be done. We'll identify the variables that cause unpredictability and investigate ways to reduce it in large-scale production.

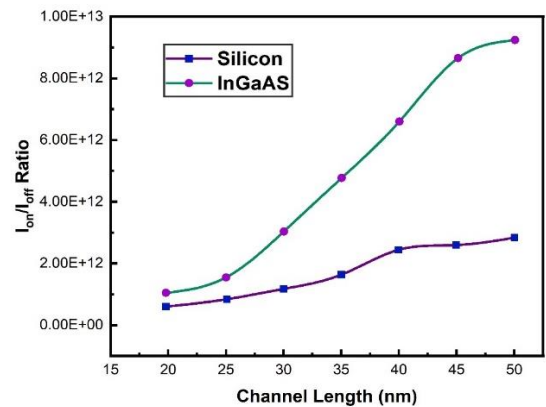


Fig. 3 – Validation of I_{on}/I_{off} Ratio by varying the Channel Length

It is crucial to validate the I_{on}/I_{off} ratio in Vertical Gate-All-Around Multi-Bridge Channel Field-Effect

Transistors (VGAA-MBCFETs) study by adjusting the channel length. One important indicator of the transistor's effectiveness in switching between the on and off states is the I_{on}/I_{off} ratio. Through a methodical manipulation of the channel length and observation of its effect on the I_{on}/I_{off} ratio, those can acquire vital insights into the performance parameters of the device. A thorough grasp of how variations in channel length impact the transistor's capacity to conduct current while it is in the on-state and reduce leakage current when it is in the off-state is made possible by this validation process.

The optimization of VGAA-MBCFET designs for specific applications is made much simpler by these findings, especially in low-power settings where energy efficiency is dependent on limiting leakage current. Furthermore, confirming the I_{on}/I_{off} ratio by changing the channel length advances our knowledge of semiconductor device physics and facilitates the creation of more precise device models. This in turn makes it easier to create VGAA-MBCFET-based integrated circuits that are more dependable and efficient and that are suited to the needs of cutting-edge applications and technologies that have strict power requirements.

Therefore, a critical first step toward improving our knowledge and use of VGAA-MBCFETs in semiconductor technology is the validation of the I_{on}/I_{off} ratio through variations in channel length. The behavior of Vertical Gate-All-Around Multi-Bridge Channel Field-Effect Transistors (VGAA-MBCFETs) as the gate length fluctuates can be profoundly understood from the transfer characteristics graph. The gate length in VGAA-MBCFETs is crucial for controlling the current that flows through the transistor channel. The degree of control that the gate exerts over the channel varies with gate length, which in turn affects how well the device performs. Several important findings can be observed when VGAA-MBCFETs with different gate lengths (e.g., 30 nm, 40 nm, 50 nm, and 60 nm) are plotted. From which it is observed that the 30nm gate length has the higher current gain in the VGAA-MBCFET.

Initially, as the gate length gets shorter, the threshold voltage usually shifts towards lower values, indicating improved gate control. Furthermore, shorter gate lengths

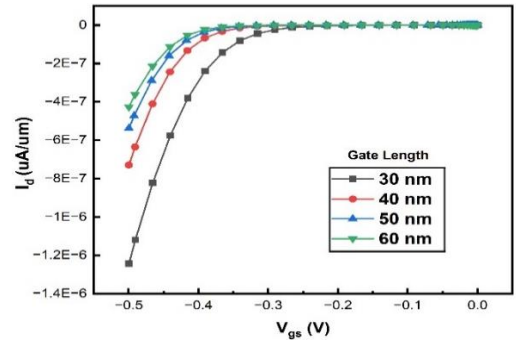


Fig. 4 – Transfer Characteristics of VGAA-MBCFET

frequently result in subthreshold swings that are steeper, which indicates better gate control and fewer leakage currents. Furthermore, because of improved carrier mobility in the channel region and increased gate-channel coupling, shorter gate lengths are typically associated with higher transconductance values. Additionally, the gate length affects the saturation behavior of drain current, with shorter lengths generally showing a faster saturation onset. Moreover, shorter gate lengths typically result in lower off-state leakage currents, which is indicative of better gate control and less channel resistance and better gate current control.

4. CONCLUSION

The study of Vertical Gate-All-Around Multi-Bridge Channel Field-Effect Transistors (VGAA-MBCFETs) proves that these transistors are promising for low-power applications due to their unique vertical design and multi-bridge architecture. VGAA-MBCFETs provide better current control and reduced leakage currents compared to previous technologies such as FinFETs and GAAFETs, which allows for lower power consumption and higher efficiency in small process nodes. The simulations and analysis demonstrated significant potential for optimizing the performance of these transistors, making them promising for the further development of energy-efficient integrated circuits and portable electronic devices.

REFERENCES

- J.P. Colinge, C.W. Lee, A. Afzalain, N.D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'neill, A. Blake, M. White, A.M. Kelleher, *Nat. Nanotechnol.* **5** No 3, 225 (2010).
- K.W. Ang, K.J. Chui, V. Bliznetsov, A. Du, N. Balasubramanian, M.F. Li, G. Samudra, Y.C. Yeo, *In IEDM Technical Digest. IEEE International Electron Devices Meeting*, 1069, (2004).
- Y. Liu, O. Gluschenkov, J. Li, A. Madan, A. Ozcan, B. Kim, T. Dyer, A. Chakravarti, K. Chan, C. Lavoie, I. Popova, *In IEEE Symposium on VLSI Technology* **44**, (2007).
- Z. Ren, G. Pei, J. Li, B.F. Yang, R. Takalkar, K. Chan, G. Xia, Z. Zhu, A. Madan, T. Pinto, T. Adam, *In IEEE Symposium on VLSI Technology* **172** (2008).
- V.V. Kozlovski, A.E. Vasil'ev, V.V. Emtsev, G.A. Oganessian, A.A. Lebedev, *J. Surf. Invest.* **13** No 6, 1155 (2019).
- T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, *IEEE International Electron Devices Meeting* **11** (2003).
- T. Mizuno, N. Sugiyama, T. Tezuka, Y. Moriyama, S. Nakaharai, T. Maeda, S. Takagi, *IEEE Digest of Technical Papers. Symposium on VLSI Technology* 202 (2004).
- A.A. Toropov, O.G. Lyublinskaya, B.Y. Meltser, V.A. Solov'ev, A.A. Sitnikova, M.O. Nestoklon, O.V. Rykhova, S.V. Ivanov, K. Thonke, R. Sauer, *Phys. Rev. B: Condens. Matter.* **70** No 20, 205314 (2004).
- C.H. Ge, C.C. Lin, C.H. Ko, C.C. Huang, Y.C. Huang, B.W. Chan, B.C. Perng, C.C. Sheu, P.Y. Tsai, L.G. Yao, C.L. Wu, *IEEE International Electron Devices Meeting*, 3 (2003).
- M. Hasan, *PhD-thesis* (2011).

11. A. Pal, A. Sarkar, *Eng. Sci. Technol. Int. J.* **17** No 4, 205 (2014).
12. G.V. Reddy, M.J. Kumar, *IEEE Trans. Nanotechnol.* **4** No 2, 260 (2015).
13. M.T.B. Kashem, S. Subrina, *Int. J. Numer. Modell. Electron. Networks. Dev. Fields.* **32** No 1, e2476 (2019).
14. J.C. Pravin, D. Nirmal, P. Prajoon, *J. Physica E.* **83**, 95 (2016).
15. S.A. Kumar, J.C. Pravin, *J. Nano- Electron. Phys.* **13** No 1, 01005 (2021).
16. H. Lou, L. Zhang, Y. Zhu, X. Lin, S. Yang, J. He, M. Chan, *IEEE Trans. Electron Dev.* **59** No 7, 1829 (2012).
17. V.R. Samaju, P.K. Tiwari, *Int. J. Numer. Modell. Electron. Networks Devices Fields* **29** No 4, 695 (2016).
18. Y.R. Lin, Y.Y. Yang, Y.H. Lin, E.D. Kurniawan, M.S. Yeh, L.C. Chen, Y.C. Wu, *IEEE J Electron Dev. Soc.* **6**, 1187 (2018).
19. S.A. Kumar, J.C. Pravin, *IETE J. Res.* **1** (2021).
20. http://www.sentaurus.dsod.pl/manuals/data/sdevice_ug.pdf

Аналіз продуктивності багатомостового багатоканального польового транзистора Vertical Gate All-Around для малопотужних додатків

S.B. Lenin¹, S.A. Kumar², T. Sibbi¹, T. Kumaran¹, R. Pravin¹

¹ Department of ECE, Sri Manakula Vinayagar Engineering College, Madagadipet Puducherry, India

² Department of ECE, Karpagam Academy of Higher Education, India

Дослідження зосереджено на багатомостовому польовому транзисторі з вертикальним затвором (VGAA-MBCFET), який є критично важливим компонентом у розробці малопотужних програм. Досліджується кілька стратегій оптимізації для покращення продуктивності VGAA-MBCFET, з особливим акцентом на покращенні коефіцієнта увімкнення/вимкнення, зменшенні струму витоку та точному налаштуванні ВАХ. Дослідження підкреслює характерну структуру вертикального затвора та переваги масштабованості, які відрізняють VGAA-MBCFET від горизонтальних аналогів, таких як FinFET і бічні GAAFET. Поглиблені дослідження масштабованості VGAA-MBCFET до менших технологічних вузлів є значним пріоритетом, оскільки визнано вирішальним для впливу на майбутні складні і компактні інтегральні схем. У документі визнається революційний вплив цих інновацій на вдосконалення великомасштабної інтеграції (LSI), а також їхній вплив на траєкторію носимих технологій у ширшому контексті мініатюризації інтегральних схем. Проблеми, пов'язані зі скороченням, відкрито обговорюються з визнанням їх складності, впливу на продуктивність і функціональність одягу. Оскільки носійна технологія спрямована на об'єднання високопродуктивних обчислювальних систем, це дослідження розглядає обмеження традиційних технологій і досліджує, чи можуть VGAA-MBCFETs бути трансформаційною технологією, що дозволяє створювати компактні, але потужні конструкції в енергоефективних електронних гаджетах. Дослідження використовує надійні підходи до моделювання, щоб забезпечити повне розуміння можливостей і можливих застосувань VGAA-MBCFETs, забезпечуючи значний внесок у поточний прогрес технології електронних пристроїв малої потужності.

Ключові слова: Широкомасштабна інтеграція (LSI), Коефіцієнт увімкнення/вимкнення, Масштабованість, Вертикальна структура затвору.