Effect of High-$k$ Dielectric Materials on Short Channel Effects of a 14 nm Tri-Gate SOI FinFET for Reduced Area on Chip

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While entering the era of More than Moore by reducing the geometrical dimensions for FET devices to accommodate more components on a single chip, short channel effects (SCEs) like higher leakage currents, Drain Induced Barrier lowering (DIBL), etc., create a major hindrance. Employing high-$k$ dielectrics as gate oxide is being a meticulous approach today on attaining an enhanced device. The objective of this work is to develop and characterize a 14 nm gate length Tri-Gate $n$-FinFET device and compare the effects of short channel parameters. This is achieved by replacing the SiO$_2$ gate oxide with various high-$k$ dielectric materials like Si$_3$N$_4$, Al$_2$O$_3$, ZrO$_2$ and HfO$_{2x}$. Here, the 14 nm gate length Tri-Gate $n$-FinFET device is developed and modelled using SILVACO TCAD tools. The SOI structure is also implemented here for betterment in device performance. Multiple devices are developed with varied gate oxides of SiO$_2$ and other high-$k$ dielectrics like Si$_3$N$_4$, Al$_2$O$_3$, ZrO$_2$ and HfO$_{2x}$ as the gate dielectric material considering the equivalent oxide thickness calculation on the same structure. The short channel device parameters such as threshold voltage, $I_{on}$ current, $I_{off}$ current, subthreshold slope, DIBL, and $I_{on}$/$I_{off}$ current ratio were systematically analyzed for different devices. The comparison of different developed devices showed that the $I_{on}$ current was almost the same for all the devices. However, the $I_{off}$ current reduced with increasing dielectric constants thereby increasing the $I_{on}$/$I_{off}$ ratio which led to lower leakage currents and better device performance. Similarly, the devices which comprised of higher dielectric constants had lower subthreshold swings and lower DIBL values leading to reduction in SCEs. Thus, the 14 nm gate length Tri-Gate $n$-FinFET device was developed and modelled successfully, and the results showed improved SCEs of the developed device by using HfO$_{2x}$ dielectrics with reduced chip area.

Keywords: High-$k$ dielectric materials, TG SOI FinFETs, Silvaco TCAD, EOT.

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1. INTRODUCTION

CMOS technology has been the choice of chip design and manufacturing for more than six decades now, where MOSFETs form an integral part. But this era is converging as the device integration densities need increment for higher speed and lower power to be at par with Moore’s law [1, 2]. This leads to drastic scaling of MOSFETs leading to Short Channel Effects (SCEs), higher leakage currents, hot carrier effect and Drain Induced Barrier Lowering (DIBL) [3].

With shrinking device geometries, the thickness of the gate-oxide layer is decreased simultaneously. With SiO$_2$ layer reaching 2 nm, a sudden rise in the gate leakage current due to tunneling is evident [4]. Thus, a need to substitute SiO$_2$ as the gate dielectric with high-$k$ (high permittivity) dielectric is need of the hour to significantly decrease the leakage of the gate current. This concept thereby stands as the core of the paper here. The high-$k$ dielectric material increases the gate capacitance without the leakage effects and increases the $I_{on}$ current [5]. The choice of a high-$k$ dielectric material also depends on its ability to provide acceptable level of leakage as well as improved mobility of the charge carriers. The SCEs can be reduced further by increasing the number of gates of the FinFET device. The Tri-Gate (TG) FinFETs due to their excellent immunity to SCEs are better choice of devices.

Based on the motivation to prepare a more susceptible device to be prone for less current leakage, a varied range of high-$k$ dielectric material based devices are deployed and studied here. Their characteristics are compared considering the equivalent oxide thickness (EOT) of 1 nm SiO$_2$ on the same TG FinFET structure thereby proposing and providing a superior design of future device.

2. DEVICE STRUCTURE AND THEORY

The circuit schematic of a TG SOI FinFET is described by the length of the fin ($L_{f,0}$), fin height ($H_{f,0}$), and thickness of silicon ($W_{Si,0}$). The detailed basic geometric dimensions of the device are also tabulated in Table 1. The designing and modelling of the device is done by SILVACO Atlas simulator [6].

Multiple high-$k$ materials like Si$_3$N$_4$ ($k = 7.8$), Al$_2$O$_3$ ($k = 9.3$), ZrO$_2$ ($k = 22$), HfO$_2$ ($k = 25$) and SiO$_2$ ($k = 3.9$) is used to develop FinFET based devices with varied gate dielectric materials and to reduce the short channel effects further which is scaled to have an equivalent oxide thickness (EOT) of 1 nm of SiO$_2$. Characteristics of all the devices are thereafter compared considering this EOT for the same TG FinFET structure.

The EOT is calculated based on the equation (1) given as [7]:

$$
EOT = t_{high-k} \cdot \frac{k_{SiO_2}}{k_{high-k}}
$$

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where $t_{\text{high-k}}$ is the physical thickness of the high-$k$ material, $k_{\text{SiO}_2}$ is the dielectric constant of SiO$_2$ and $k_{\text{high-k}}$ is the dielectric constant of the high-$k$ material.

<table>
<thead>
<tr>
<th>Table 1 – Characteristics of a TG n-FinFET</th>
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<td><strong>Notations</strong></td>
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<td>$L_D$, $L_S$</td>
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<tr>
<td>$L_o$</td>
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<tr>
<td>$T_{ox}$ (SiO$_2$)</td>
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<td>$W_{fin}$</td>
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![Fig. 1 – $I_D$-$V_{GS}$ characteristics of a TG FinFET with different gate oxide materials on a linear scale at $V_{GS} = 0.1$ V](image)

![Fig. 2 – Variation of threshold voltage ($V_{th}$) of a TG n-FinFET with various gate dielectric materials](image)

3. RESULTS AND DISCUSSION

The 3D FinFET is designed using SILVACO for various gate oxide materials. The $I_D$-$V_{GS}$ characteristics are plotted in Fig. 1 using linear scale for SOI TG FinFET device with various gate dielectric materials. The Si$_3$N$_4$ dielectric material is slightly better than SiO$_2$ in terms of higher diffusion barrier. Al$_2$O$_3$ as a gate dielectric material shows better interface trap density. The dielectric HfO$_2$, due to the high barrier height, ensures lower leakage, thus limiting electron tunneling [8]. From Fig. 2, the threshold voltage of the device is detected to be 0.23 V for SiO$_2$, and the maximum threshold voltage is 0.29 V for HfO$_2$ at $V_{GS} = 0.1$ V, thereby also indicating a higher leakage for the device with SiO$_2$ as the gate oxide. The maximum on current $I_{on}$ is determined to be approximately same for all gate dielectrics at nearly 1.5 mA at $V_{GS} = 0.1$ V. Hence the device with HfO$_2$ as the dielectric holds an upper hand in respect to performance.

The threshold voltage ($V_{th}$), which is obtained from Fig. 2, is a deciding factor for achieving improved $I_{on}$ current, as it increases the speed of the circuit.

As the gate voltage increases, then, depending upon the threshold voltages, a sharp and large increase in the drain current occurs, which is also affected by the increase in drain voltage.

Fig. 3 depicts the $I_D$-$V_{GS}$ transfer characteristics on a logarithmic scale for the TG FinFET structure with various gate dielectric materials. $I_{off}$ is evaluated by using the equation (2) [9] below

$$I_{off}(nA) = 100 \frac{W}{L} \times 10^{v_{th}/SS},$$

where $W$ and $L$ are the width and length of the channel respectively, $V_{th}$ is the threshold voltage of the device, and SS is the subthreshold swing.

From Fig. 3, the $I_{on}$ and $I_{off}$ currents are obtained for all the devices. The leakage current, i.e., the $I_{off}$ current varies significantly in the range of picoamperes, as shown in Fig. 4, leading to distinctive variations in the $I_{on}/I_{off}$ current ratio. This clearly instigates that the device with highest $k$ value is expected to provide the least leakage through the gate, which is highly desired and beneficial for a better performing FinFET.

Fig. 5 depicts the on-to-off current ratio for different dielectric values. The ratio of $I_{on}$ to $I_{off}$ current shows a steady increase from SiO$_2$ to HfO$_2$ and it reaches a maximum of $1.35 \times 10^8$ for HfO$_2$, which is almost 5 times the value of SiO$_2$, thereby indicating the concerned device to be the best providing the least gate-leakage.

Fig. 6 shows the $I_D$-$V_{GS}$ characteristics of a TG n-FinFET device with different gate dielectric materials, where $V_{GS}$ is kept constant at 0.5 V. It is evidently

![Fig. 3 – $I_D$-$V_{GS}$ characteristics of a TG FinFET with different gate oxide materials on a log scale at $V_{GS} = 0.1$ V](image)
Effect of High-k Dielectric Materials on Short ...

![Diagram](image1)

**Fig. 4** – Variation of off current ($I_{off}$) of a TG FinFET with various gate dielectric materials

![Diagram](image2)

**Fig. 5** – Variation of $I_{on}/I_{off}$ ratio of a TG FinFET with various gate dielectric materials

![Diagram](image3)

**Fig. 6** – $I_D-V_{DS}$ characteristics of a TG FinFET with different gate dielectric materials at $V_{GS} = 0.5$ V

observed that the saturation region is obtained speedily for all the gate dielectric materials, though for the device with HfO$_2$ the increment in saturation region is reasonably observable indicating enhanced performance.

The SS parameter for the TG FinFET with SiO$_2$ as a dielectric material is determined to be 66.75 mV/decade, while for HfO$_2$ it is calculated to be 61.68 mV/decade as obtained from Fig. 7, thereby, clearly indicating that the device with HfO$_2$ provides the best result (least leakage).

The DIBL is another major SCE which should be minimal for improvement in the operation of the device and for the device to perform healthier. The DIBL for all the devices is calculated using the standard equation (3) as in [10]:

$$DIBL (\text{mV/V}) = \frac{V_{TH}}{V_{DSS}}$$  \hspace{1cm} (3)

where $V_{TH}$ is the change in the threshold voltage and $V_{DSS}$ is the change in the drain-to-source voltage. DIBL is thereafter plotted in Fig. 8, and the device with high-$k$ of HfO$_2$ outshined others and proved to be the best performing FinFET among the devices analyzed.

DIBL is therefore determined for various high-$k$ dielectric material based FinFETs, and the concerned data is plotted as shown in Fig. 8. It is observed that HfO$_2$ provided minimum DIBL of 35.01 mV/V, whereas the maximum DIBL of 105.58 mV/V is achieved for SiO$_2$ FinFET. A clear indication is observed that the HfO$_2$ stands to be the best suitable candidate with minimal leakage for a 14 nm gate length TG FinFET with EOT of 1 nm (SiO$_2$).

![Diagram](image4)

**Fig. 7** – Variation of subthreshold swing (SS) of a TG FinFET with various gate dielectric materials

![Diagram](image5)

**Fig. 8** – Comparison of DIBL of a TG FinFET with various gate dielectric materials

4. CONCLUSIONS

The performance of SiO$_2$, Si$_3$N$_4$, Al$_2$O$_3$, ZrO$_2$ and HfO$_2$ as different gate dielectric material is compared in a TG SOI n-FinFET with 14 nm channel length and minimal device area which is developed using Silvaco TCAD software. The thickness of the oxide layer was kept at 1 nm EOT of SiO$_2$. The threshold voltage, $I_{on}/I_{off}$ current ratios of the device were compared for different dielectrics. Improvements in $I_{on}$, $I_{off}$ and $I_{on}/I_{off}$ for the device with HfO$_2$ high-$k$ dielectric are observed. The $I_{on}/I_{off}$ ratio obtained for HfO$_2$ ($k = 25$) is $1.35 \times 10^6$ and SiO$_2$ ($k = 3.9$) is $2.77 \times 10^5$. Similarly, the SCEs like subthreshold swing and DIBL also showed...
improved results for the FinFET with HfO$_2$ as a dielectric material. Thus, TG FinFETs can be scaled down to gate lengths of 14 nm using high-$k$/metal gates and are possibly the best substitutes for extending the use of CMOS technology on and beyond 14 nm technology node.

REFERENCES


Вплив high-$k$ діелектричних матеріалів на короткоканальні ефекти 14 нм тризатворного транзистора SOI FinFET для зменшеної площини мікрокомпонент

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При зменшенні геометричних розмірів пристроїв FET для розміщення більшої кількості компонентів на одній мікрокомпоненті короткоканальних ефектів (SCEs), такі як більші струми витоку, індуковане відключення на одній мікрокомпоненті короткоканальні ефекти (SCEs), такі як більші струми витоку, індуковане відключення діелектричных матеріалів, таких як Si$_3$N$_4$, Al$_2$O$_3$, ZrO$_2$, та HfO$_2$. У роботі тризатворний транзистор $n$-FinFET з довжиною затвора 14 нм розроблено і змодельовано за допомогою інструментів Silvaco TCAD. У роботі також реалізовано структуру SOI для підвищення продуктивності пристрою. Розроблено кілька пристроїв з різними оксидами затвора SiO$_2$ і іншими high-$k$ діелектриками, такими як Si$_3$N$_4$, Al$_2$O$_3$, ZrO$_2$ та HfO$_2$, як матеріалами затвора з урахуванням розрахунку еквівалентної товщини оксиду на одній і тій же структурі. Параметри короткоканального пристрою, такі як порогова напруга, струми $I_{on}$ та $I_{off}$, порогова крутизна характеристики, DIBL і відключення $I_{on}/I_{off}$ систематично аналізувалися для різних пристроїв. Порівняння різних зменшених пристроїв показало, що струм $I_{on}$ був практично однаковим для всіх пристроїв. Однак струм $I_{off}$ знижувався зі збільшенням діелектричної проникності.

Ключові слова: High-$k$ діелектричні матеріали, TG SOI FinFETs, Silvaco TCAD, EOT.