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HIGH-K HFO_2 BASED METAL-OXIDE-SEMICONDUCTOR DEVICES USING SILICON AND SILICON CARBIDE SEMICONDUCTOR

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In this paper we have calculated the flatband capacitance (C_{FB}) for high-k dielectric material hafnia oxide (HfO_2) as an insulator and silicon carbide (SiC) as a semiconductor material for metal-oxide-semiconductor (MOS) devices. We simulate the capacitance-voltage (C-V) characteristics of the MOS devices with ultrathin oxide using ATLAS, a commercially available TCAD tool from SILVACO. The tool has investigated the effect on C-V characteristics of different oxide thickness and doping concentration of SiO_2 and HfO_2 as insulators and Si and SiC as semiconductor based MOS devices. Excellent agreement was observed over a wide range of oxide thickness and substrate doping for the materials. The C-V characteristics of different polytype of SiC semiconductor also studied for n-type MOS devices.

Keywords: *C-V CHARACTERISTICS, HfO_2, MOS, SILICON CARBIDE, FLATBAND CAPACITANCE.*

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1. INTRODUCTION

In attempt to replace conventional SiO_2 with new high-k materials, HfO_2 has received tremendous attention [1] as a future gate dielectric for sub-100 nm technology due to its high dielectric constant, reasonable barrier height and superior thermodynamic stability with Si. The high-k value along with high bandgap motivates this replacement. The properties of various promising high-k dielectric materials are compared [2] in Table 1. The continually shrinking gate-oxide thickness results in direct tunnelling and excessive leakage currents in Si-based MOS devices. One of the promising materials in the high-k dielectric family is HfO_2. The electrical and other physical properties of HfO_2 have been widely studied [3-13] due to its low leakage current, larger conduction band offset, and acceptable thermal stability. Today Si is the material dominating for Ultra Large Scale Integration (ULSI) circuit design in electronics Industry. SiC materials however are presently metamorphosing from research and development into a commercial market driven manufacturing product [14]. Promising markets for SiC material include high-power switching devices [15-16] and microwave devices [17]. These thrilling device results stem primarily from the exploitation of the unique electrical and thermophysical properties offered by SiC compared to Si, Ge and GaAs. For the high saturated electron drift velocity, high breakdown field, high thermal

conductivity, and wide bandgap SiC is considered as the important material to fabricate the high power, compact, high temperature and high frequency devices [18]. Due to the differing crystal structures of Si and C atoms within the SiC crystal lattice, each SiC polytype (3C-, 4H-, and 6H-SiC) exhibits exclusive fundamental electrical and mechanical properties [19-21].

Table 1 *– Properties of high-k dielectric materials*

Material	Dielectric constant (ε)	Bandgap, E_g (eV)	Conduction band offset to Si (eV)	Crystal Structure
SiO_2	3.9	9	3.5	Amorphous
Si_3N_4	7	5.3	2.4	Amorphous
Al_2O_3	9	8.8	2.8	Amorphous
$HfSiO_4$	15	6	1.5	Amorphous
Y_2O_3	15	6	2.3	Cubic
$ZrSiO_4$	15	6	1.5	Amorphous
HfO_2	25	6	1.5	Monoclinic, Tetragonal
ZrO_2	25	5.8	1.4	Monoclinic, Tetragonal
Ta_2O_5	26	4.4	0.3	Orthorhombic
La_2O_3	30	6	2.3	Hexagonal, Cubic
TiO_2	80	3.05	0.0	Tetragonal

In this paper, the effect of change of oxide thickness and Si doping concentration on the C–V characteristics of MOS devices has been studied. SiO_2 and HfO_2 have been considered as gate dielectrics, Si and SiC have been considered as semiconductors material, aluminium is the electrode and their performance has been investigated. The effect on C-V characteristics of different polytype of SiC (3C-, 4H-, and 6H-SiC) semiconductors for n-type MOS devices also studied by the simulator.

2. CALCULATION OF C_{FB}

If the thermal voltage $V_T = q/(kT)$, q is the electronic charge, k is the Boltzmann constant, T is the temperature, N_{po} and P_{po} are the equilibrium densities of electrons and holes in the bulk of the semiconductor respectively at the surface, the surface potential $\psi = \psi_s$, the differential capacitance (C_D) of the semiconductor depletion layer is given by [22]:

$$C_D = \frac{\partial Q_s}{\partial \psi_s} = \frac{\partial}{\partial \psi_s}\left[\frac{\sqrt{2}kT\,\varepsilon_s}{qL_D}\left\{\left(e^{-V_T\psi_s} + V_T\psi_s - 1\right) + \frac{N_{po}}{P_{po}}\left(e^{V_T\psi_s} - V_T\psi_s - 1\right)\right\}^{1/2}\right] \quad (1)$$

Where:

$$L_D = \sqrt{\frac{kT\,\varepsilon_s}{P_{po}q^2}} = \sqrt{\frac{\varepsilon_s}{qV_T P_{po}}} = Debye\ Length \quad (2)$$

At the flat band condition, that is $\psi_s = 0$, C_D can be obtained by expanding the exponential terms into series. The total capacitance of the system is a

series combination of the oxide capacitance (C_{OX}) and C_D For a given oxide thickness, t_{OX}, the value of C_{OX} is constant and correspondence to the maximum capacitance of the system. So the flatband capacitance is given by:

$$C_{FB}\left(\psi_s = 0\right) = C_{OX}\frac{\varepsilon_s}{L_D}\Bigg/\left(\frac{\in_{OX}}{t_{OX}} + \frac{\varepsilon_s}{L_D}\right), \tag{3}$$

Then by calculation with equation (2) and (3):

$$\frac{C_{FB}}{C_{OX}} = \left(1 + \frac{\in_{OX}}{\in_s}\sqrt{\frac{kT\varepsilon_s}{P_{po}q^2t_{OX}^2}}\right)^{-1} = \left(1 + \frac{\in_{OX}}{\in_s}\sqrt{\frac{kT\varepsilon_s}{N_A orN_D q^2t_{OX}^2}}\right)^{-1} \tag{4}$$

This is the general formula for calculation of C_{FB}/C_{OX} for any MOS devices. For standard Si/SiO_2 system the equation becomes:

$$\frac{C_{FB}}{C_{OX}} = \left(1 + \frac{7.84\sqrt{T}}{t_{OX}\sqrt{N_A orN_D}}\right)^{-1}, \tag{5}$$

For Si/HfO_2 based MOS system the equation can be written as:

$$\frac{C_{FB}}{C_{OX}} = \left(1 + \frac{50.22\sqrt{T}}{t_{OX}\sqrt{N_A orN_D}}\right)^{-1}, \tag{6}$$

Also for SiC / SiO_2 based system the equation becomes:

$$\frac{C_{FB}}{C_{OX}} = \left(1 + \frac{9.53\sqrt{T}}{t_{OX}\sqrt{N_A orN_D}}\right)^{-1}, \tag{7}$$

And for SiC / HfO_2 based MOS devices the equation can be written as:

$$\frac{C_{FB}}{C_{OX}} = \left(1 + \frac{61.091\sqrt{T}}{t_{OX}\sqrt{N_A orN_D}}\right)^{-1}. \tag{8}$$

3. RESULTS AND DISCUSSION

The MOS devices are simulated by versatile, modular and extensive solution TCAD tools ATLAS at high frequency (1 MHz). In Fig. 1 the C-V characteristics of Si and 6H-SiC as the substrate materials with substrate concentration as 1×10^{17} cm^{-3}, oxide thickness as 30 nm and oxide material as SiO_2 are shown in the respective graph. It shows almost identical, indicating a good interface quality of 6H-SiC / SiO_2. Moreover it is found, there is a shift in the gate voltage at which transition occurs towards negative value for 6H-SiC semiconductor. This is primarily due to large densities of interface state at the SiO_2/SiC interface [23]. These states are responsible for undesirable effects which hamper the development of the 6H-SiC semiconductor field effect transistor.

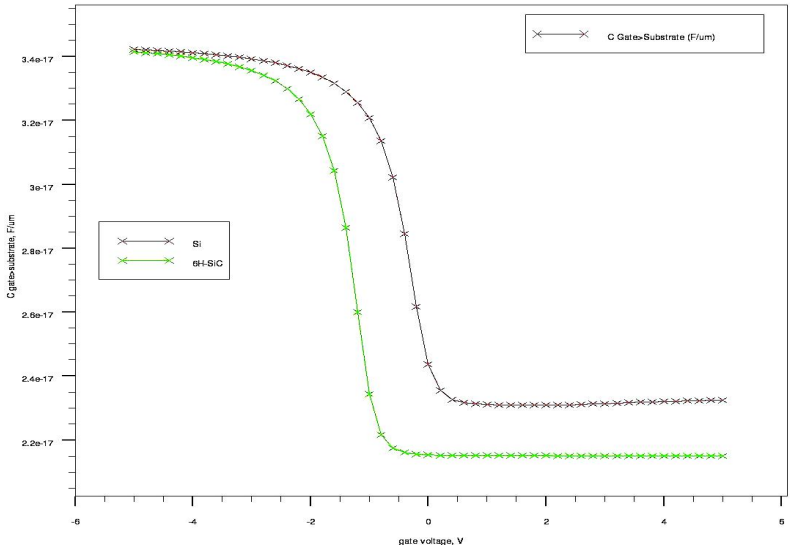

Fig. 1 – *C-V characteristics of* Si *and* SiC-4H

The variation of the gate to substrate capacitance with the gate voltage with different oxide thicknesses of the parameters are shown in Fig. 2 (a), (b), (c) and (d). The thicknesses are 20 nm, 30 nm, 40 nm, 50 nm and 60 nm. Both (Si and SiC-6H) the semiconductor with the insulators (SiO_2 and HfO_2) of the graphs shows that the value of the capacitance is higher at lower thicknesses. Hence working with the lower thicknesses will meet the essential requirement for having higher drive current.

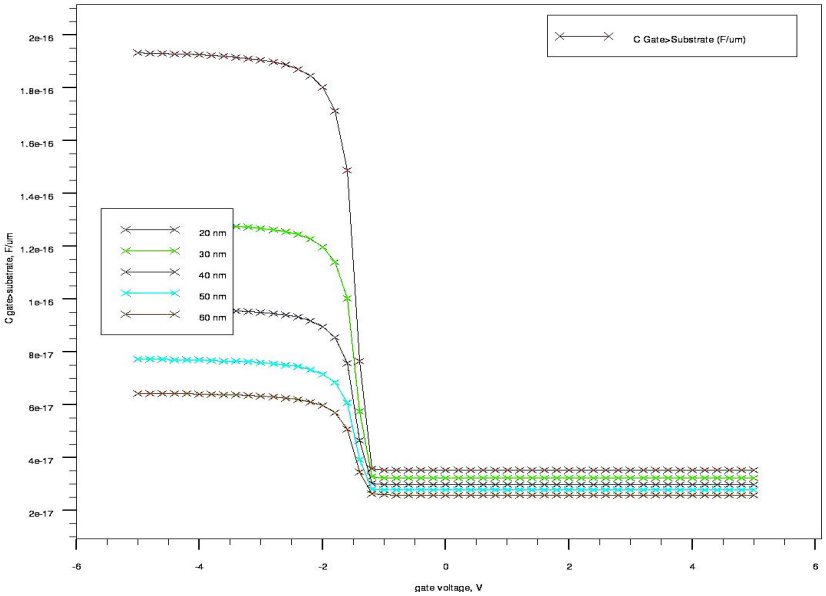

Fig. 2 (a) – *C-V characteristics of different Insulator thickness for* 6H-SiC/HfO_2

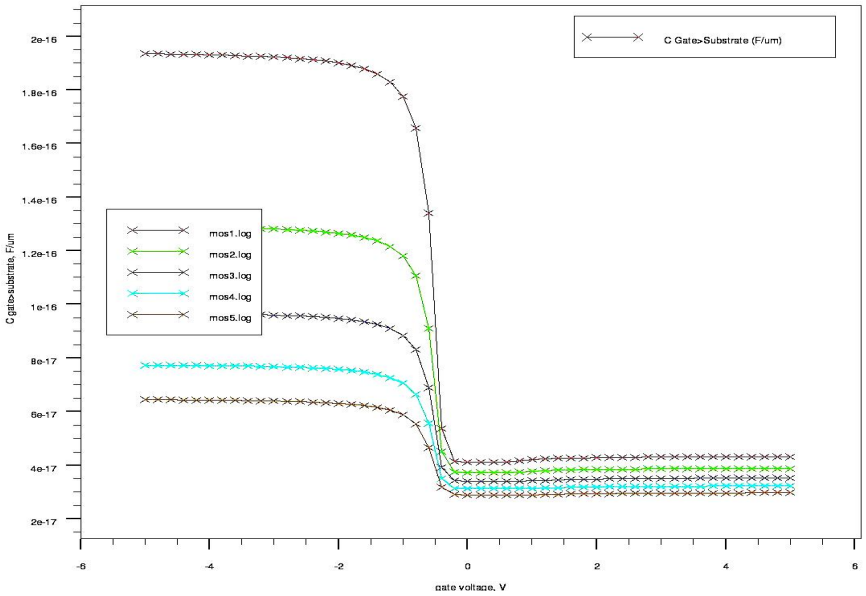

Fig. 2 (b) – *C-V characteristics of different Insulator thickness for* Si/HfO_2

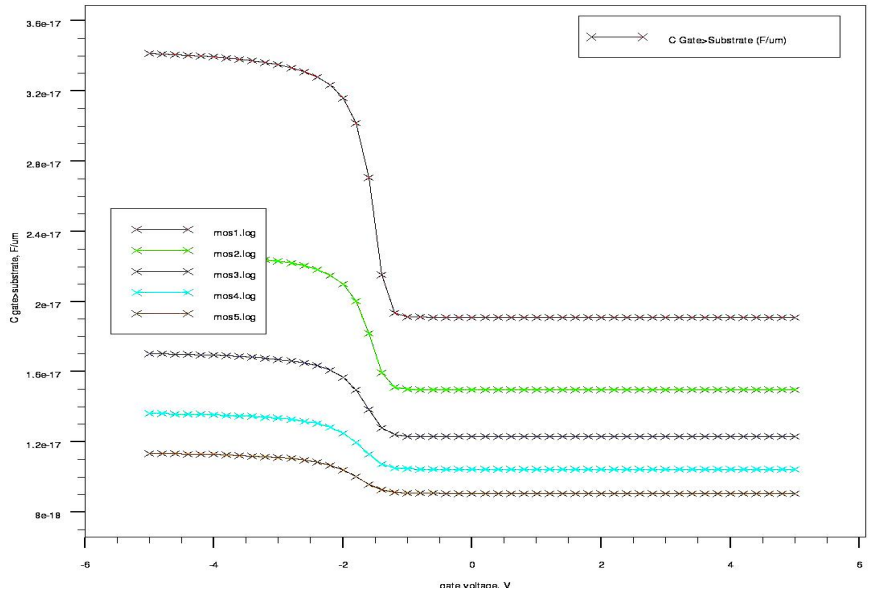

Fig. 2 (c) – *C-V characteristics of different Insulator thickness for* $6H\text{-}SiC/SiO_2$

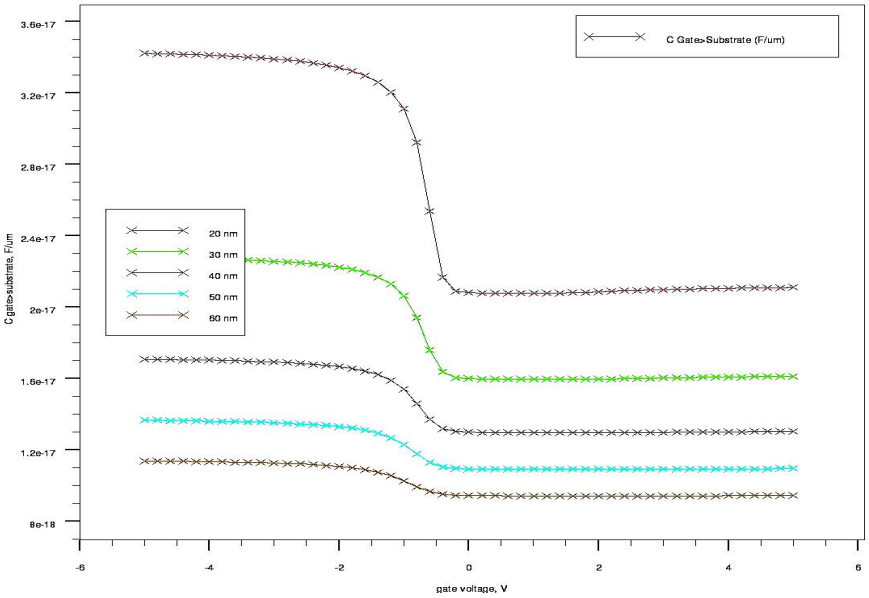

Fig. 2 (d) – *C-V characteristics of different Insulator thickness for* Si/SiO_2

The variation of the gate to substrate capacitance with the gate voltage with different substrate concentrations is shown in Fig. 3 (a) and (b). The concentrations are 1×10^{14} cm^{-3}, 1×10^{15} cm^{-3}, 1×10^{16} cm^{-3}, and 1×10^{17} cm^{-3}. It is found for the material HfO_2 that the relative change in the value of the gate voltage at which transition occurs is much smaller than for the material SiO_2 for different concentrations. This is an advantage of using HfO_2 as it results in better stability from the physics point of view. The transition gate voltage for HfO_2 is found to be nearly at zero voltage for all the concentrations, but for SiO_2 at lower concentration a higher threshold gate voltage is required.

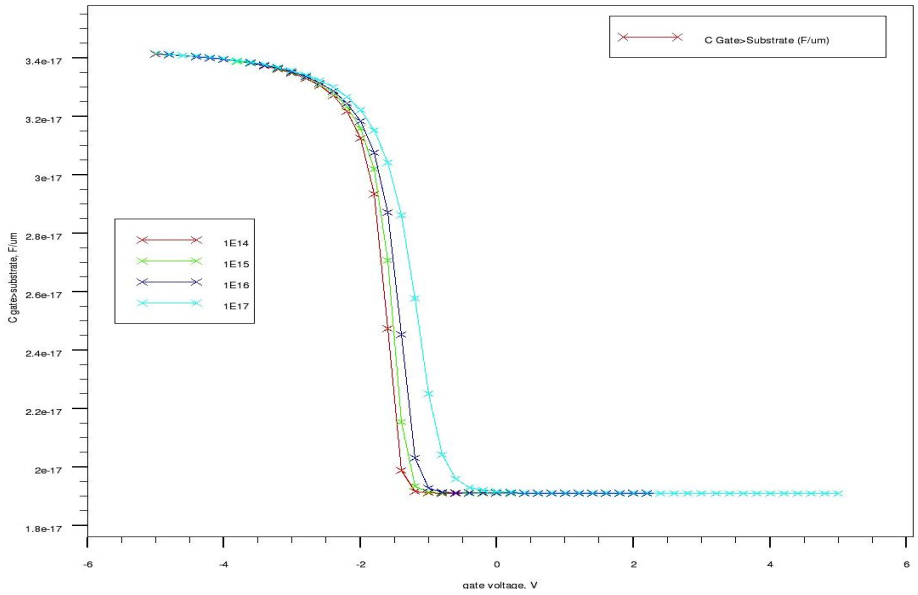

Fig. 3 (a) – *C-V characteristics of* 6H-SiC/SiO_2 *with different concentration*

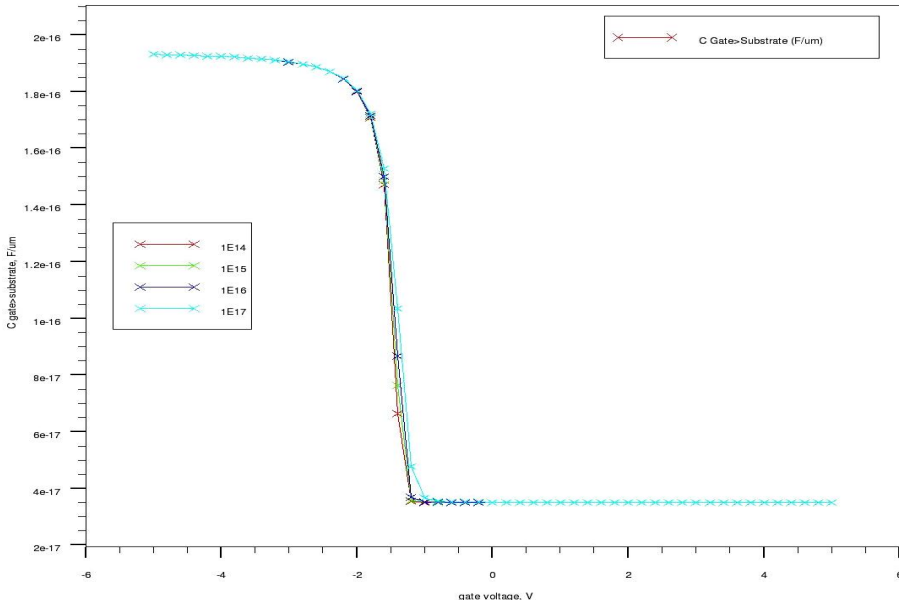

Fig. 3 (b) – *C-V characteristics of* 6H-SiC/HfO_2 *with different concentration*

In Fig. 4 the variation of the gate to substrate capacitance as a function of the gate voltage for different SiC polytypes (-4H, -6H, -3C) is shown. The transition which is the 3C-SiC polytype is found to have the transition gate voltage at nearly zero value, the value at which transition occur for Si substrate. Yet, 3C-SiC having lower bandgap, lower thermal conductivity and also lower carrier velocity than the other polytype, is seldomly used.

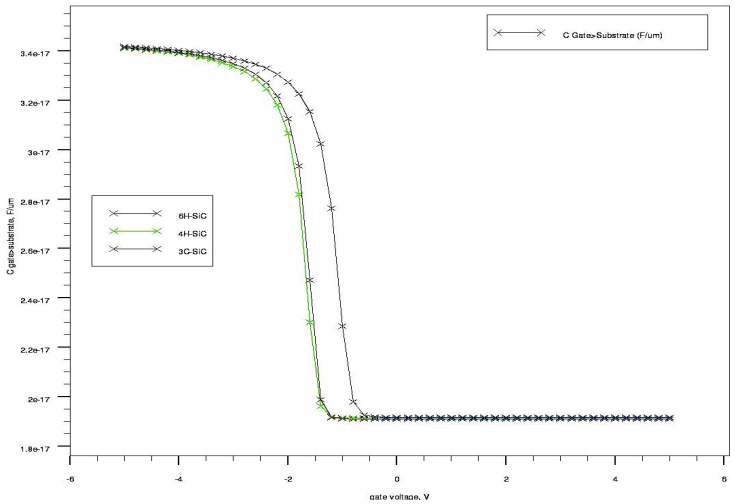

***Fig. 4** – C-V characteristics for different* 6H-SiC *polytype*

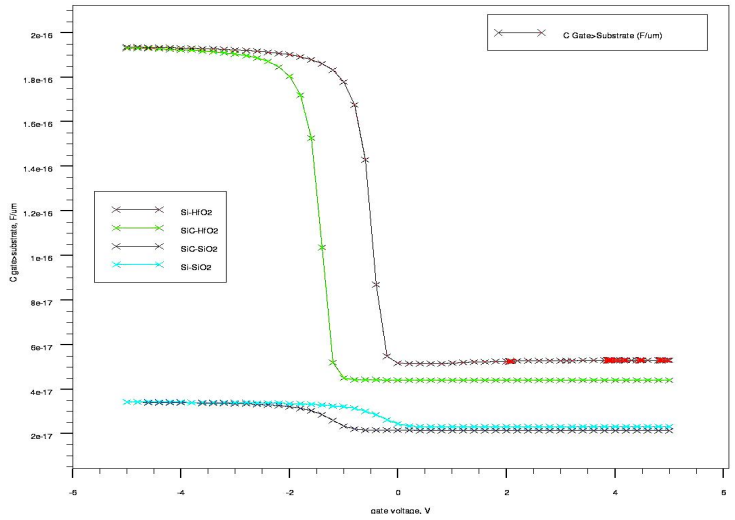

***Fig. 5** – C-V characteristics of Si and SiC semiconductor for* SiO_2 *and* HfO_2

The MOS structures with 6H-SiC and HfO_2 shows a higher change in the value of the capacitance than its other counterparts and results in a stable device. The transition is also found to be at zero gate voltage while that for Si and HfO_2 is more towards the negative gate voltage (see Fig. 5). The structure with Si and SiO_2 gives a view of the textual MOS characteristics while changing the semiconductor makes the transition to be at the negative gate voltage, the reasons for which are already stated before.

4. CONCLUSION

In this paper we present a comprehensive study of the C-V characteristics of Si and SiC substrate material for MOS devices with HfO_2 and SiO_2 as the

oxide for aluminium gate electrode has been carried out using ATLAS from SILVACO. Almost identical transitions in C-V are observed with the gate dielectric materials, showing better reliability of HfO_2 with significant reduction of tunnelling leakage current. The higher thickness of HfO_2 also results in lesser leakage current. The main drawback of SiC is the presence of the interface states at the SiO_2/SiC interface, which may be removed by improved oxidation process [23].

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